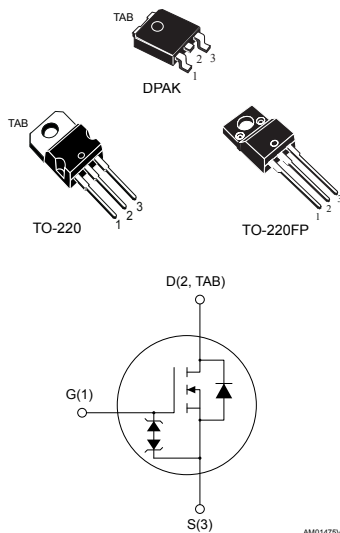


N-channel 400 V, 0.85 Ω typ., 5.4 A, SuperMESH™ Power MOSFETs in DPAK, TO-220 and TO-220FP packages



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STD7NK40ZT4	400 V	1 Ω	5.4 A	70 W
STP7NK40Z				70 W
STP7NK40ZFP				25 W

- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitance
- Zener-protected

Applications

- Switching applications

Description

These high-voltage devices are Zener-protected N-channel Power MOSFETs developed using the SuperMESH™ technology by STMicroelectronics, an optimization of the well-established PowerMESH™. In addition to a significant reduction in on-resistance, these devices are designed to ensure a high level of dv/dt capability for the most demanding applications.

Product status links

[STD7NK40ZT4](#)
[STP7NK40Z](#)
[STP7NK40ZFP](#)

Product summary

STD7NK40ZT4

Marking	D7NK40Z
Package	DPAK
Packing	Tape and reel

STP7NK40Z

Marking	P7NK40Z
Package	TO-220
Packing	Tube

STP7NK40ZFP

Marking	P7NK40ZFP
Package	TO-220FP
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value			Unit
		STD7NK40ZT4	STP7NK40Z	STP7NK40ZFP	
V _{DS}	Drain-source voltage	400			V
V _{DGR}	Drain-gate voltage (R _{GS} = 20 kΩ)	400			V
V _{GS}	Gate-source voltage	±30			V
I _D	Drain current (continuous) at T _C = 25 °C	5.4	5.4	5.4 ⁽¹⁾	A
	Drain current (continuous) at T _C = 100 °C	3.4	3.4	3.4 ⁽¹⁾	A
I _{DM} ⁽²⁾	Drain current (pulsed)	21.6	21.6	21.6 ⁽¹⁾	A
P _{TOT}	Total dissipation at T _C = 25 °C	70	70	25	W
I _{AR}	Avalanche current, repetitive or non-repetitive (pulse width is limited by T _J max.)	5.4			A
E _{AS}	Single pulse avalanche energy (starting T _J = 25 °C, I _D = I _{AR} , V _{DD} = 50 V)	130			mJ
ESD	Gate-source, human body model, R = 1.5 kΩ, C = 100 pF	3			kV
dv/dt ⁽³⁾	Peak diode recovery voltage slope	4.5			V/ns
V _{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s, T _C = 25 °C)			2.5	kV
T _J	Operating junction temperature range	-55 to 150			°C
T _{stg}	Storage temperature range				

1. This value is limited by maximum junction temperature.

2. Pulse width is limited by safe operating area.

3. I_{SD} ≤ 5.4 A, di/dt ≤ 200 A/μs, V_{DD} < V_{(BR)DSS}

Table 2. Thermal data

Symbol	Parameter	Value			Unit
		DPAK	TO-220	TO-220FP	
R _{thj-case}	Thermal resistance junction-case	1.78	1.78	5	°C/W
R _{thj-amb}	Thermal resistance junction-ambient			62.5	°C/W
R _{thj-pcb} ⁽¹⁾	Thermal resistance junction-pcb	50			°C/W

1. When mounted on an 1-inch² FR-4, 2 Oz copper board.

2 Electrical characteristics

($T_C = 25\text{ }^\circ\text{C}$ unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0\text{ V}$	400			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 400\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 400\text{ V}$, $T_C = 125\text{ }^\circ\text{C}^{(1)}$			50	μA
I_{GSS}	Gate body leakage current	$V_{GS} = \pm 20\text{ V}$, $V_{DS} = 0\text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 50\text{ }\mu\text{A}$	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 2.7\text{ A}$		0.85	1	Ω

1. Defined by design, not subject to production test.

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	535	-	μF
C_{oss}	Output capacitance			82		
C_{rss}	Reverse transfer capacitance			18		
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{GS} = 0\text{ V}$, $V_{DS} = 0\text{ to }320\text{ V}$	-	53	-	μF
Q_g	Total gate charge	$V_{DD} = 320\text{ V}$, $I_D = 5.4\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 16. Test circuit for gate charge behavior)	-	19	26	nC
Q_{gs}	Gate-source charge			4		
Q_{gd}	Gate-drain charge			10		

1. $C_{oss\text{ eq.}}$ is defined as the constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 200\text{ V}$, $I_D = 2.7\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	15	-	ns
t_r	Rise time			15		
$t_{d(off)}$	Turn-off delay time	(see Figure 15. Test circuit for resistive load switching times and Figure 20. Switching time waveform)	-	30	-	ns
t_f	Fall time			12		
$t_{r(Voff)}$	Off-voltage rise time	$V_{DD} = 320\text{ V}$, $I_D = 5.4\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	12	-	ns
t_f	Fall time			10		
t_c	Crossover time	(see Figure 17. Test circuit for inductive load switching and diode recovery times)	-	20	-	ns

Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		5.4	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				21.6	
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 5.4 \text{ A}$, $V_{GS} = 0 \text{ V}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 5.4 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$, $V_{DD} = 50 \text{ V}$, $T_J = 150 \text{ }^\circ\text{C}$ (see Figure 17. Test circuit for inductive load switching and diode recovery times)	-	220		ns
Q_{rr}	Reverse recovery charge			990		nC
I_{RRM}	Reverse recovery current			9		A

1. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2. Pulse width is limited by safe operating area.

Table 7. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1 \text{ mA}$ (open drain)	30	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

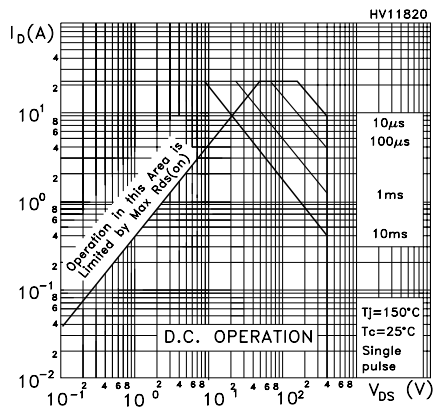
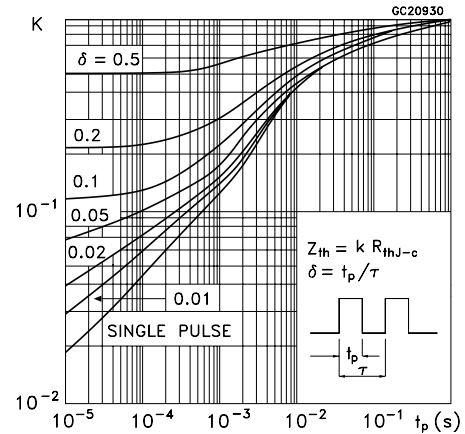
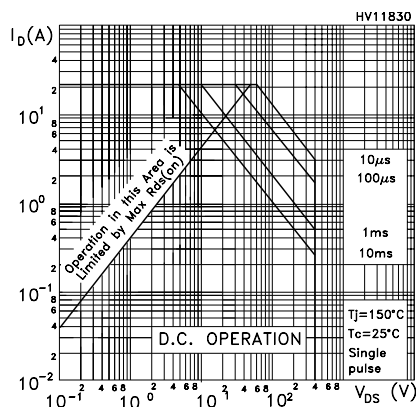
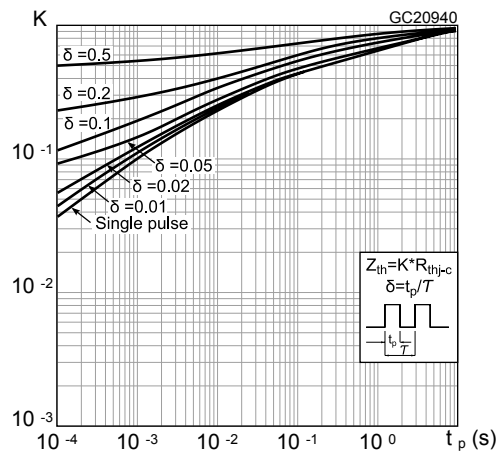
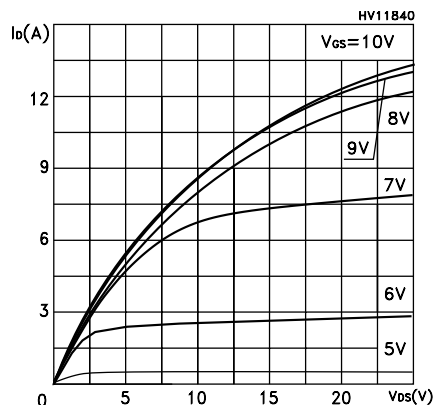
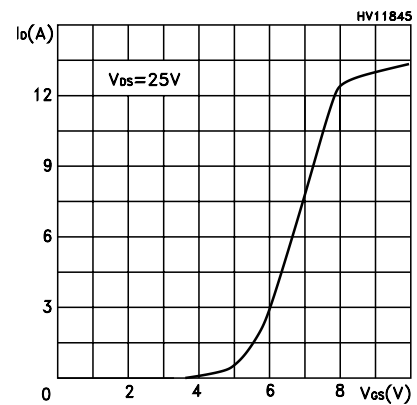
2.1 Electrical characteristics (curves)
Figure 1. Safe operating area for TO-220/DPAK

Figure 2. Thermal impedance for TO-220/DPAK

Figure 3. Safe operating area for TO-220FP

Figure 4. Thermal impedance for TO-220FP

Figure 5. Output characteristics

Figure 6. Transfer characteristics


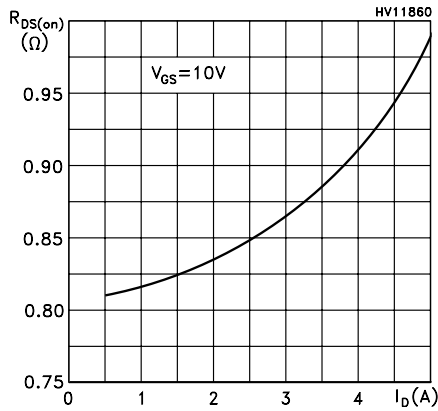
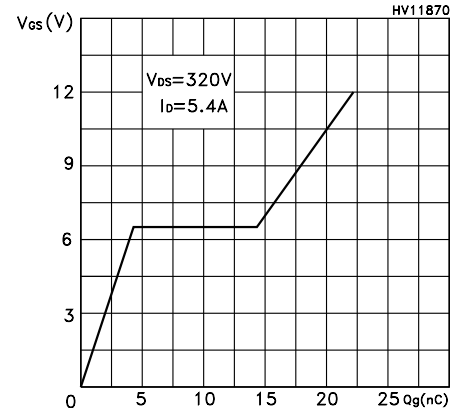
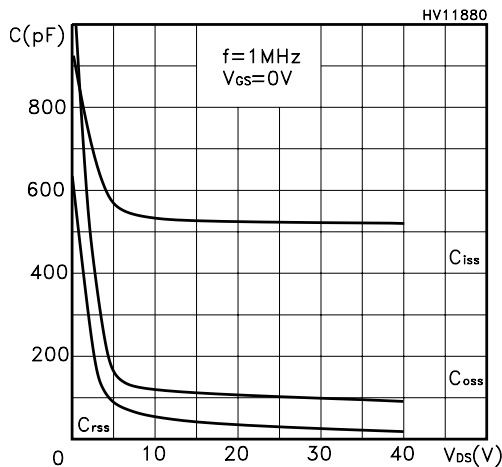
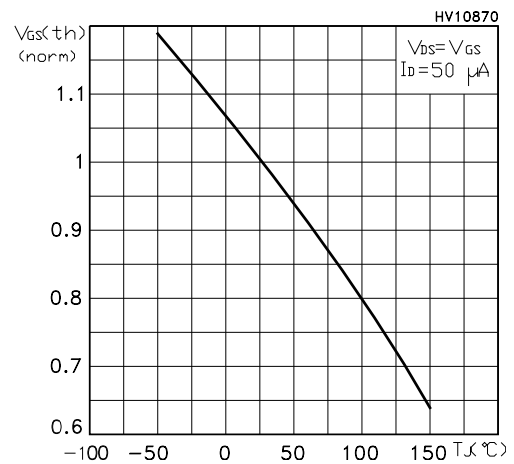
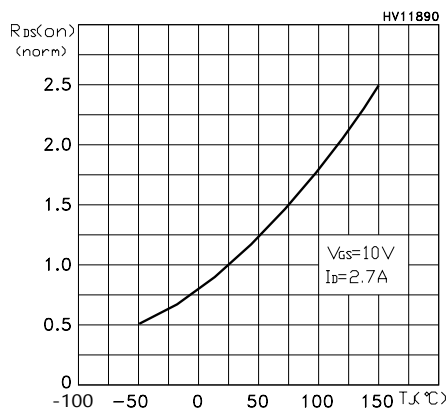
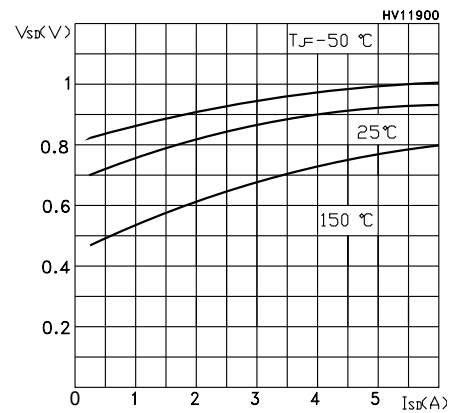
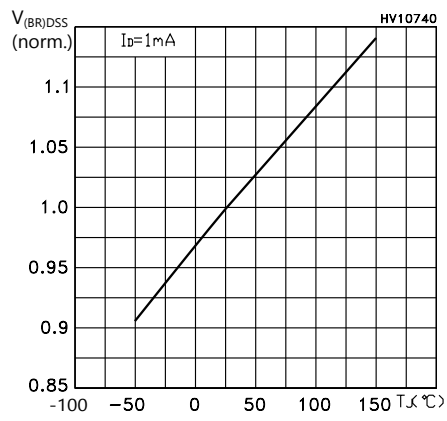
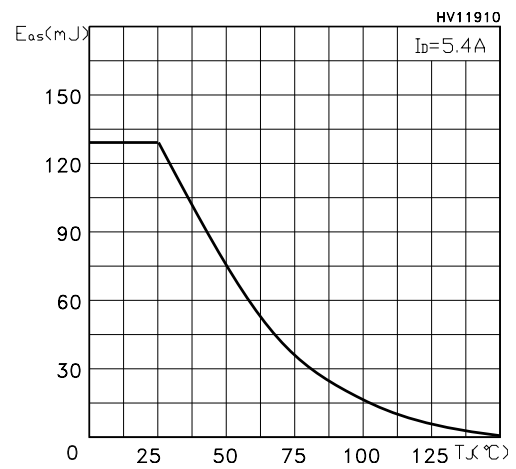
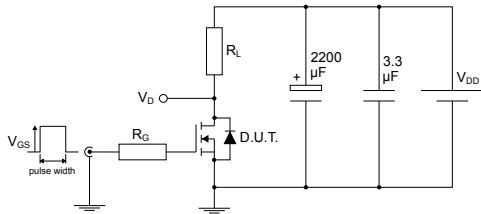
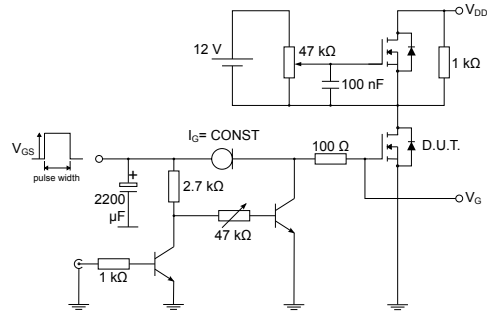
Figure 7. Static drain-source on-resistance

Figure 8. Gate charge vs gate-source voltage

Figure 9. Capacitance variations

Figure 10. Normalized gate threshold voltage vs temperature

Figure 11. Normalized on-resistance vs temperature

Figure 12. Source-drain diode forward characteristics


Figure 13. Normalized $V_{(BR)DSS}$ vs temperature

Figure 14. Maximum avalanche energy vs temperature


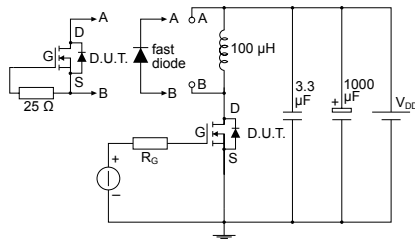
3 Test circuits

Figure 15. Test circuit for resistive load switching times


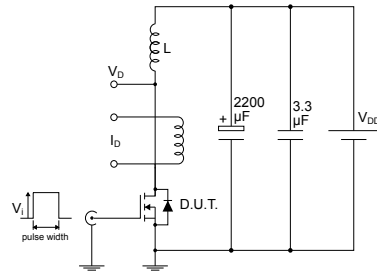
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Figure 16. Test circuit for gate charge behavior


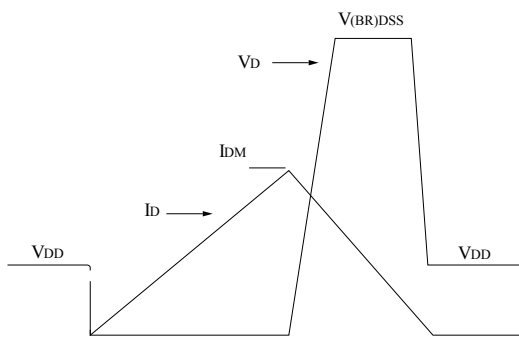
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Figure 17. Test circuit for inductive load switching and diode recovery times


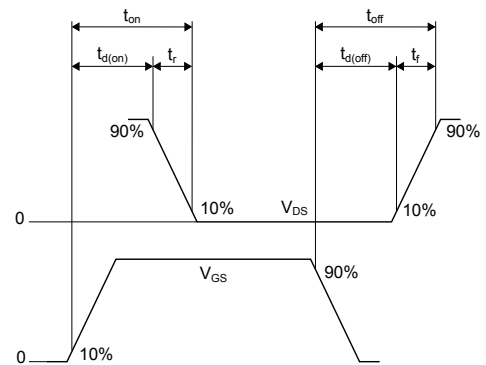
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Figure 18. Unclamped inductive load test circuit


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Figure 19. Unclamped inductive waveform


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Figure 20. Switching time waveform


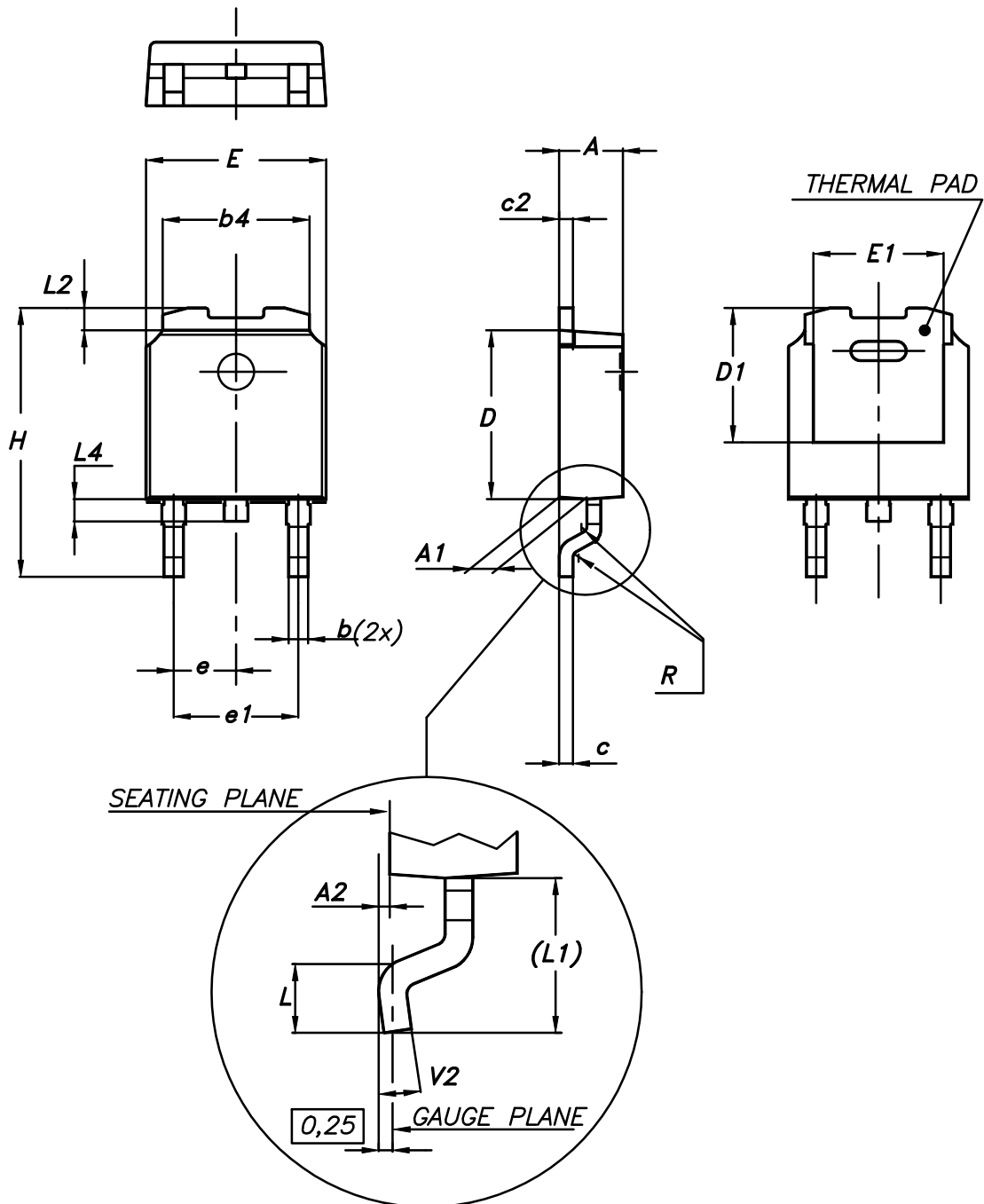
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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 DPAK (TO-252) type A package information

Figure 21. DPAK (TO-252) type A package outline



0068772_A_25

Table 8. DPAK (TO-252) type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	4.60	4.70	4.80
e	2.159	2.286	2.413
e1	4.445	4.572	4.699
H	9.35		10.10
L	1.00		1.50
(L1)	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

4.2 DPAK (TO-252) type E package information

Figure 22. DPAK (TO-252) type E package outline

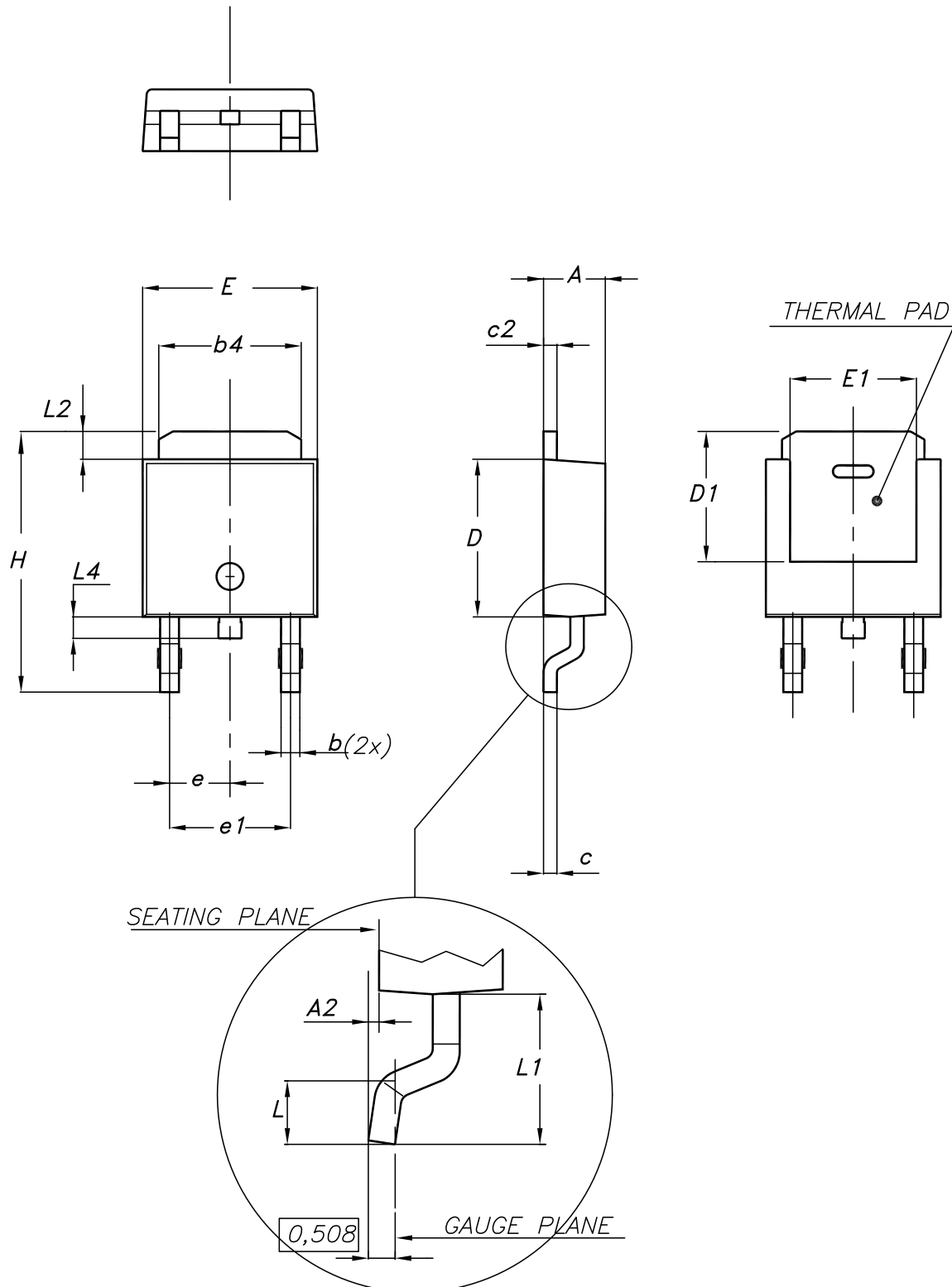
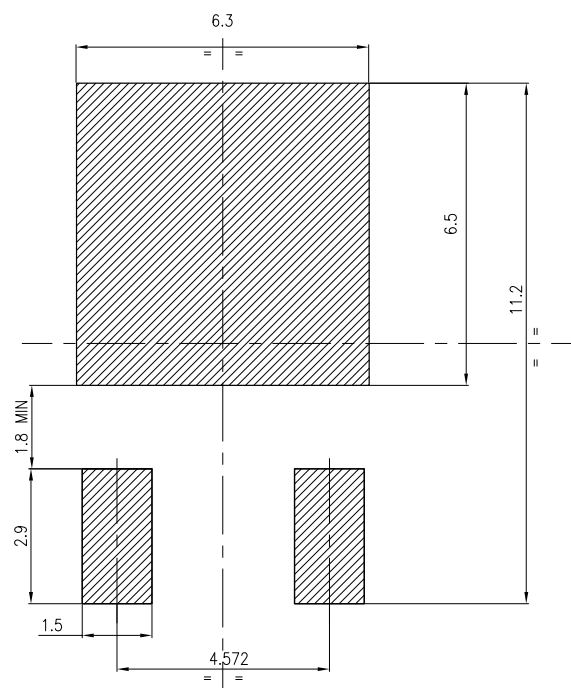


Table 9. DPAK (TO-252) type E mechanical data

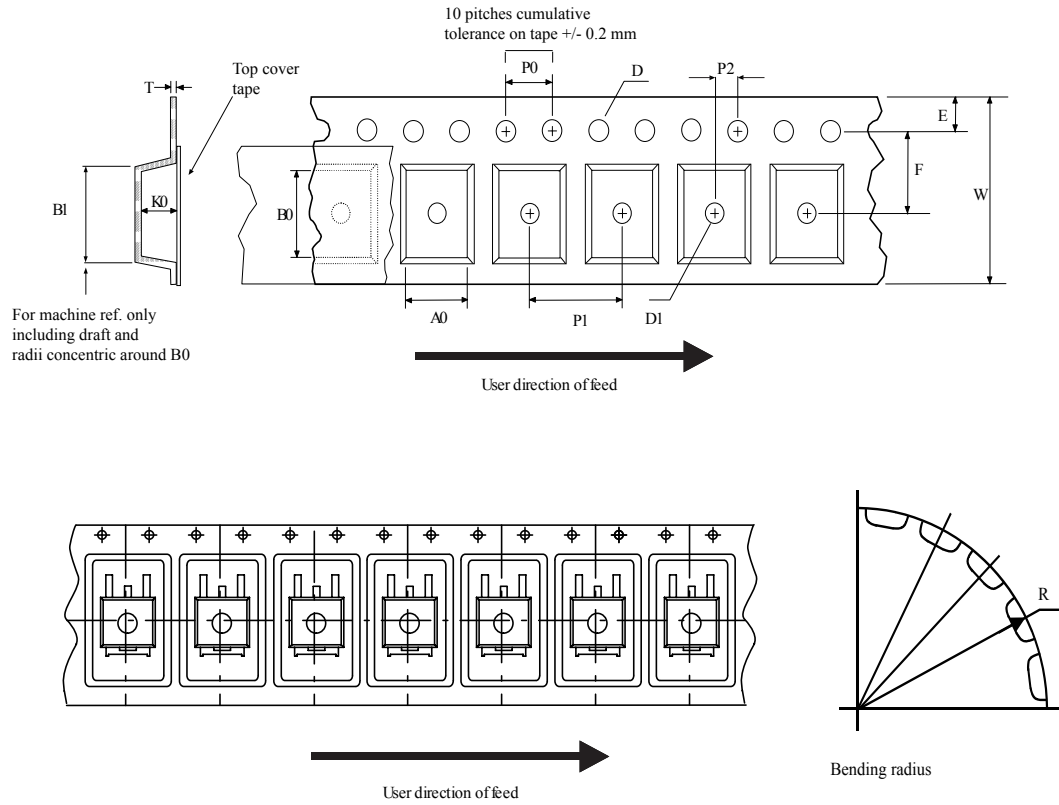
Dim.	mm		
	Min.	Typ.	Max.
A	2.18		2.39
A2			0.13
b	0.65		0.884
b4	4.95		5.46
c	0.46		0.61
c2	0.46		0.60
D	5.97		6.22
D1	5.21		
E	6.35		6.73
E1	4.32		
e		2.286	
e1		4.572	
H	9.94		10.34
L	1.50		1.78
L1		2.74	
L2	0.89		1.27
L4			1.02

Figure 23. DPAK (TO-252) recommended footprint (dimensions are in mm)


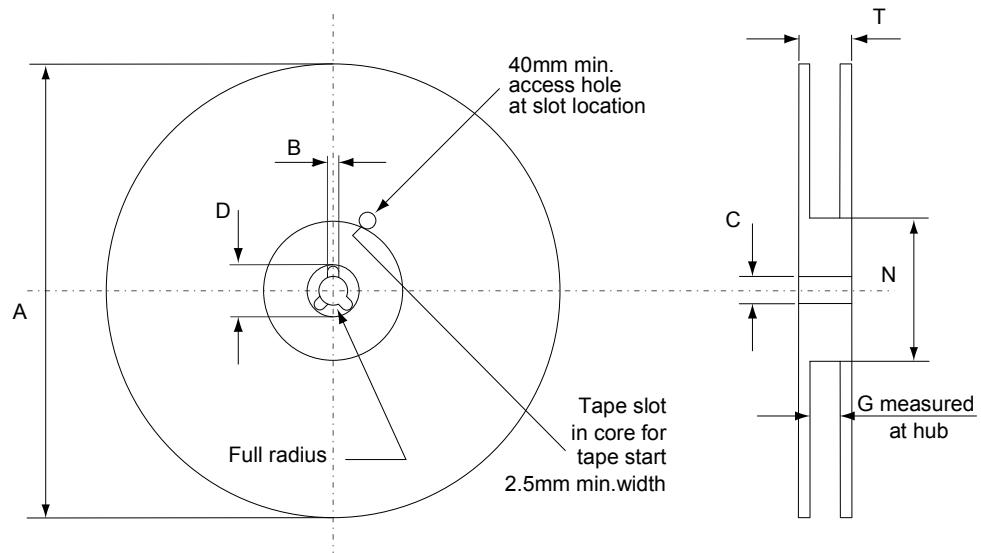
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4.3 DPAK (TO-252) packing information

Figure 24. DPAK (TO-252) tape outline



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Figure 25. DPAK (TO-252) reel outline


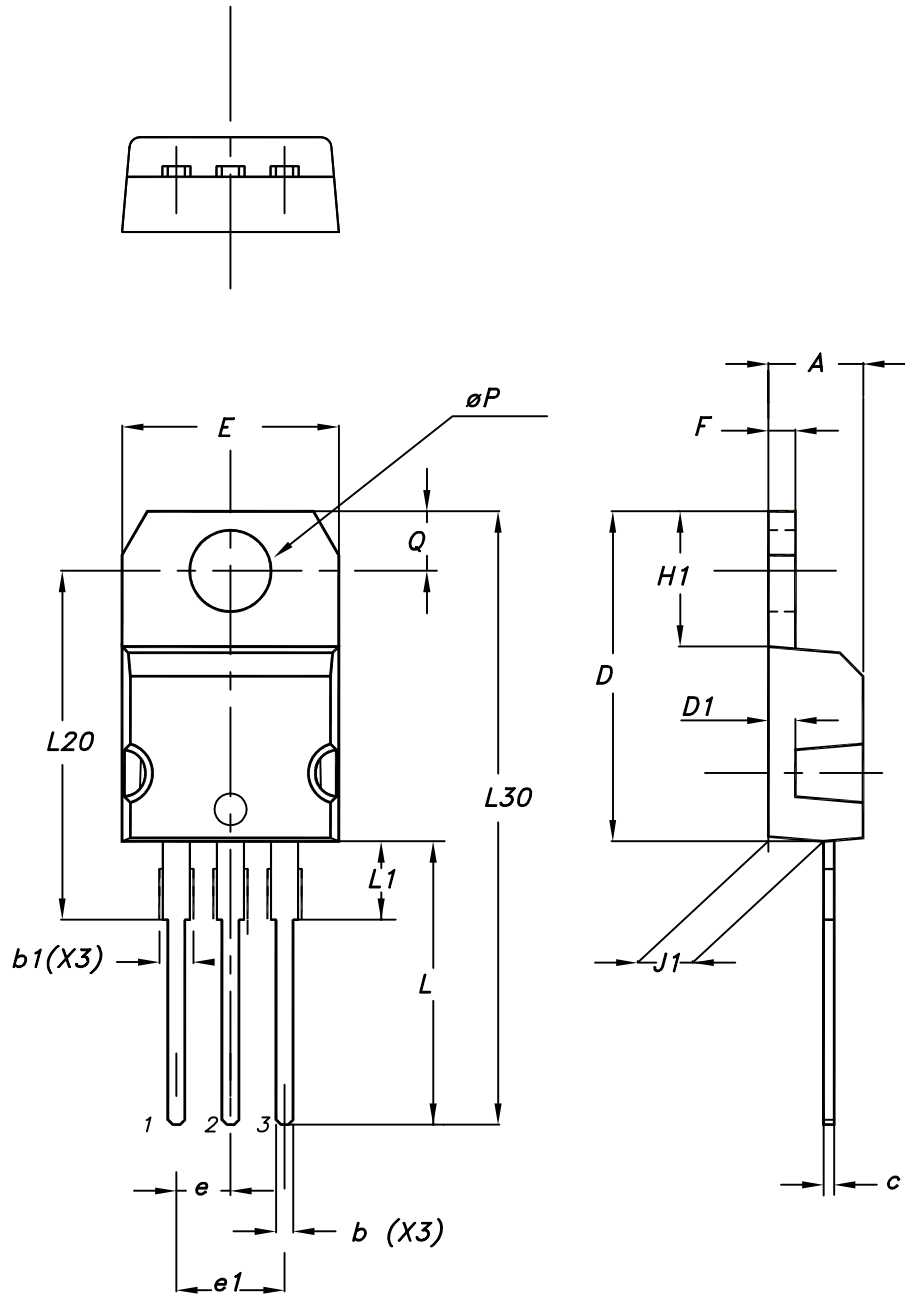
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Table 10. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

4.4 TO-220 type A package information

Figure 26. TO-220 type A package outline



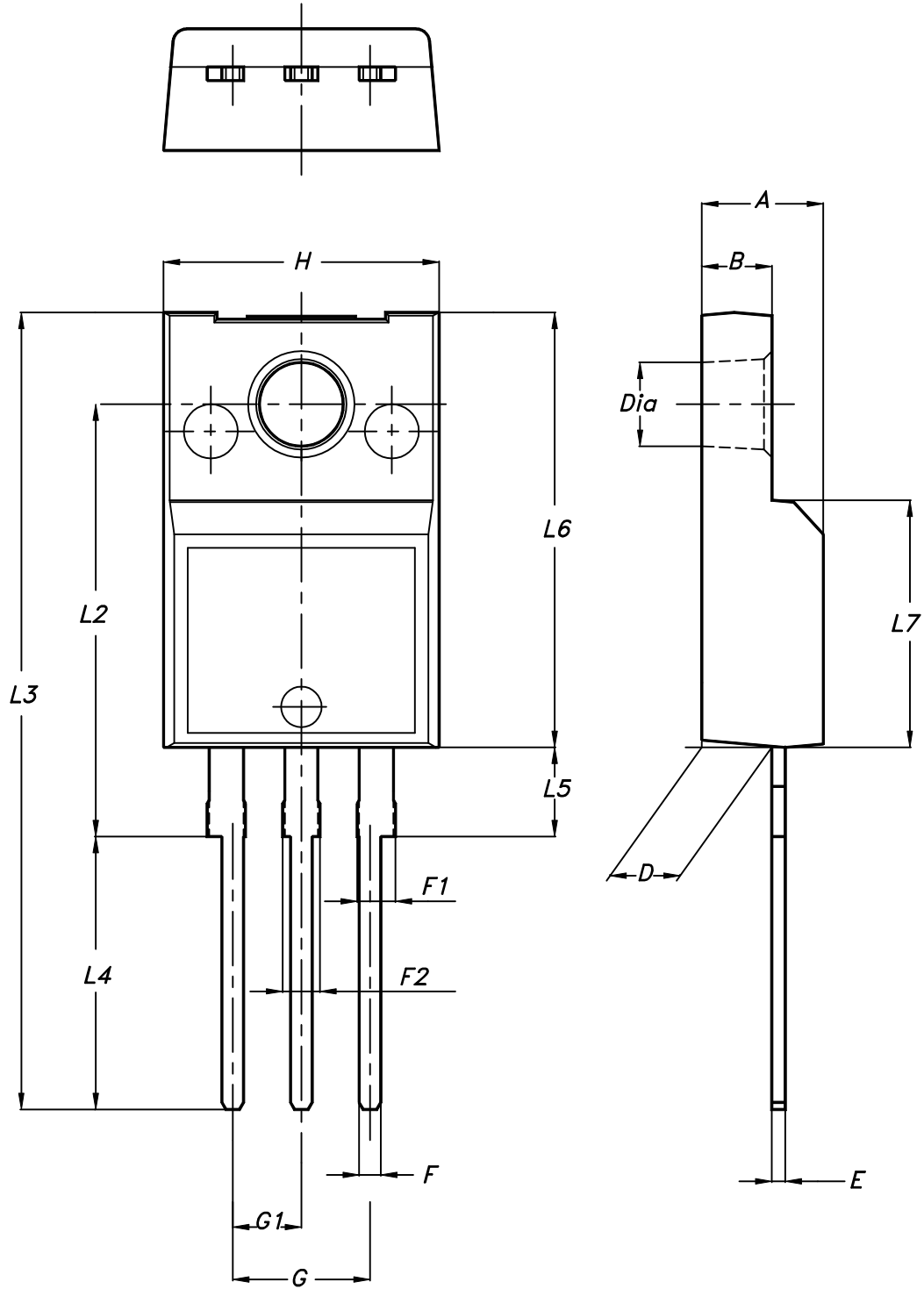
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Table 11. TO-220 type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95

4.5 TO-220FP package information

Figure 27. TO-220FP package outline



7012510_Rev_12_B

Table 12. TO-220FP package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Revision history

Table 13. Document revision history

Date	Version	Changes
02-Sep-2002	2	Document updated.
11-Jul-2018	3	Part number STD7NK40Z-1 was moved to a separate datasheet, and the document was updated accordingly. Updated title, features, applications and description on cover page. Updated Section 1 Electrical ratings , Section 2 Electrical characteristics , Section 3 Test circuits and Section 4 Package information . Minor text changes

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