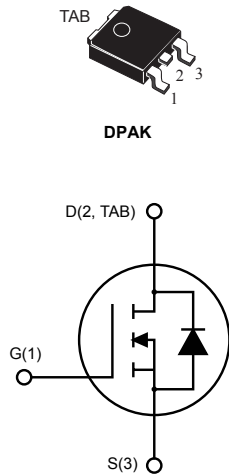



## Automotive-grade N-channel 250 V, 318 mΩ, 8 A, STripFET™ II Power MOSFET in a DPAK package



AM01475v1\_noZen

### Features

Order code	$V_{DS}$	$R_{DS(on)max.}$	$I_D$
STD8NF25	250 V	420 mΩ	8 A

- AEC-Q101 qualified 
- 100% avalanche tested
- 175 °C maximum junction temperature

### Applications

- Switching applications

### Description

This Power MOSFET series has been developed using STMicroelectronics' unique STripFET™ process, which is specifically designed to minimize input capacitance and gate charge. This renders the device suitable for use as primary switch in advanced high-efficiency isolated DC-DC converters for telecom and computer applications, and applications with low gate charge driving requirements.

#### Product status link

[STD8NF25](#)

#### Product summary

<b>Order code</b>	STD8NF25
<b>Marking</b>	8NF25
<b>Package</b>	DPAK
<b>Packing</b>	Tape and reel

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	250	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	8	A
	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	6	A
$I_{DM}^{(1)}$	Drain current (pulsed)	32	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	72	W
$T_J$	Operating junction temperature range	-55 to 175	$^\circ\text{C}$
$T_{stg}$	Storage temperature range		

1. Pulse width is limited by safe operating area.

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	2.08	$^\circ\text{C/W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	50	$^\circ\text{C/W}$

1. When mounted on an 1-inch<sup>2</sup> FR-4, 2 Oz copper board

**Table 3. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or non-repetitive (pulse width limited by $T_{Jmax}$ )	8	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	110	mJ

## 2 Electrical characteristics

( $T_{CASE} = 25\text{ °C}$  unless otherwise specified)

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$ , $V_{GS} = 0\text{ V}$	250			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 250\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ , $V_{DS} = 250\text{ V}$ , $T_C = 125\text{ °C}$ <sup>(1)</sup>			50	$\mu\text{A}$
$I_{GSS}$	Gate body leakage current	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	2		4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 8\text{ A}$		318	420	m $\Omega$

1. Defined by design, not subject to production test.

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$	-	500	-	$\mu\text{F}$
$C_{oss}$	Output capacitance			90		
$C_{rss}$	Reverse transfer capacitance			15		
$Q_g$	Total gate charge	$V_{DD} = 200\text{ V}$ , $I_D = 8\text{ A}$ , $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 13. Test circuit for gate charge behavior)	-	16	-	nC
$Q_{gs}$	Gate-source charge			3.5		
$Q_{gd}$	Gate-drain charge			8		

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 125\text{ V}$ , $I_D = 4\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$	-	13	-	ns
$t_r$	Rise time			10		
$t_{d(off)}$	Turn-off delay time	(see Figure 12. Test circuit for resistive load switching times and Figure 17. Switching time waveform)	-	26	-	ns
$t_f$	Fall time			6		

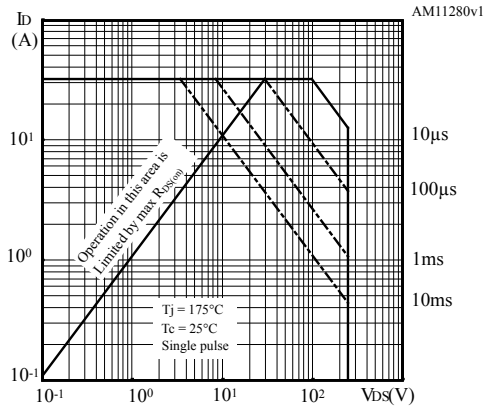
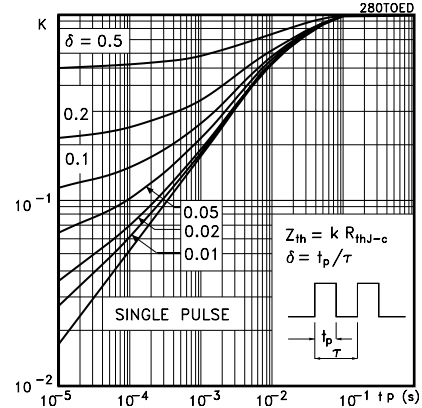
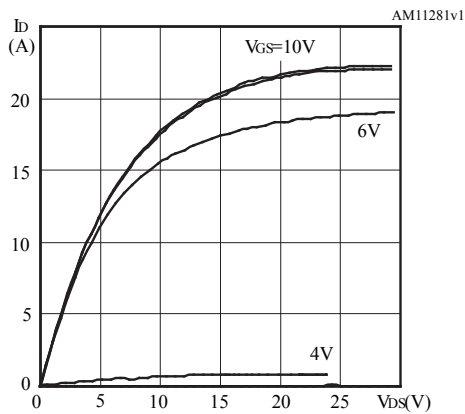
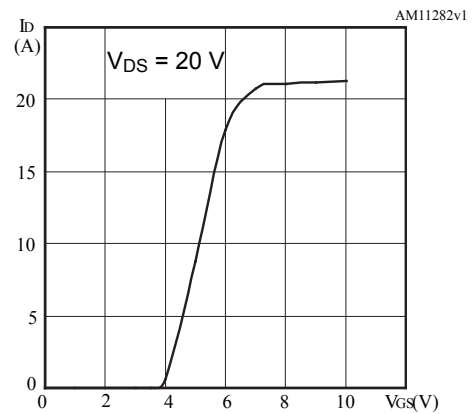
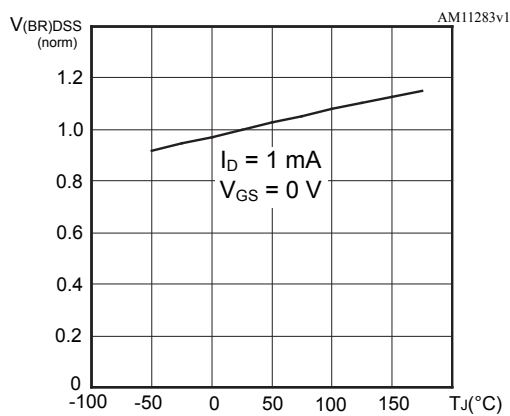
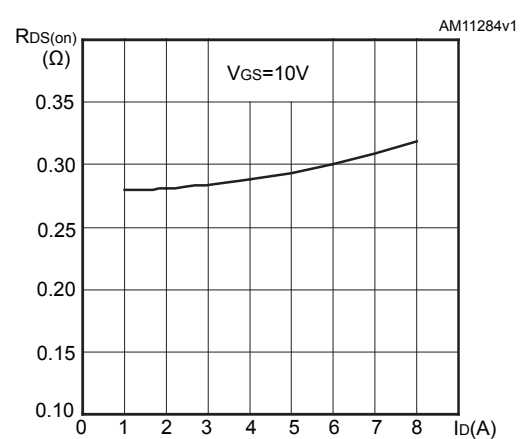
**Table 7. Source drain diode**

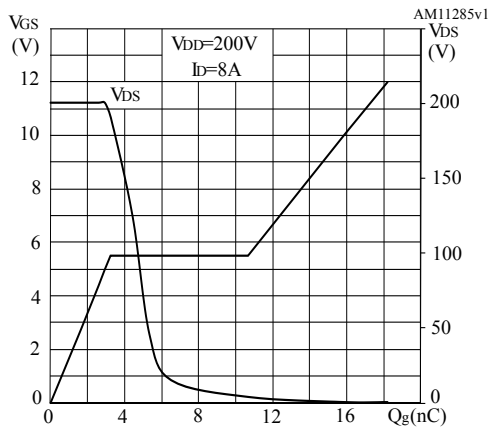
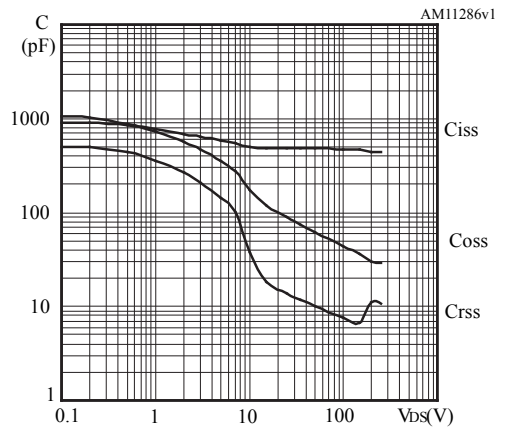
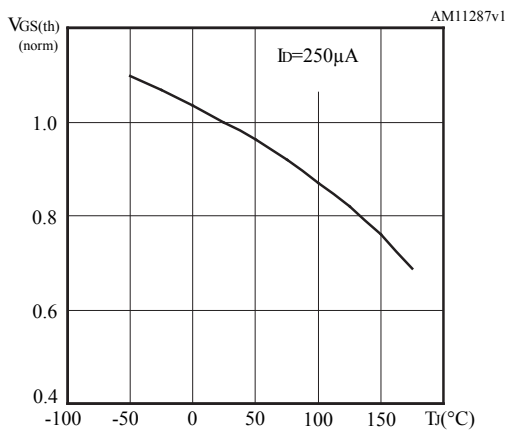
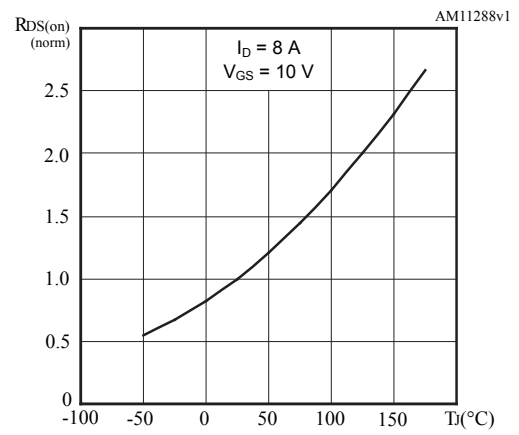
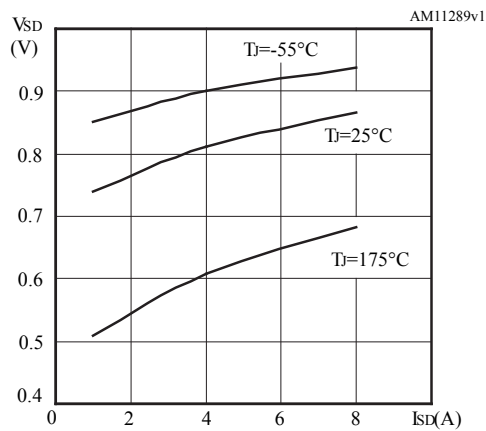
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		8	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				32	
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 8\text{ A}$ , $V_{GS} = 0\text{ V}$	-		1.5	V

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{rr}$	Reverse recovery time	$I_{SD} = 8 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ , $V_{DD} = 50 \text{ V}$ (see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	115		ns
$Q_{rr}$	Reverse recovery charge			0.47		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current			8.5		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 8 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ , $V_{DD} = 50 \text{ V}$ , $T_j = 150 \text{ }^\circ\text{C}$ (see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	130		ns
$Q_{rr}$	Reverse recovery charge			0.58		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current			9.5		A

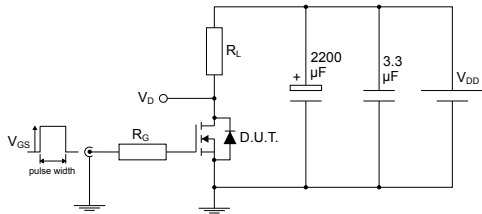
1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)

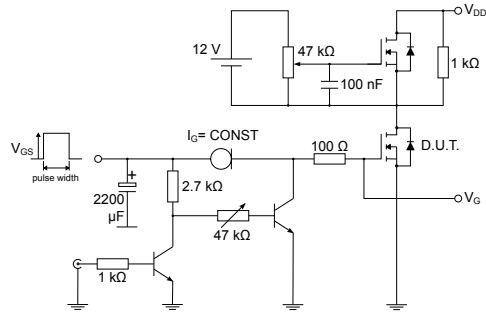
**Figure 1. Safe operating area**

**Figure 2. Thermal impedance**

**Figure 3. Output characteristics**

**Figure 4. Transfer characteristics**

**Figure 5. Normalized V(BR)DSS vs temperature**

**Figure 6. Static drain-source on-resistance**


**Figure 7. Gate charge vs gate-source voltage**

**Figure 8. Capacitance variations**

**Figure 9. Normalized gate threshold voltage vs temperature**

**Figure 10. Normalized on-resistance vs temperature**

**Figure 11. Source-drain diode forward characteristics**


### 3 Test circuits

**Figure 12. Test circuit for resistive load switching times**


AM01468v1

**Figure 13. Test circuit for gate charge behavior**


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**Figure 14. Test circuit for inductive load switching and diode recovery times**

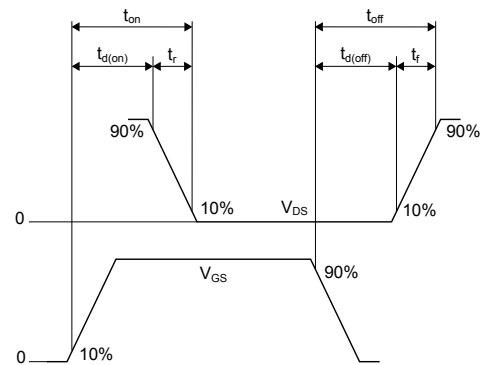

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**Figure 15. Unclamped inductive load test circuit**


AM01471v1

**Figure 16. Unclamped inductive waveform**


AM01472v1

**Figure 17. Switching time waveform**


AM01473v1

## 4 Package information

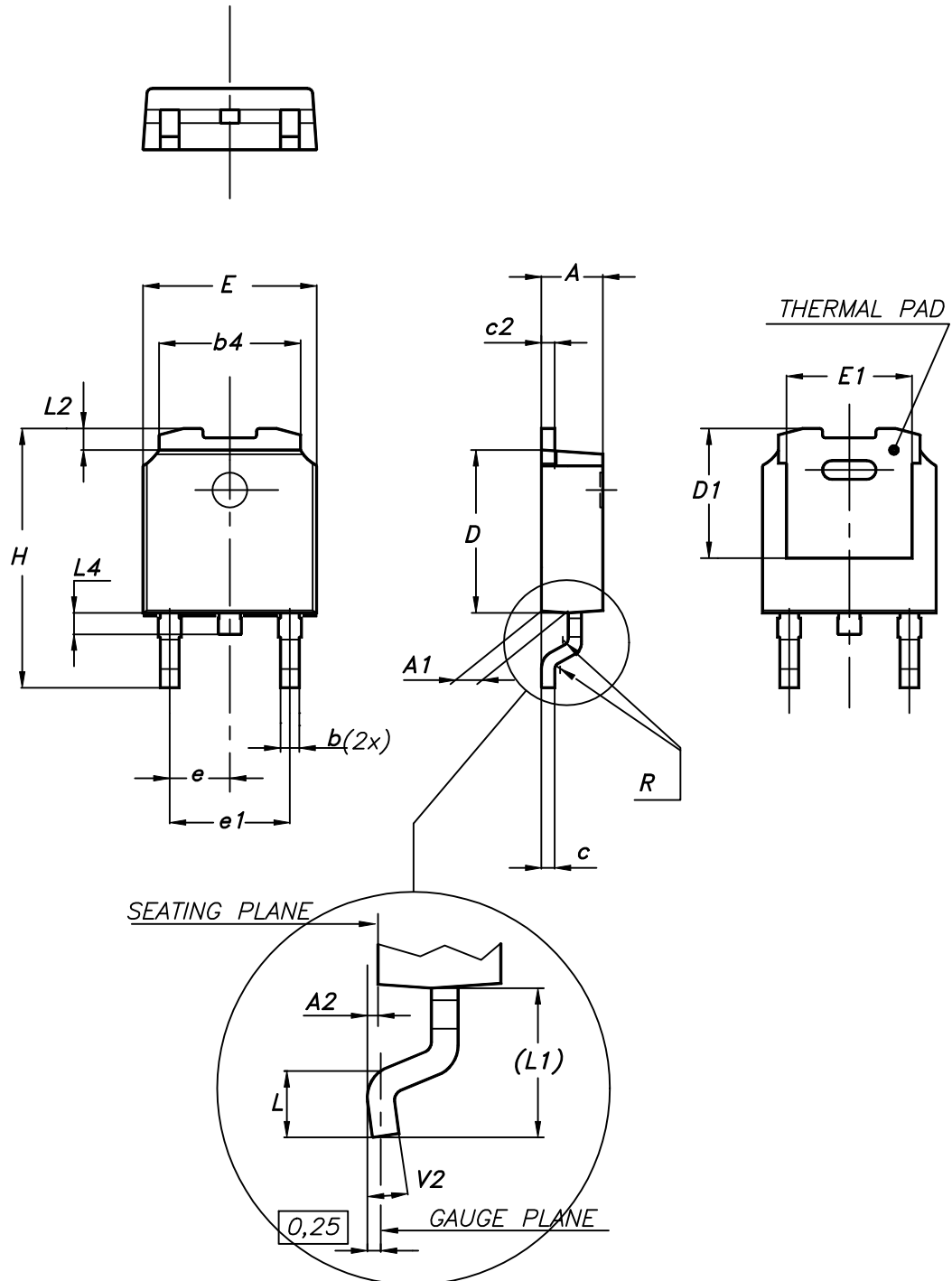
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### 4.1 DPAK (TO-252) type A2 package information

Figure 18. DPAK (TO-252) type A2 package outline

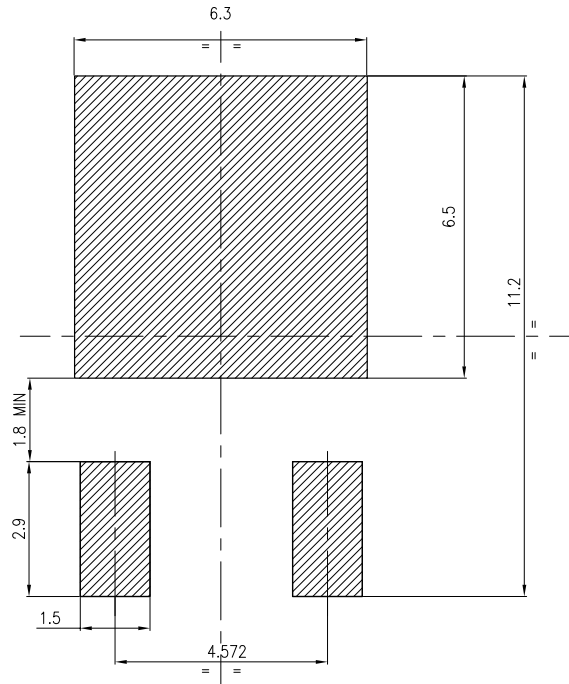


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**Table 8. DPAK (TO-252) type A2 mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	5.10	5.20	5.30
e	2.159	2.286	2.413
e1	4.445	4.572	4.699
H	9.35		10.10
L	1.00		1.50
L1	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

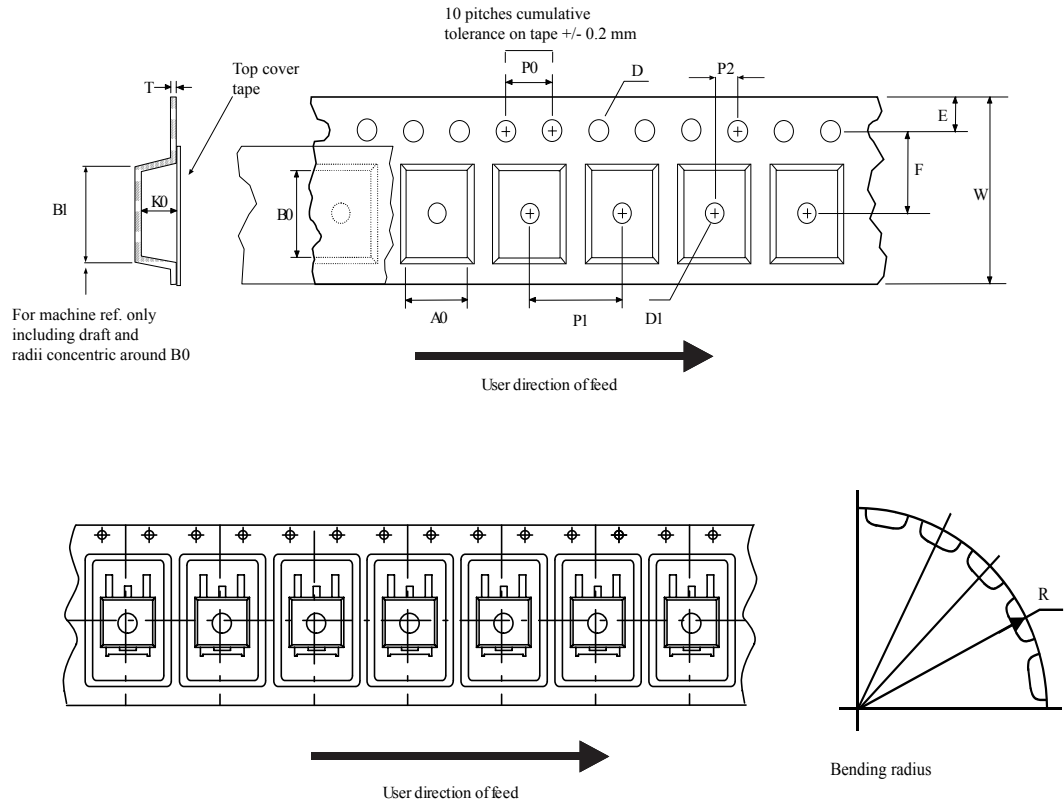
Figure 19. DPAK (TO-252) recommended footprint (dimensions are in mm)



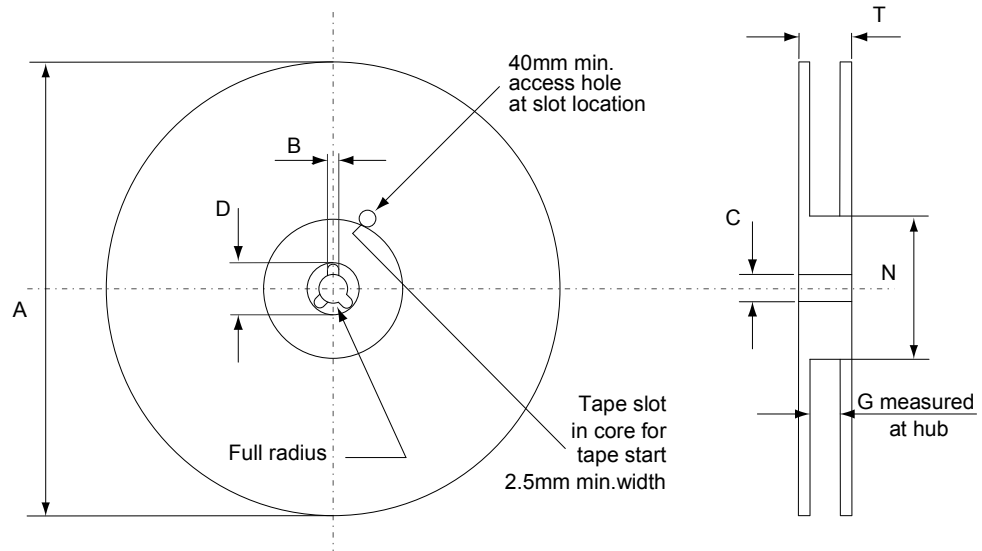
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## 4.2 DPAK (TO-252) packing information

**Figure 20. DPAK (TO-252) tape outline**



AM08852v1

**Figure 21. DPAK (TO-252) reel outline**


AM06038v1

**Table 9. DPAK (TO-252) tape and reel mechanical data**

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

## Revision history

**Table 10. Document revision history**

Date	Version	Changes
26-Apr-2012	1	First release.
03-Jul-2018	2	Removed maturity status indication from cover page. Updated title, features and description on cover page. Updated <a href="#">Section 4.1 DPAK (TO-252) type A2 package information</a> . Minor text changes

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[SSM6P69NU,LF](#) [DMP22D4UFO-7B](#)