# STD8NM50N, STP8NM50N

N-channel 500 V, 0.73 Ω typ., 5 A, MDmesh™ II Power MOSFETs in DPAK and TO-220 packages
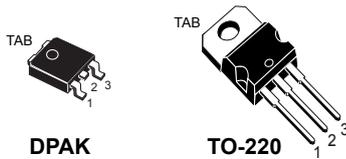
DPAK

TO-220
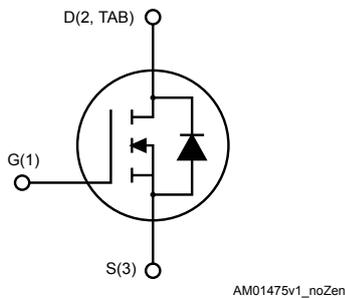
Features

Order codes	V$_{DS}$ @ T$_{Jmax}$	R$_{DS(on)}$ max.	I$_D$
STD8NM50N	550 V	0.79 Ω	5 A
STP8NM50N			

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Applications

- Switching applications

Description

These devices are N-channel Power MOSFETs developed using the second generation of MDmesh™ technology. These revolutionary Power MOSFETs associate a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. They are therefore suitable for the most demanding high-efficiency converters.

Product status links
STD8NM50N
STP8NM50N

Product summary	
Order code	STD8NM50N
Marking	8NM50N
Package	DPAK
Packing	Tape and reel
Order code	STP8NM50N
Marking	8NM50N
Package	TO-220
Packing	Tube

DS6808 - Rev 7 - September 2018
For further information contact your local STMicroelectronics sales office.

www.st.com

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	500	
V_{GS}	Gate-source voltage	±25	V
I_D	Drain current (continuous) at T_{case} = 25 °C	5	A
	Drain current (continuous) at T_{case} = 100 °C	3	
I_{DM}[1]	Drain current (pulsed)	20	A
P_{TOT}	Total dissipation at T_{case} = 25 °C	45	W
dv/dt[2]	Peak diode recovery voltage slope	15	V/ns
T_{stg}	Storage temperature range	-55 to 150	°C
T_j	Operating junction temperature range		

1. *Limited by maximum junction temperature*

2. *$I_{SD} ≤ 5 A$, di/dt ≤ 400 A/µs, $V_{DS(Peak)} ≤ V_{(BR)DSS}$, V_{DD} = 80% $V_{(BR)DSS}$*

Table 2. Thermal data

Symbol	Parameter	Value		Unit
		DPAK	TO-220	
$R_{thj-case}$	Thermal resistance junction-case	2.78		°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient		62.5	°C/W
$R_{thj-pcb}$[1]	Thermal resistance junction-pcb	50		°C/W

1. *When mounted on an 1 inch² FR-4, 2 Oz copper board*

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or non-repetitive (pulse width limited by T_{Jmax})	2	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	140	mJ

2 Electrical characteristics

(T_{case} = 25 °C unless otherwise specified)

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	500			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 500 V			1	µA
		V_{GS} = 0 V, V_{DS} = 500 V, T_{case} = 125 °C [1]			100	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 2.5 A		0.73	0.79	Ω

1. *Defined by design, not subject to production test.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 50 V, f = 1 MHz, V_{GS} = 0 V	-	364	-	pF
C_{oss}	Output capacitance		-	33	-	
C_{rss}	Reverse transfer capacitance		-	1.2	-	
$C_{oss\ eq.}$ [1]	Equivalent output capacitance	V_{DS} = 0 to 400 V, V_{GS} = 0 V	-	147.5	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	-	5.4	-	Ω
Q_g	Total gate charge	V_{DD} = 400 V, I_D = 5 A,	-	14	-	nC
Q_{gs}	Gate-source charge	V_{GS} = 0 to 10 V	-	3	-	
Q_{gd}	Gate-drain charge	(see Figure 15. Test circuit for gate charge behavior)	-	7	-	

1. *$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 250 V, I_D = 2.5 A,	-	7	-	ns
t_r	Rise time	R_G = 4.7 Ω, V_{GS} = 10 V	-	4.4	-	
$t_{d(off)}$	Turn-off delay time	(see Figure 14. Test circuit for resistive load switching times and Figure 19. Switching time waveform)	-	25	-	
t_f	Fall time		-	9	-	

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		5	A
I_{SDM}[1]	Source-drain current (pulsed)		-		20	A
V_{SD}[2]	Forward on voltage	V_{GS} = 0 V, I_{SD} = 5 A	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 5 A, di/dt = 100 A/µs,	-	187		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 60 V	-	1.3		µC
I_{RRM}	Reverse recovery current	(see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	14		A
t_{rr}	Reverse recovery time	I_{SD} = 5 A, di/dt = 100 A/µs,	-	224		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 60 V, T_j = 150 °C	-	1.5		µC
I_{RRM}	Reverse recovery current	(see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	13		A

1. Pulse width is limited by safe operating area.

2. Pulse test: pulse duration = 300 µs, duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area for DPAK
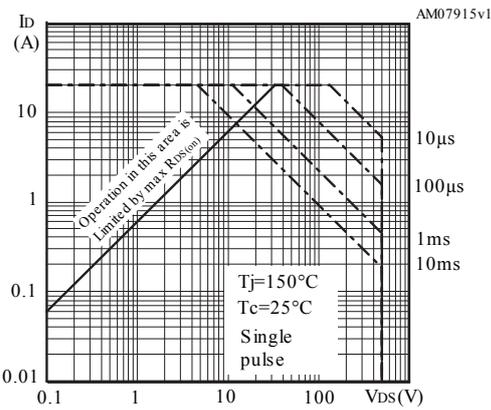
Figure 2. Thermal impedance for DPAK

$$Z_{th} = KR_{thJ-c}$$
$$\delta = t_p / \tau$$
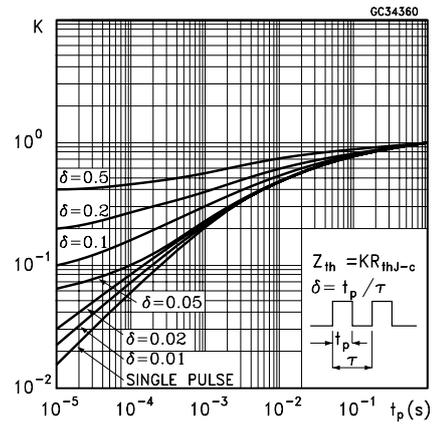
Figure 3. Safe operating area for TO-220
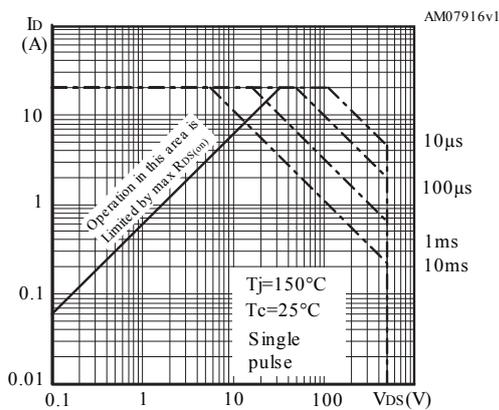
Figure 4. Thermal impedance for TO-220

$$Z_{th} = k \, R_{thJ-c}$$
$$\delta = t_p / \tau$$
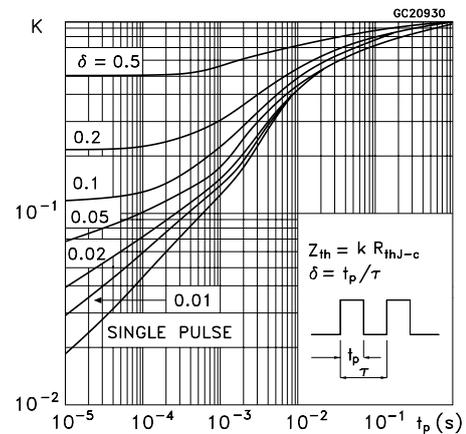
Figure 5. Output characteristics
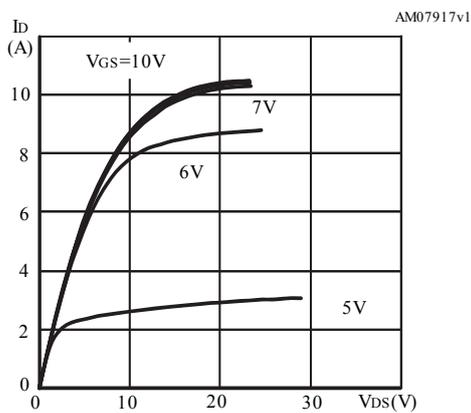

Figure 6. Transfer characteristics
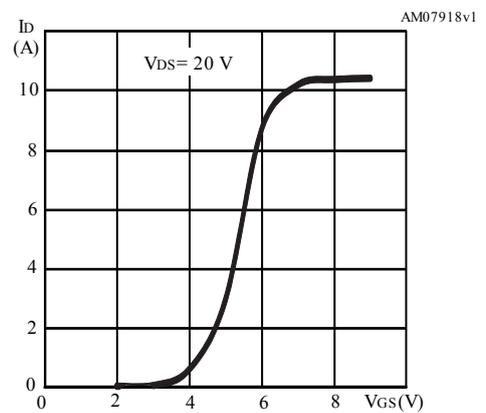
Figure 7. Static drain-source on-resistance

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$R_{DS(on)}$ (Ω), V_{GS}=10V vs I_D(A)
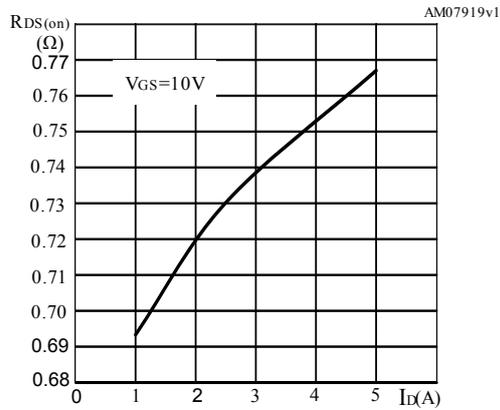
Figure 8. Gate charge vs gate-source voltage

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V_{GS} (V), V_{DS} (V), V_{DD}=400 V, I_D=5 A vs Q_g(nC)
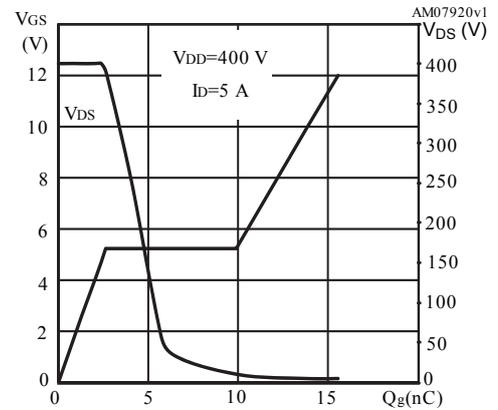
Figure 9. Capacitance variations

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C (pF), Ciss, Coss, Crss vs V_{DS}(V)
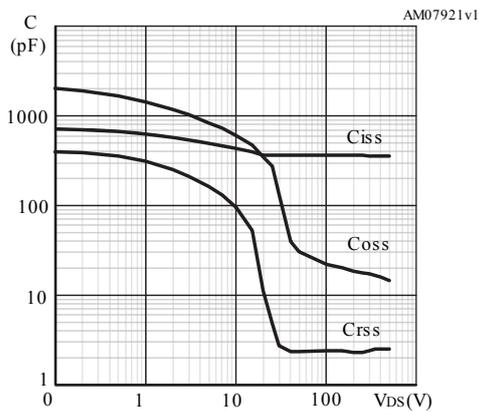
Figure 10. Output capacitance stored energy

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E (μJ) vs V_{DS}(V)
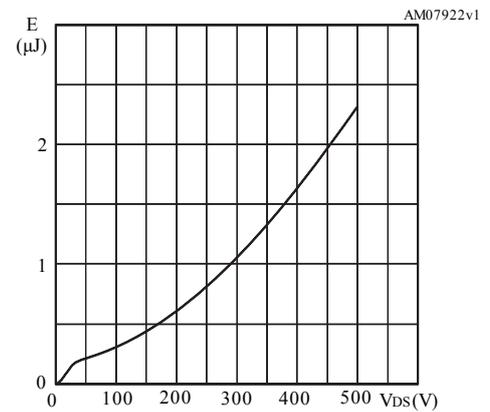
Figure 11. Normalized gate threshold voltage vs temperature

AM07923v1

$V_{GS(th)}$ (norm), I_D = 250 μA vs T_J(°C)
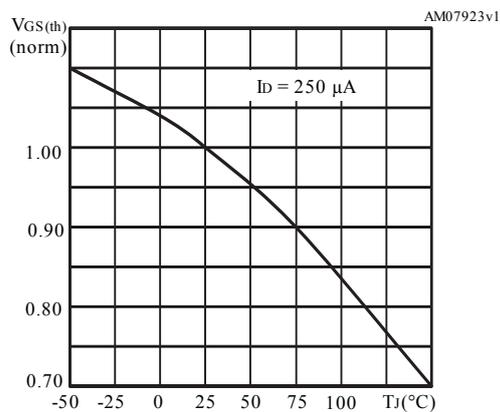
Figure 12. Normalized on-resistance vs temperature

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$R_{DS(on)}$ (norm), I_D = 2.5 A vs T_J(°C)
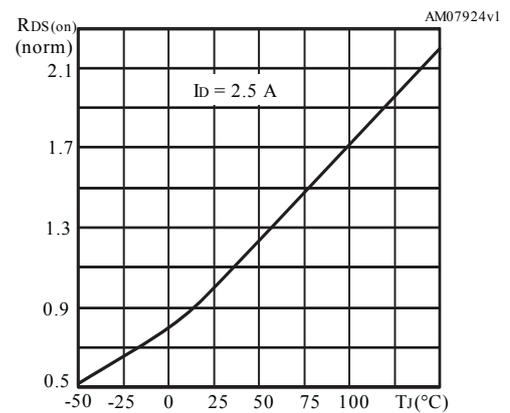
Figure 13. Normalized V$_{(BR)DSS}$ vs temperature
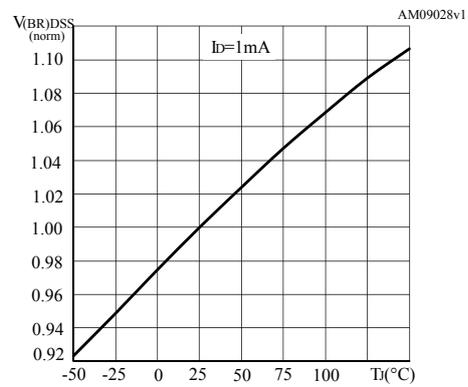
3 Test circuits

**Figure 14. Test circuit for resistive load switching times**
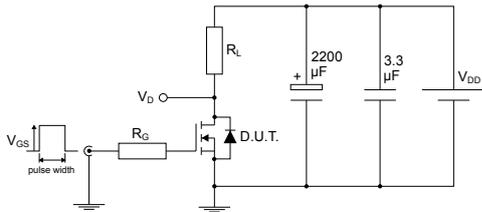
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**Figure 15. Test circuit for gate charge behavior**
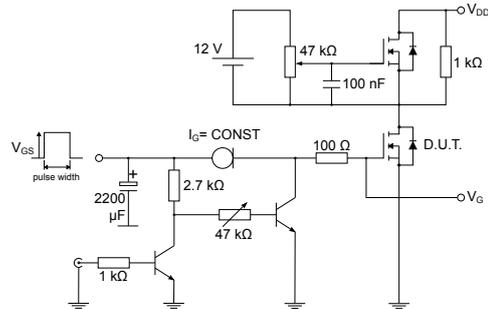
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Figure 16. Test circuit for inductive load switching and diode recovery times
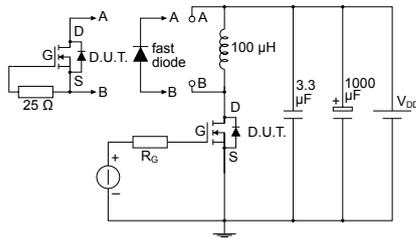
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Figure 17. Unclamped inductive load test circuit
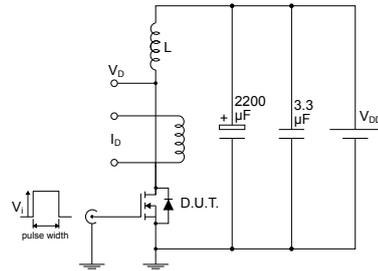
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Figure 18. Unclamped inductive waveform
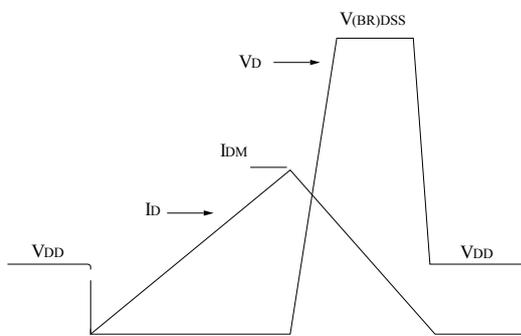
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Figure 19. Switching time waveform
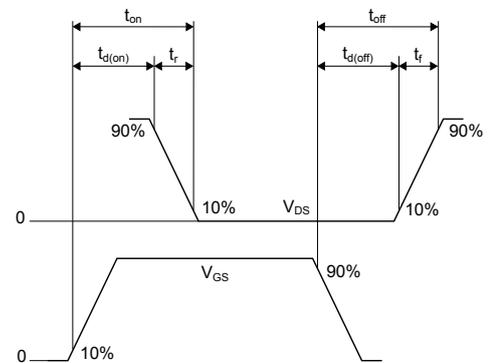
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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 DPAK (TO-252) type A package information

Figure 20. **DPAK (TO-252) type A package outline**
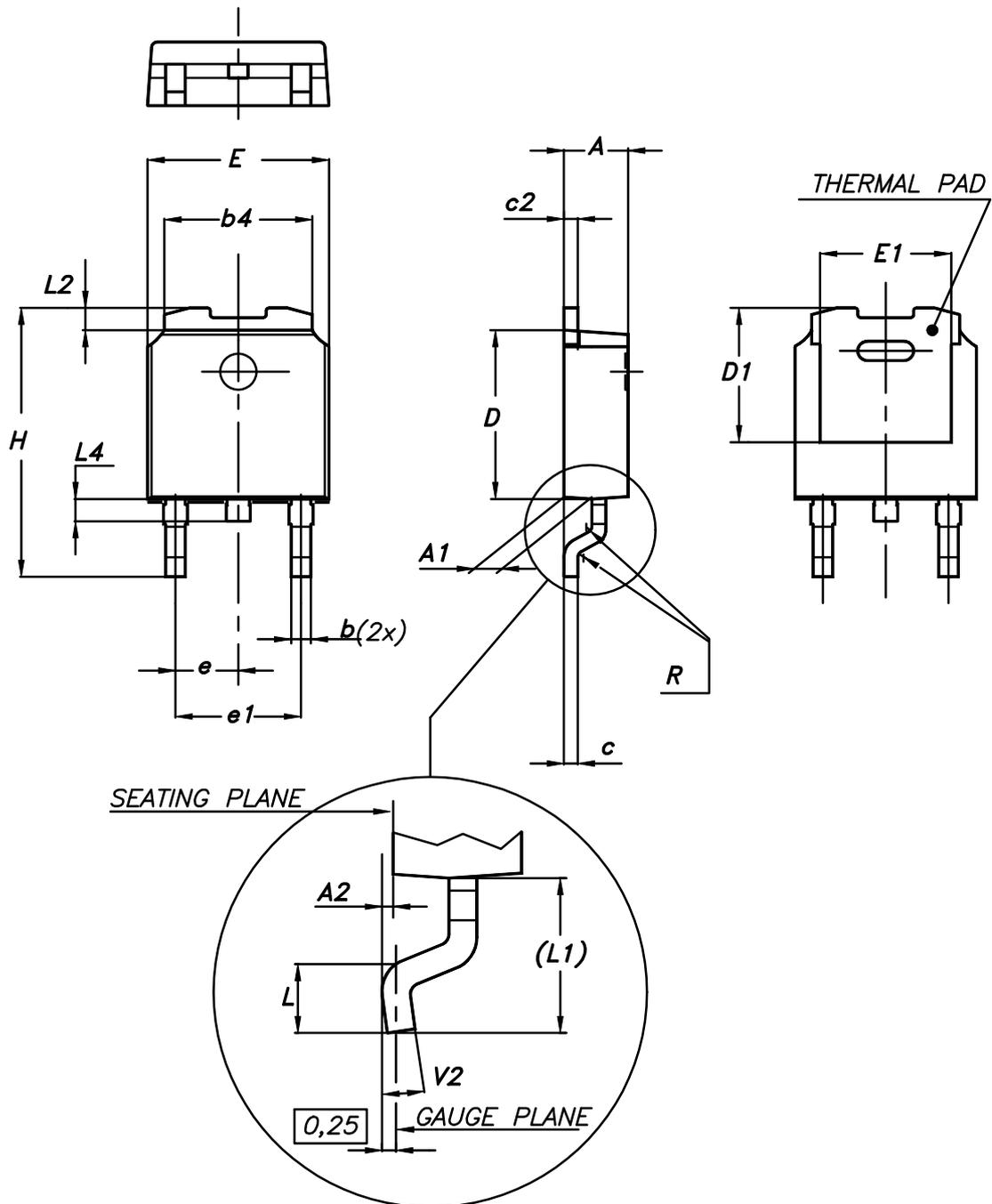
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Table 8. **DPAK (TO-252) type A mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	4.60	4.70	4.80
e	2.159	2.286	2.413
e1	4.445	4.572	4.699
H	9.35		10.10
L	1.00		1.50
(L1)	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

4.2 DPAK (TO-252) type C package information

Figure 21. DPAK (TO-252) type C package outline
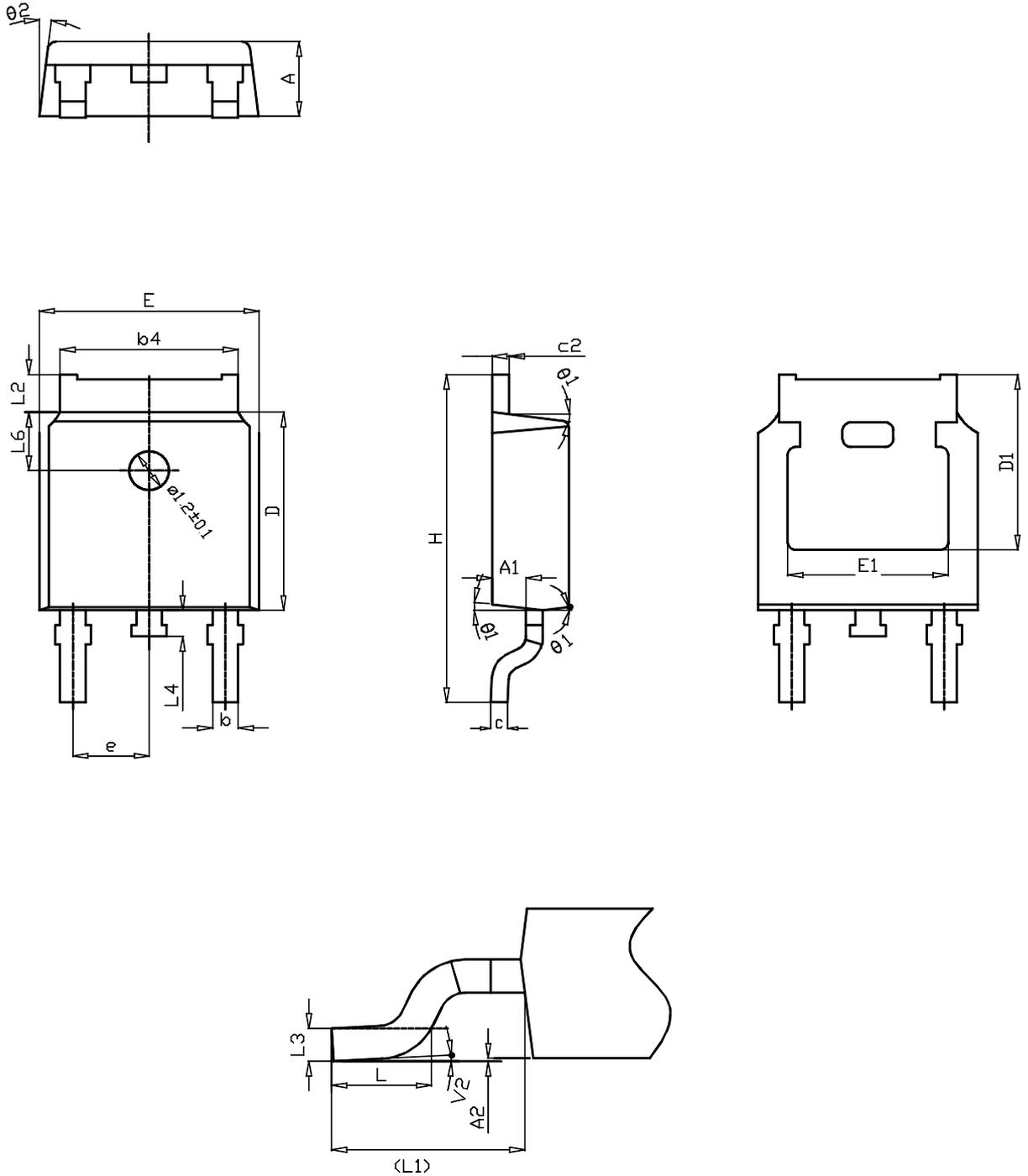
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Table 9. DPAK (TO-252) type C mechanical data

| Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.38
A1	0.90	1.01	1.10
A2	0.00		0.10
b	0.72		0.85
b4	5.13	5.33	5.46
c	0.47		0.60
c2	0.47		0.60
D	6.00	6.10	6.20
D1	5.25		
E	6.50	6.60	6.70
E1	4.70		
e	2.186	2.286	2.386
H	9.80	10.10	10.40
L	1.40	1.50	1.70
L1	2.90 REF		
L2	0.90		1.25
L3	0.51 BSC		
L4	0.60	0.80	1.00
L6	1.80 BSC		
θ1	5°	7°	9°
θ2	5°	7°	9°
V2	0°		8°

**Figure 22. DPAK (TO-252) recommended footprint (dimensions are in mm)**
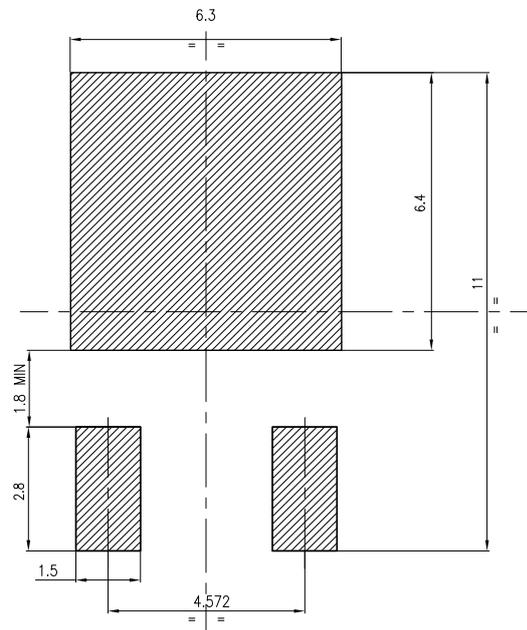
FP_0068772_25_C

4.3 DPAK (TO-252) packing information

Figure 23. DPAK (TO-252) tape outline
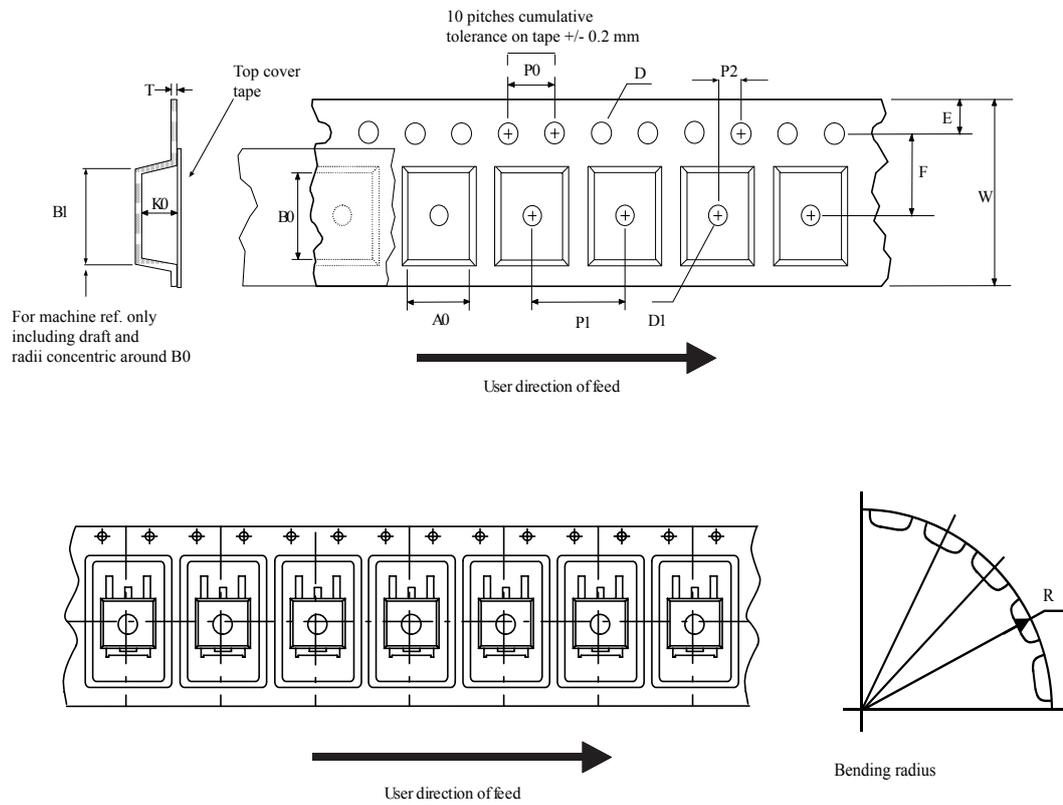

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Figure 24. **DPAK (TO-252) reel outline**
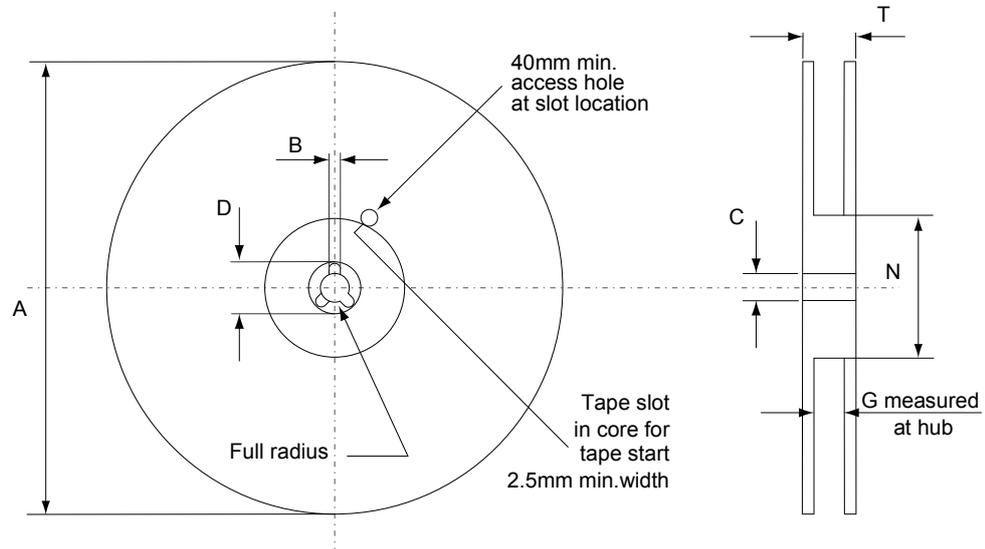
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Table 10. **DPAK (TO-252) tape and reel mechanical data**

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

4.4 TO-220 type A package information

Figure 25. TO-220 type A package outline
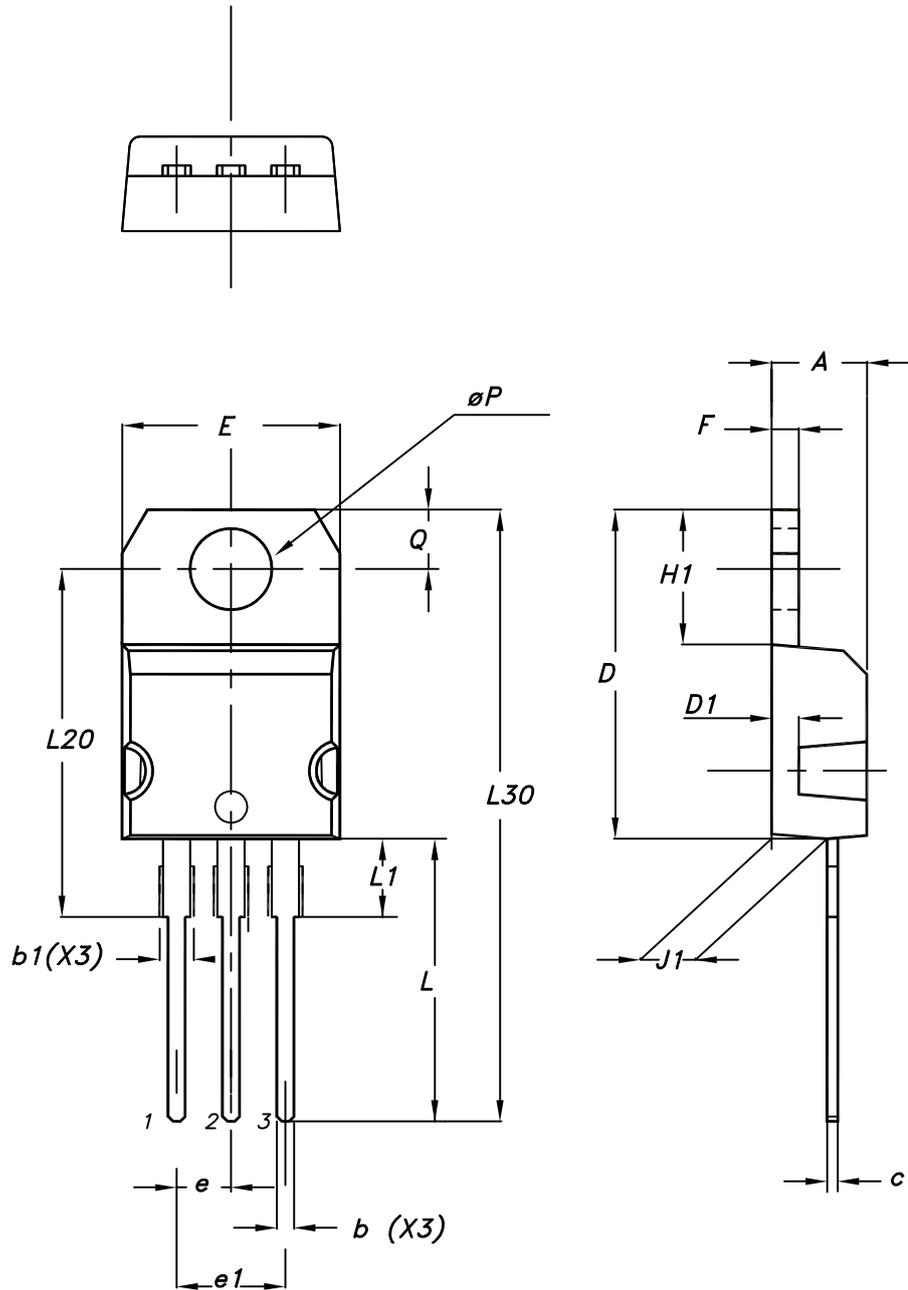
0015988_typeA_Rev_21

Table 11. TO-220 type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95

Revision history

Table 12. Document revision history

Date	Version	Changes
20-Apr-2010	1	Initial release.
03-Sep-2010	2	Document status promoted from preliminary data to datasheet. Inserted *Section 2.1: Electrical characteristics (curves)*. Corrected RDS(on) max value in: *Features*.
03-Feb-2011	3	Modified: *Figure 4.* Modified: *note 1*. Modified: *Table 5*.
21-Oct-2011	4	Updated VDSS (@Tjmax) in cover page. Updated Section 4: Package mechanical data. Minor text changes
15-Nov-2011	5	The part number STF8NM50N has been moved to a separate datasheet.
13-Sep-2012	6	*Figure 2* and *Figure 4* have been modified. *Section 4: Package mechanical data* has been updated.
04-Sep-2018	7	The part number STU8NM50N has been moved to a separate datasheet. Removed maturity status indication from cover page. The document status is production data. Updated Section 4 Package information. Minor text changes

Contents

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