

Automotive-grade P-channel -30 V, 5 mΩ typ., -80 A STripFET™ H6 Power MOSFET in a DPAK package

Datasheet - production data

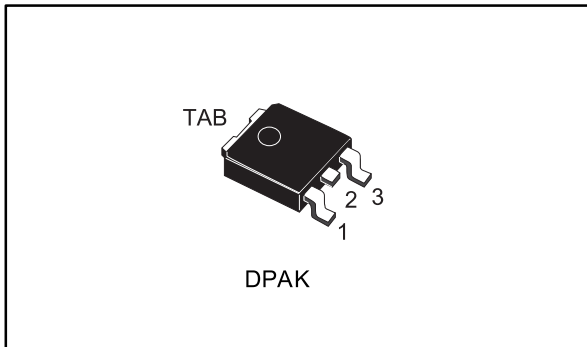
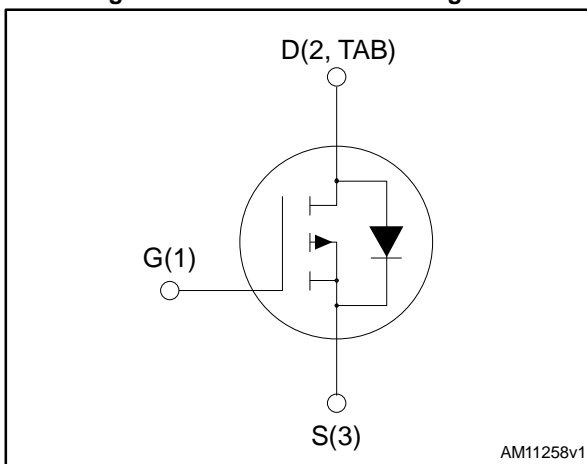


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D	P _{TOT}
STD95P3LLH6AG	-30 V	6.9 mΩ	-80 A	104 W

- Designed for automotive applications and AEC-Q101 qualified
- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss
- Logic level

Applications

- Switching applications

Description

This device is a P-channel Power MOSFET developed using the STripFET™ H6 technology with a new trench gate structure. The resulting Power MOSFET exhibits very low R_{DS(on)} in all packages.

Table 1: Device summary

Order code	Marking	Package	Packing
STD95P3LLH6AG	95P3LLH6	DPAK	Tape and reel

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	-30	V
V_{GS}	Gate-source voltage	± 18	V
$I_D^{(1)}$	Drain current (continuous) at $T_{case} = 25\text{ }^\circ\text{C}$	-80	A
	Drain current (continuous) at $T_{case} = 100\text{ }^\circ\text{C}$	-80	A
$I_{DM}^{(2)}$	Drain current (pulsed)	-320	A
P_{TOT}	Total dissipation at $T_{case} = 25\text{ }^\circ\text{C}$	104	W
$E_{AS}^{(3)}$	Single pulse avalanche energy	650	mJ
T_{stg}	Storage temperature range	-55 to 150	$^\circ\text{C}$
T_j	Operating junction temperature range		

Notes:

- (1) Limited by wire bonding
- (2) Pulse width is limited by safe operating area.
- (3) starting $T_j = 25\text{ }^\circ\text{C}$, $I_{AS} = -40\text{ A}$, $V_{DD} = -25\text{ V}$

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	1.2	$^\circ\text{C/W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	50	

Notes:

- (1) When mounted on a 1-inch² FR-4, 2 Oz copper board

2 Electrical characteristics

($T_{\text{case}} = 25\text{ °C}$ unless otherwise specified)

Table 4: Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage	$V_{\text{GS}} = 0\text{ V}$, $I_{\text{D}} = -1\text{ mA}$	-30			V
I_{DSS}	Zero gate voltage drain current	$V_{\text{GS}} = 0\text{ V}$, $V_{\text{DS}} = -30\text{ V}$			-1	μA
		$V_{\text{GS}} = 0\text{ V}$, $V_{\text{DS}} = -30\text{ V}$, $T_{\text{case}} = 125\text{ °C}^{(1)}$			-10	
I_{GSS}	Gate-body leakage current	$V_{\text{DS}} = 0\text{ V}$, $V_{\text{GS}} = \pm 18\text{ V}$			± 100	nA
$V_{\text{GS(th)}}$	Gate threshold voltage	$V_{\text{DS}} = V_{\text{GS}}$, $I_{\text{D}} = -250\text{ }\mu\text{A}$	-1		-2.5	V
$R_{\text{DS(on)}}$	Static drain-source on-resistance	$V_{\text{GS}} = -10\text{ V}$, $I_{\text{D}} = -40\text{ A}$		5	6.9	m Ω
		$V_{\text{GS}} = -4.5\text{ V}$, $I_{\text{D}} = -40\text{ A}$		7.5	9.7	

Notes:

⁽¹⁾Defined by design, not subject to production test.

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{ISS}	Input capacitance	$V_{\text{DS}} = -25\text{ V}$, $f = 1\text{ MHz}$, $V_{\text{GS}} = 0\text{ V}$	-	6250	-	pF
C_{OSS}	Output capacitance		-	830	-	
C_{RSS}	Reverse transfer capacitance		-	590	-	
Q_{g}	Total gate charge	$V_{\text{DD}} = -15\text{ V}$, $I_{\text{D}} = -80\text{ A}$, $V_{\text{GS}} = -10\text{ V}$ (see Figure 14 : "Gate charge test circuit")	-	113	-	nC
Q_{gs}	Gate-source charge		-	18.5	-	
Q_{gd}	Gate-drain charge		-	19	-	

Table 6: Switching on/off (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{\text{d(on)}}$	Turn-on delay time	$V_{\text{DD}} = -15\text{ V}$, $I_{\text{D}} = -80\text{ A}$, $R_{\text{G}} = 4.7\text{ }\Omega$, $V_{\text{GS}} = -10\text{ V}$ (see Figure 13 : "Switching times test circuit for resistive load")	-	15	-	ns
t_{r}	Rise time		-	30	-	
$t_{\text{d(off)}}$	Turn-off delay time		-	110	-	
t_{f}	Fall time		-	70	-	

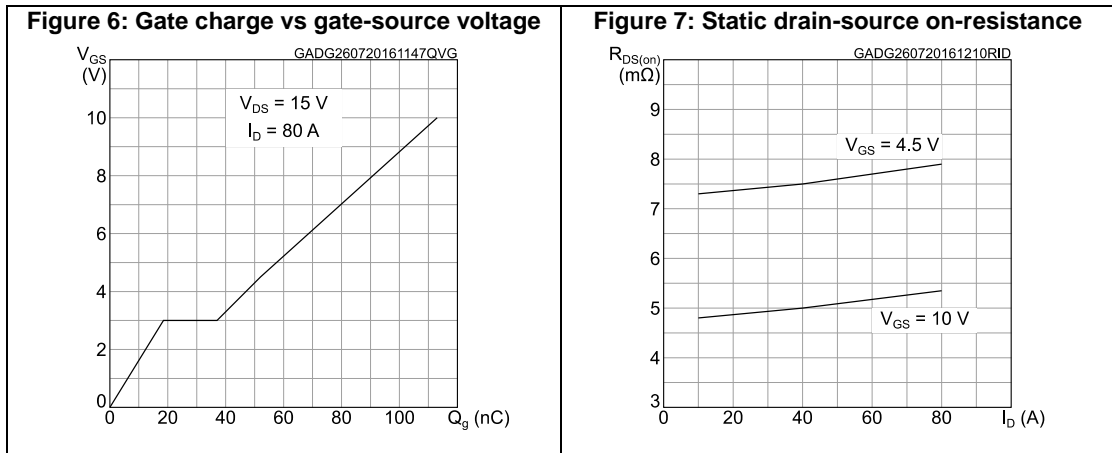
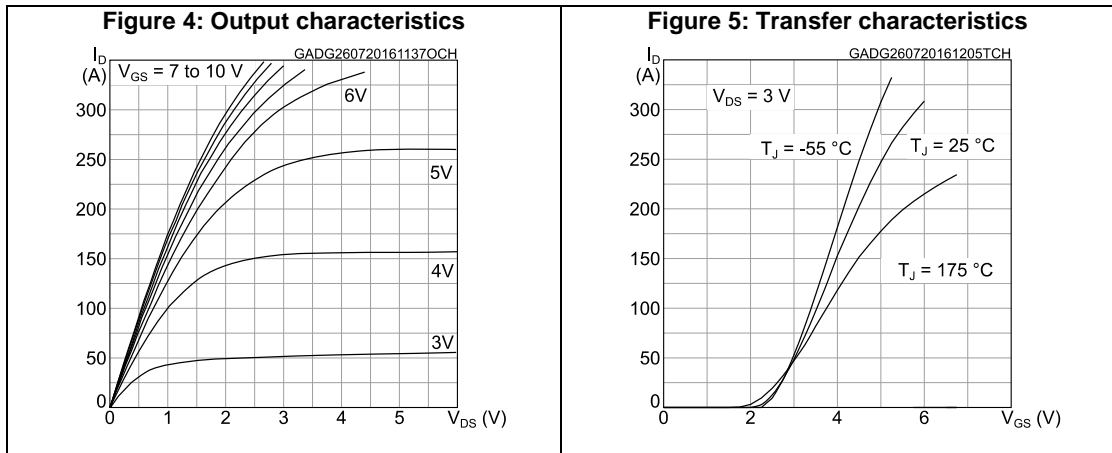
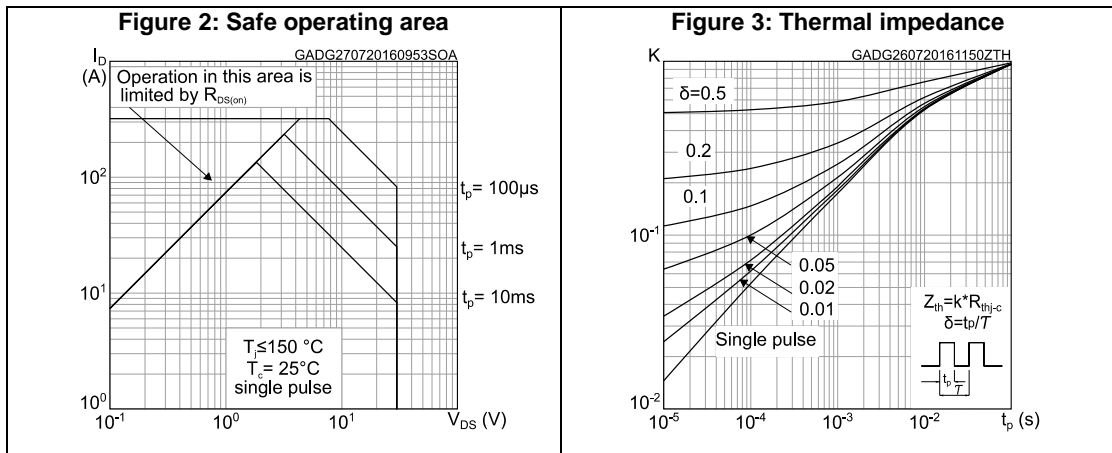
Table 7: Source-drain diode

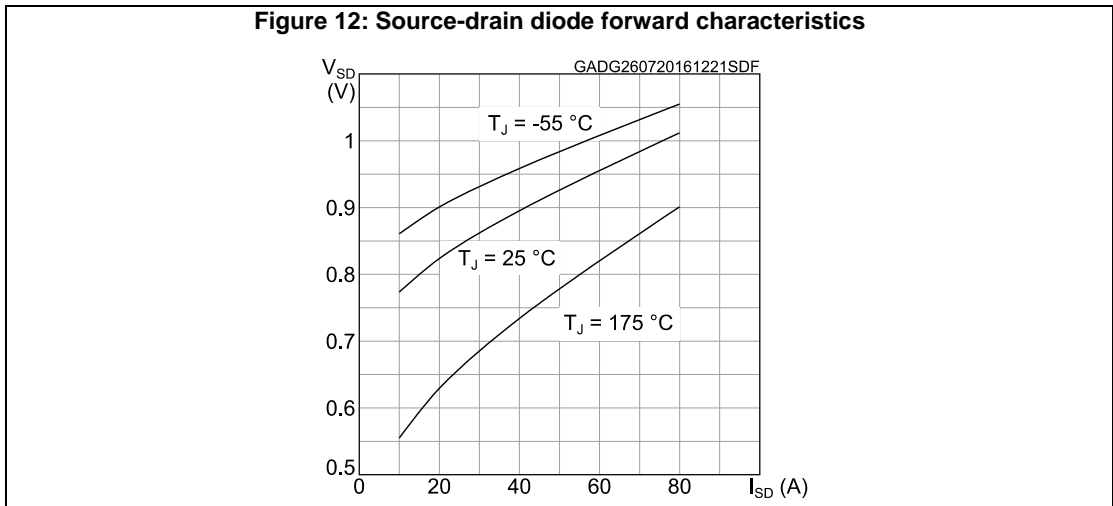
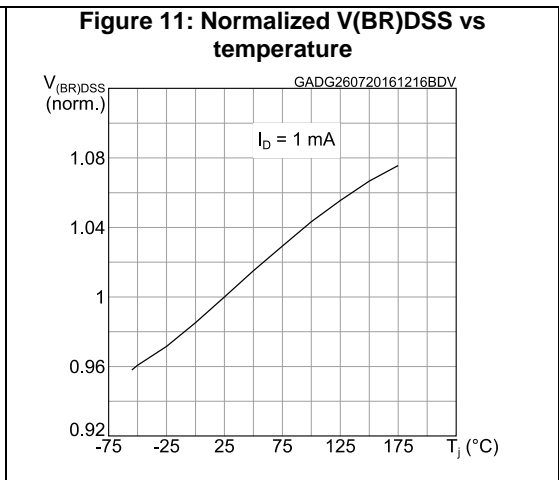
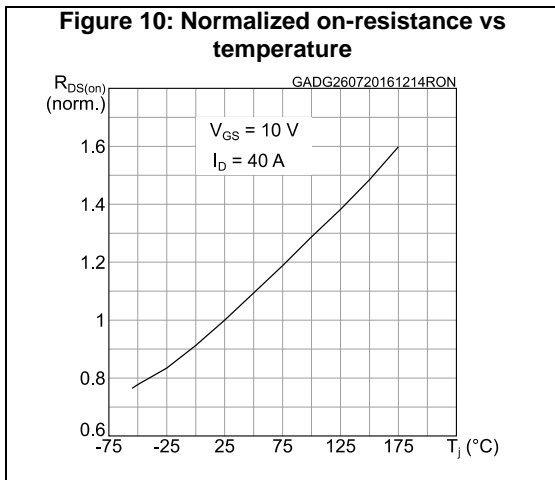
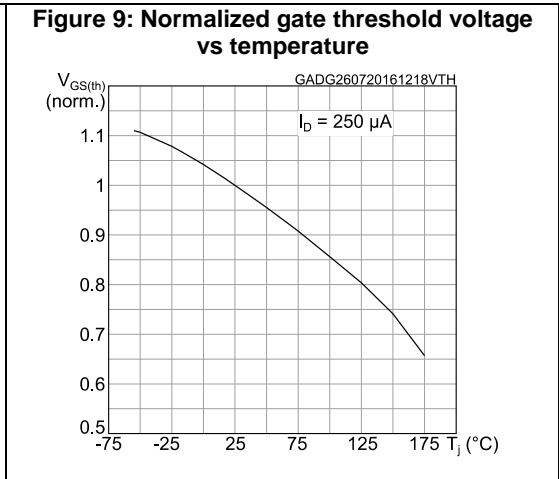
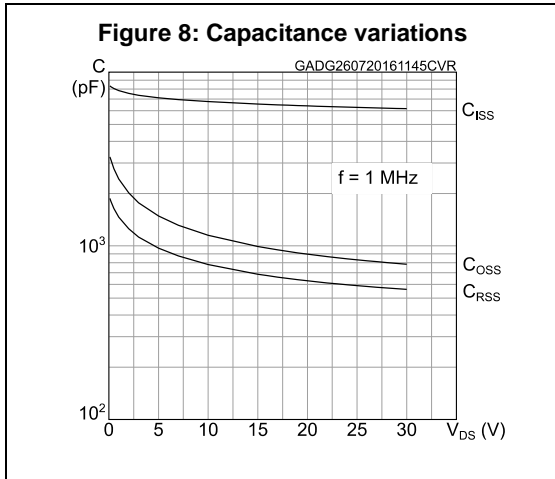
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		-80	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		-320	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = -80\text{ A}$	-		-1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = -80\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = -24\text{ V}$ (see Figure 15: "Test circuit for inductive load switching and diode recovery times")	-	27		ns
Q_{rr}	Reverse recovery charge		-	17		nC
I_{RRM}	Reverse recovery current		-	-1.2		A

Notes:

- (1) Pulse width is limited by safe operating area.
(2) Pulse test: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)





For the P-channel Power MOSFET, current and voltage polarities are reversed.

3 Test circuits

Figure 13: Switching times test circuit for resistive load

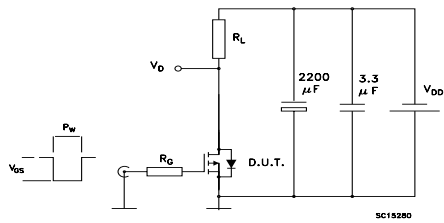


Figure 14: Gate charge test circuit

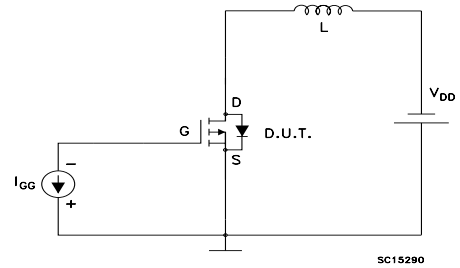
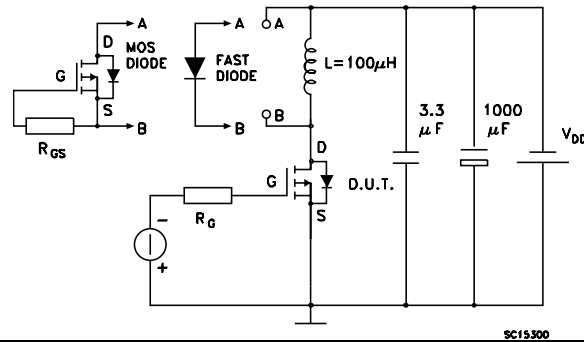


Figure 15: Test circuit for inductive load switching and diode recovery times

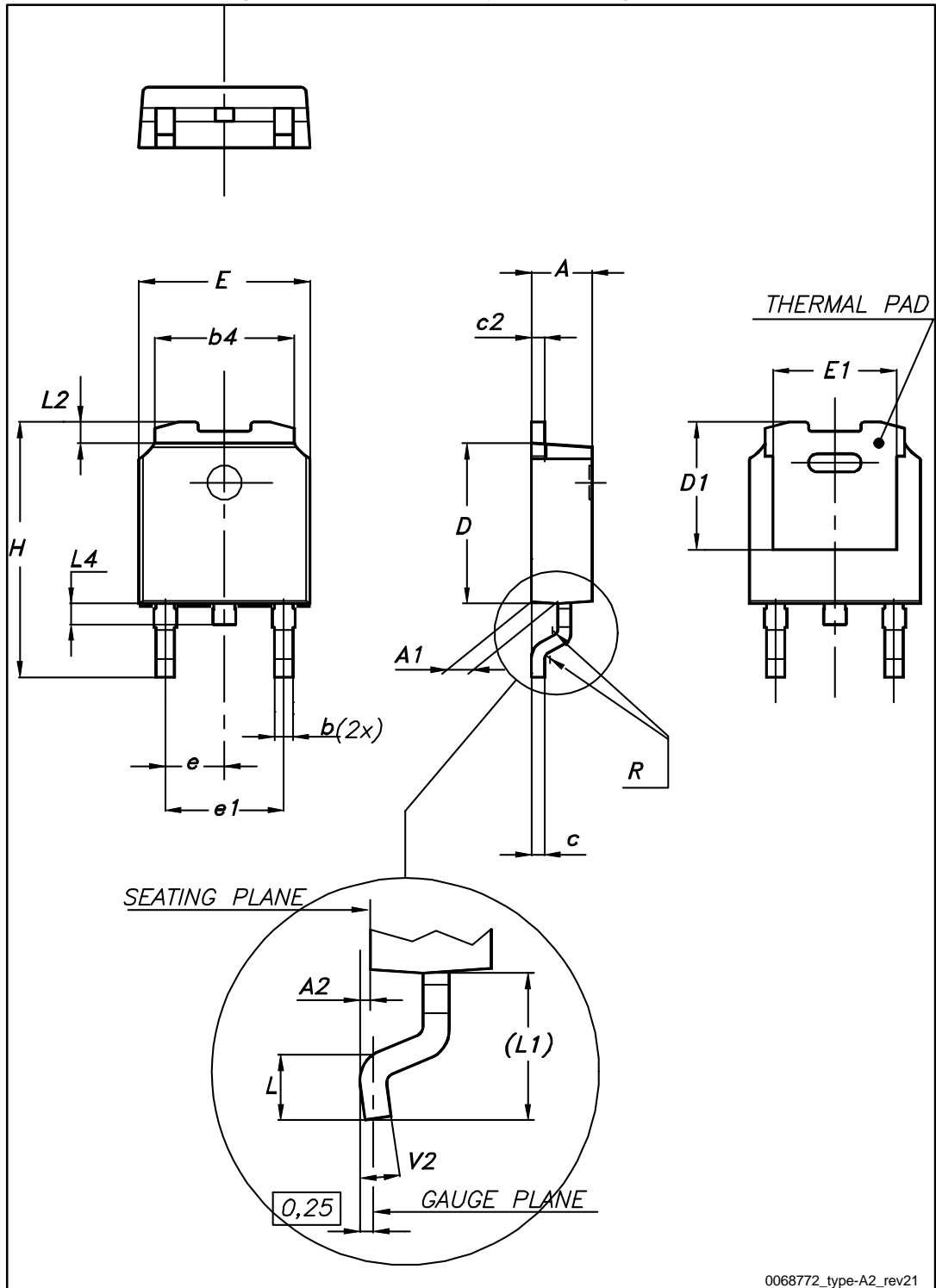


4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 DPAK type A2 package information

Figure 16: DPAK (TO-252) type A2 package outline

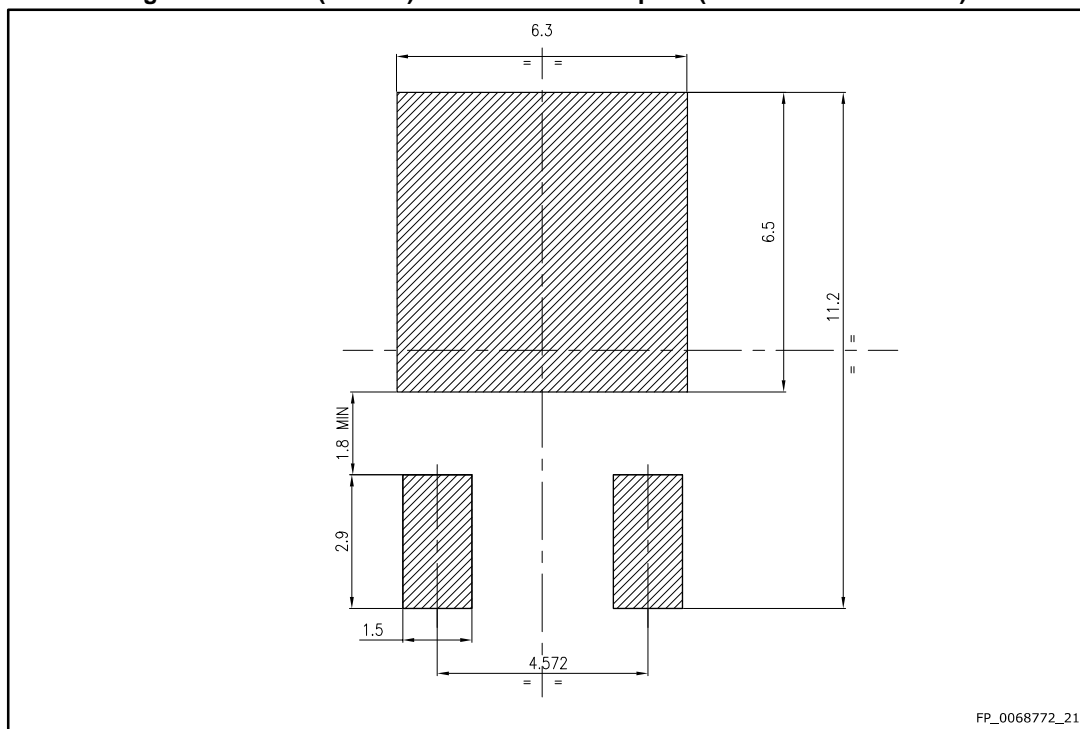


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Table 8: DPAK (TO-252) type A2 mechanical data

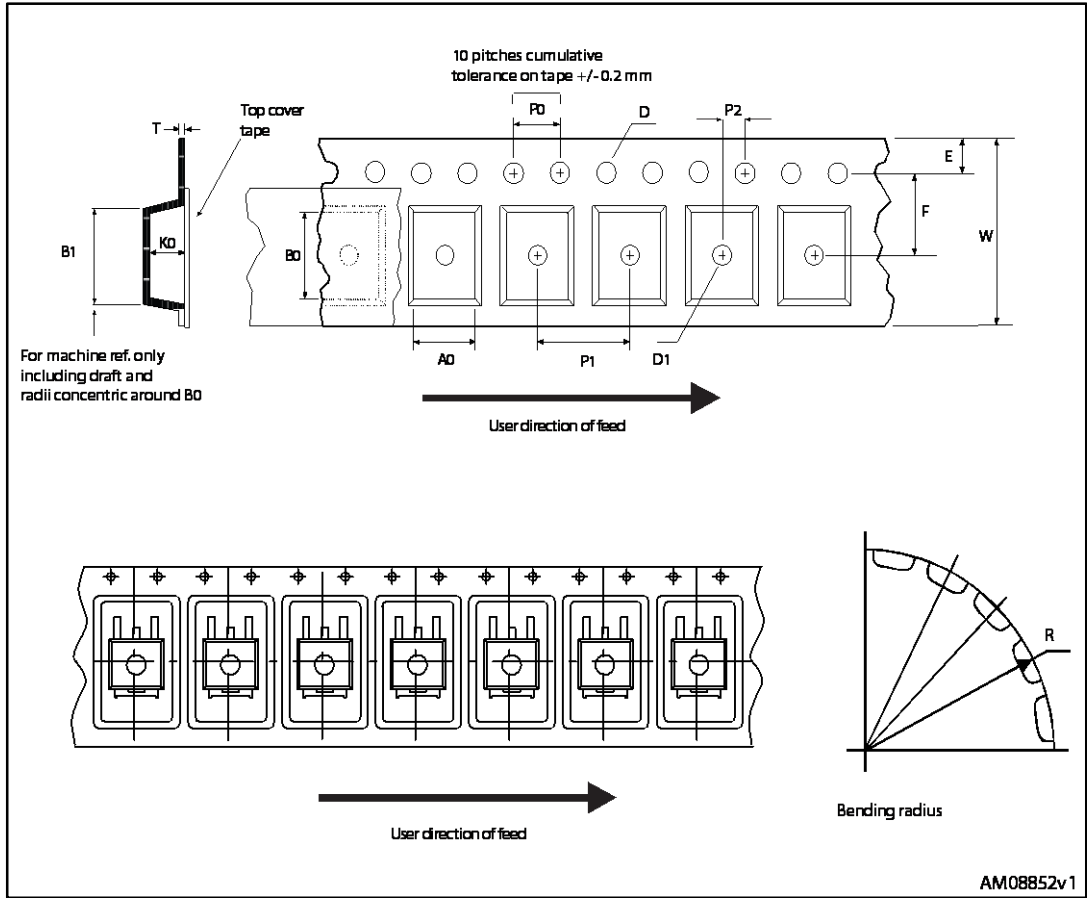
Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	5.10	5.20	5.30
e	2.16	2.28	2.40
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
L1	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 17: DPAK (TO-252) recommended footprint (dimensions are in mm)



4.2 DPAK packing information

Figure 18: DPAK (TO-252) tape outline



5 Revision history

Table 10: Document revision history

Date	Revision	Changes
26-Jul-2016	1	First release.

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