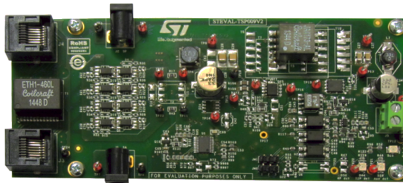


3.3 V/6 A, synchronous flyback converter, Power Over Ethernet (PoE) - IEEE 802.3at compliant reference design



Features

- IEEE 802.3at compliant PD interface
- Works with power supplied from Ethernet LAN cables or from local auxiliary sources
- Line input voltage range: 40 V_{DC} to 60 V_{DC}
- Output voltage: 3.35 V_{DC} ± 5%
- Output current: 6 A
- Peak-to-peak output ripple: < 25 mV
- Efficiency DC-DC full-load: > 90%
- Overall peak efficiency: > 87%
- Transient response $\Delta V_{\text{OUTPK-PK}}$ to 50% load step: < 250 mV
- ΔV in load line case: < 0.5%
- RoHs compliant

Description

The [STEVAL-TSP009V2](#) is a reference design for a PoE+, high-efficiency, 3.3 V - 6 A flyback converter based on the [PM8803](#) PoE controller.

The [PM8803](#) is a highly integrated device embedding an IEEE802.3at-compliant powered device (PD) interface together with a PWM controller and support for auxiliary sources.

The [STEVAL-TSP009V2](#) reference design is based on an isolated flyback CCM converter featuring synchronous rectification with gate driver transformer.

Product summary	
3.3 V/6 A, synchronous fly-back converter, Power Over Ethernet (PoE) - IEEE 802.3at compliant reference design	STEVAL-TSP009V2
High efficiency integrated IEEE 802.3at PoE-PD interface and PWM controller type 2 PSE indicator, plus support for forward active clamp topology	PM8803

1 Detailed description

The [STEVAL-TSP009V2](#) reference design for the [PM8803](#) covers a broad range of Power over Ethernet (PoE) applications.

The [PM8803](#) is a highly integrated device embedding an IEEE802.3at compliant powered device (PD) interface together with a PWM controller and support for auxiliary sources.

Although the [PM8803](#) can be configured to work in several isolated topologies (self-driven or transformer gate-driven), we focus here on a high-efficiency isolated flyback converter topology with synchronous rectification, 3.3 V output voltage and 6 A output current capability.

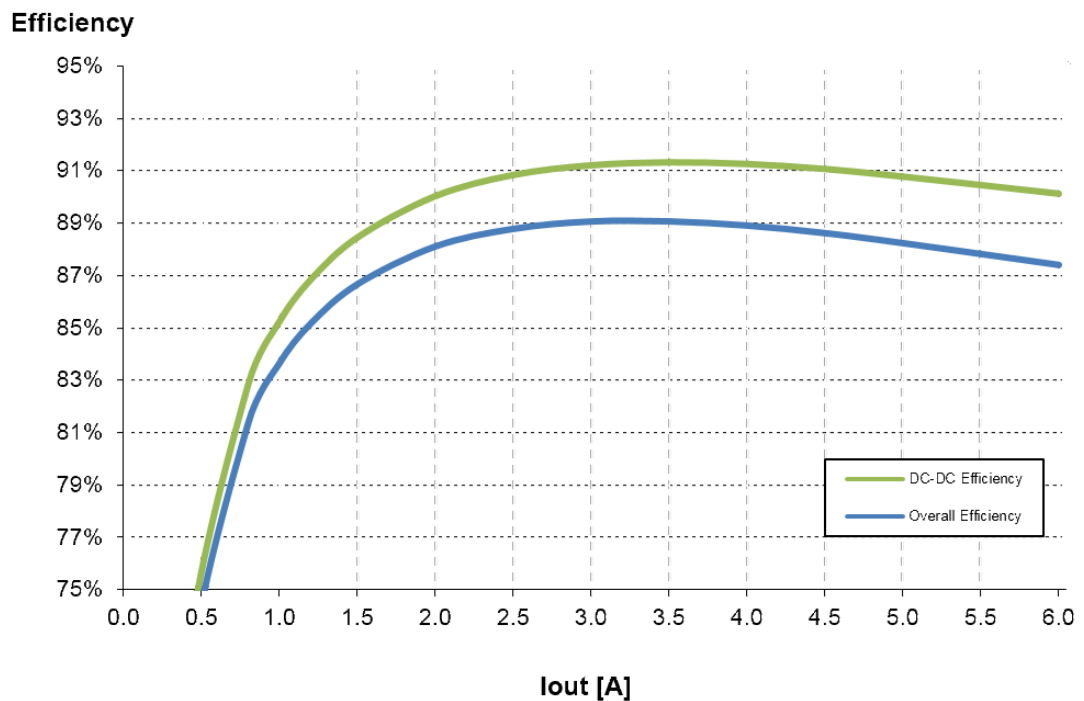
Auxiliary sources can be connected to the reference design on two different input connectors: one input (AUX II) allows prevalence of the auxiliary sources with respect to the PoE, whereas the other input (AUX I) allows the use of a wall adapter with voltage lower than the internal PoE UVLO threshold, while still benefiting from the inherent inrush and DC current limit.

The possible configurations supported by the [STEVAL-TSP009V2](#) reference design are:

- input diode bridges (four possible options, including active bridges)
- optional 4-pair detection circuit, to detect a high power PSE source
- optional booster circuit, to increase the max input current over 800 mA
- diode or synchronous rectification (four package options for diode and three package options for MOSFET)
- primary side snubber (three options including active clamp)
- power transformer (three size options for transformer gate-driven solutions and two size options for self-driven) applications

1.1 Efficiency

Figure 1. STEVAL-TSP004V2 reference design: 3.3 V_{OUT} overall and DC-DC efficiency



2 Schematic diagrams

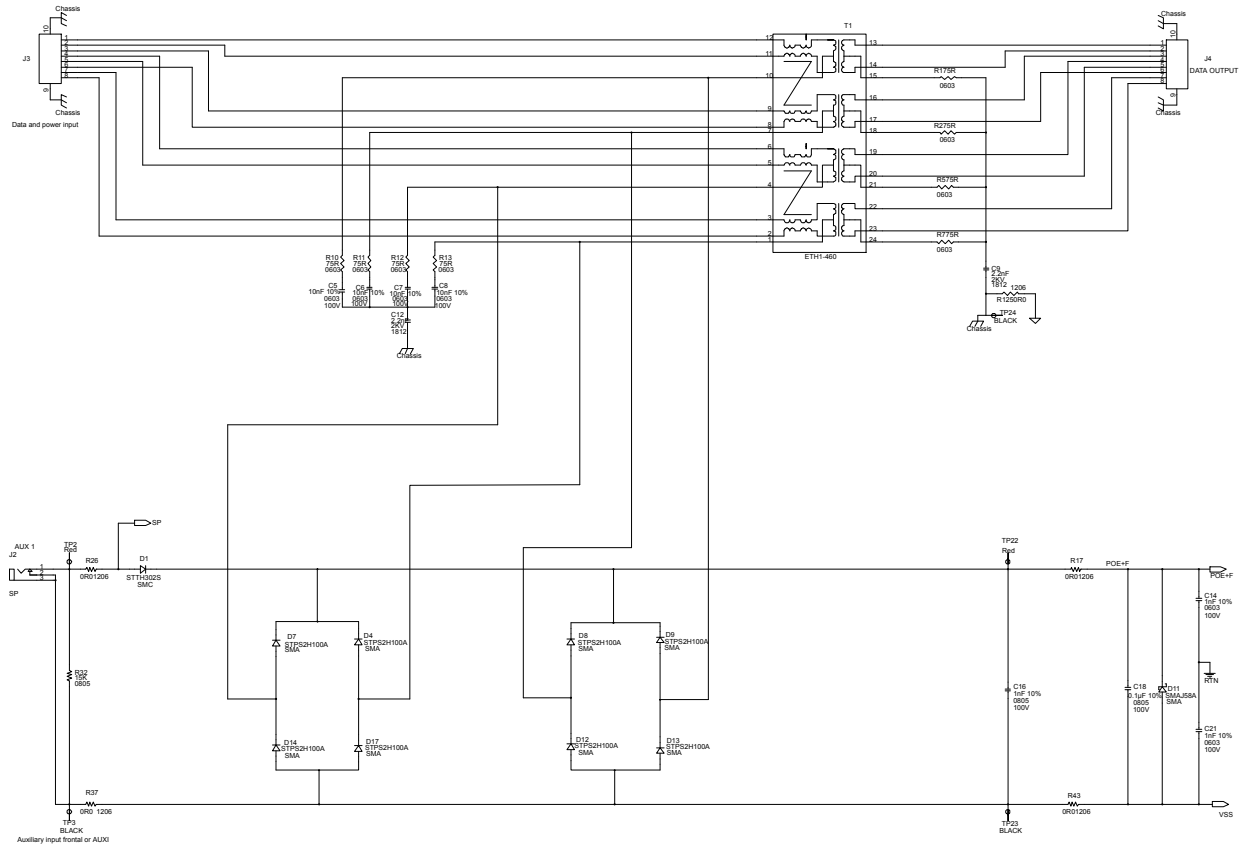
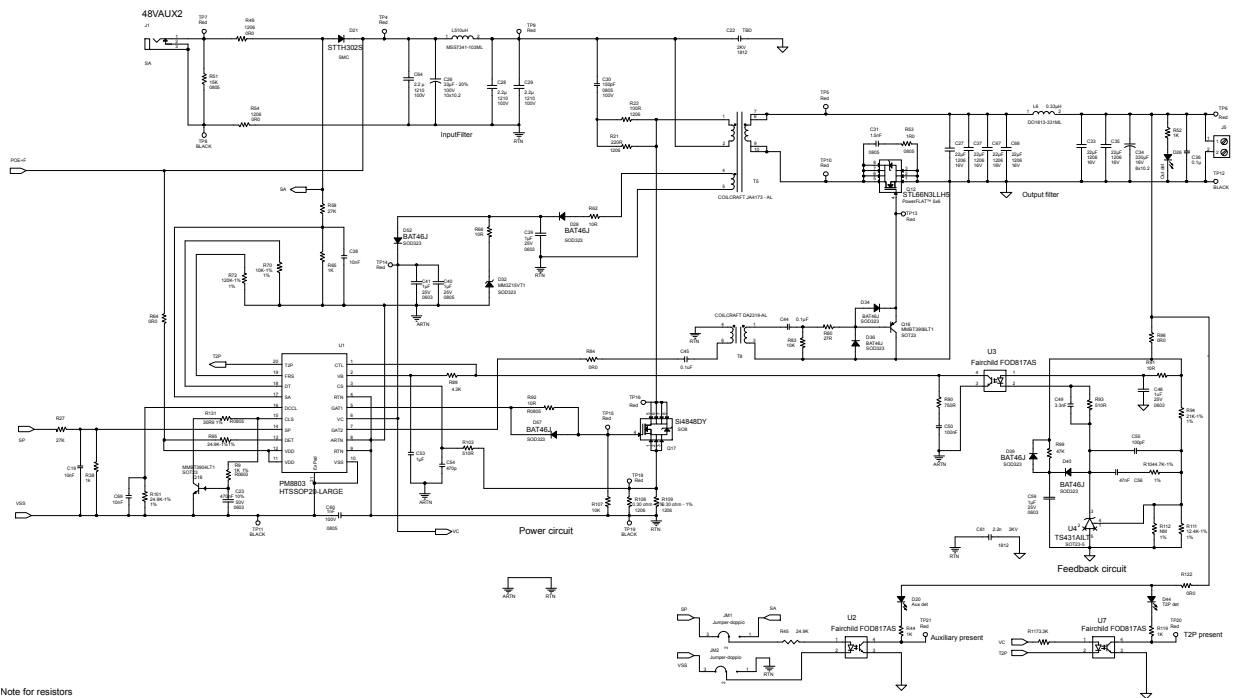
Figure 2. STEVAL-TSP009V2 circuit schematic (1 of 2)


Figure 3. STEVAL-TSP009V2 circuit schematic (2 of 2)


Note for resistors
Where not indicated, the body is 0603 and tolerance is 5%

Note for capacitors
Where not indicated, the body is 0603 and the voltage is 50 V

Note:
The ARTN is a dedicated plane of signal ground that is connected to the RTN power ground plane close to pin 4 and 9 of PM8803

Note for Jumpers JM1 and JM2
Move the short on both jumpers at the same time:
- short between pin1 and 2 when using AUX2 input
- short between pin2 and 3 when using AUX1 input

Revision history

Table 1. Document revision history

Date	Version	Changes
24-Apr-2015	1	Initial release.
07-May-2019	2	Updated title. Added product summary table. Minor text and formatting changes.

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