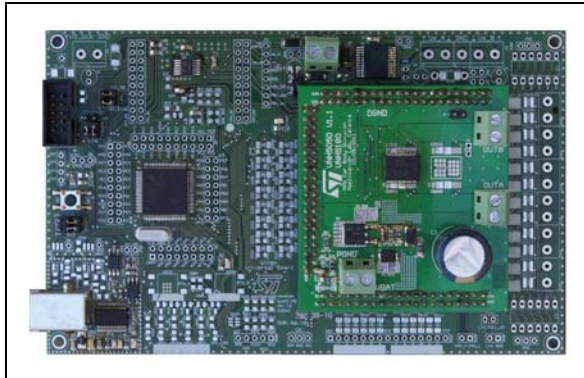


## Motor driver evaluation board based on VNH5050A

Data brief



### Description

STEVAL-VNH5050A offers dedicated power stage and controls suitable for electric DC motor driving. This evaluation board comes pre-assembled with VNH5050A H-bridge belonging to the VNH Motor Driver series based on VIPower® proprietary technology. Typical applications are dual washer pump and seat regulation.

This evaluation board consists of a motherboard (STM8 Universal Board) and a daughterboard.

The motherboard, based on STM8 microcontroller, provides the logic section for monitoring and driving the VNH5050A assembled in the daughterboard.

With the aim to make simpler the board usage and settings, ST provides a dedicated and user-friendly software with a Graphic User Interface (GUI). This enables the user to set VNH5050A parameters (PWM, Motor direction...) and at the same time it shows real time device diagnostic information like current output evolution, battery voltage monitoring, board temperature and much more.

### Features

Type	$R_{DS(on)}$	$I_{out}$	$V_{CC(max)}$
VNH5050A-E	50 mΩ max (per leg)	30 A	41 V

- Handling up to 30 A of maximum motor current output
- Undervoltage and overvoltage shutdown
- Overvoltage clamp
- Device thermal protection
- Cross-conduction protection
- Current and power limitation
- Very low standby power consumption
- Programmable PWM operation (up to 20 kHz)
- Protection against loss of ground and loss of  $V_{CC}$
- Motor current monitoring (thanks to VNH5050A current sense output)
- Device output protected against short to ground and short to  $V_{CC}$
- Graphic User Interface (GUI)

**Table 1. Device summary**

Order code	Reference
STEVAL-VNH5050A	VNH5050A evaluation board



# 1 Application schematics and layouts

## 1.1 VNH5050A daughterboard

Figure 1. VNH5050A daughterboard top layer

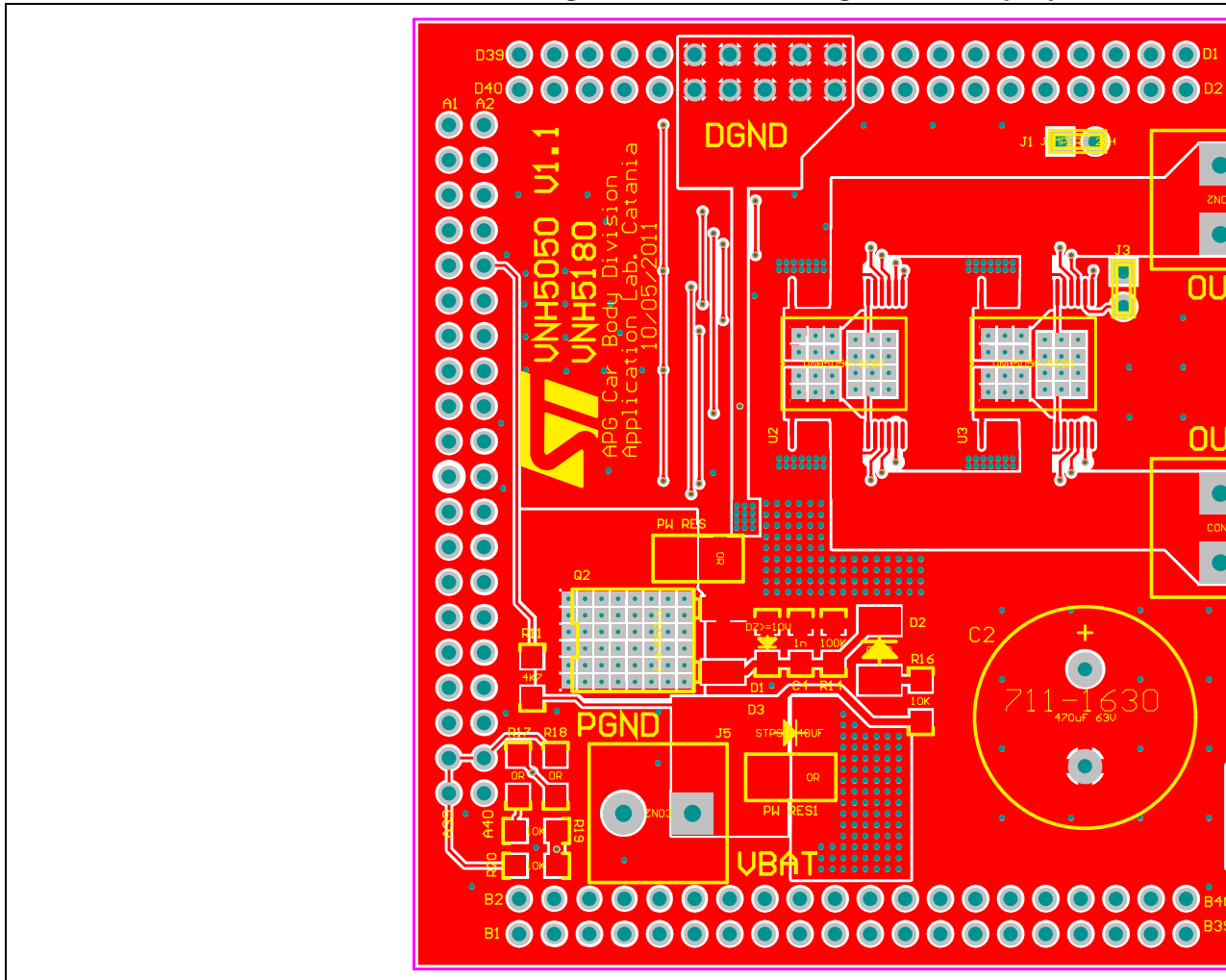


Figure 2. VNH5050A daughterboard bottom layer

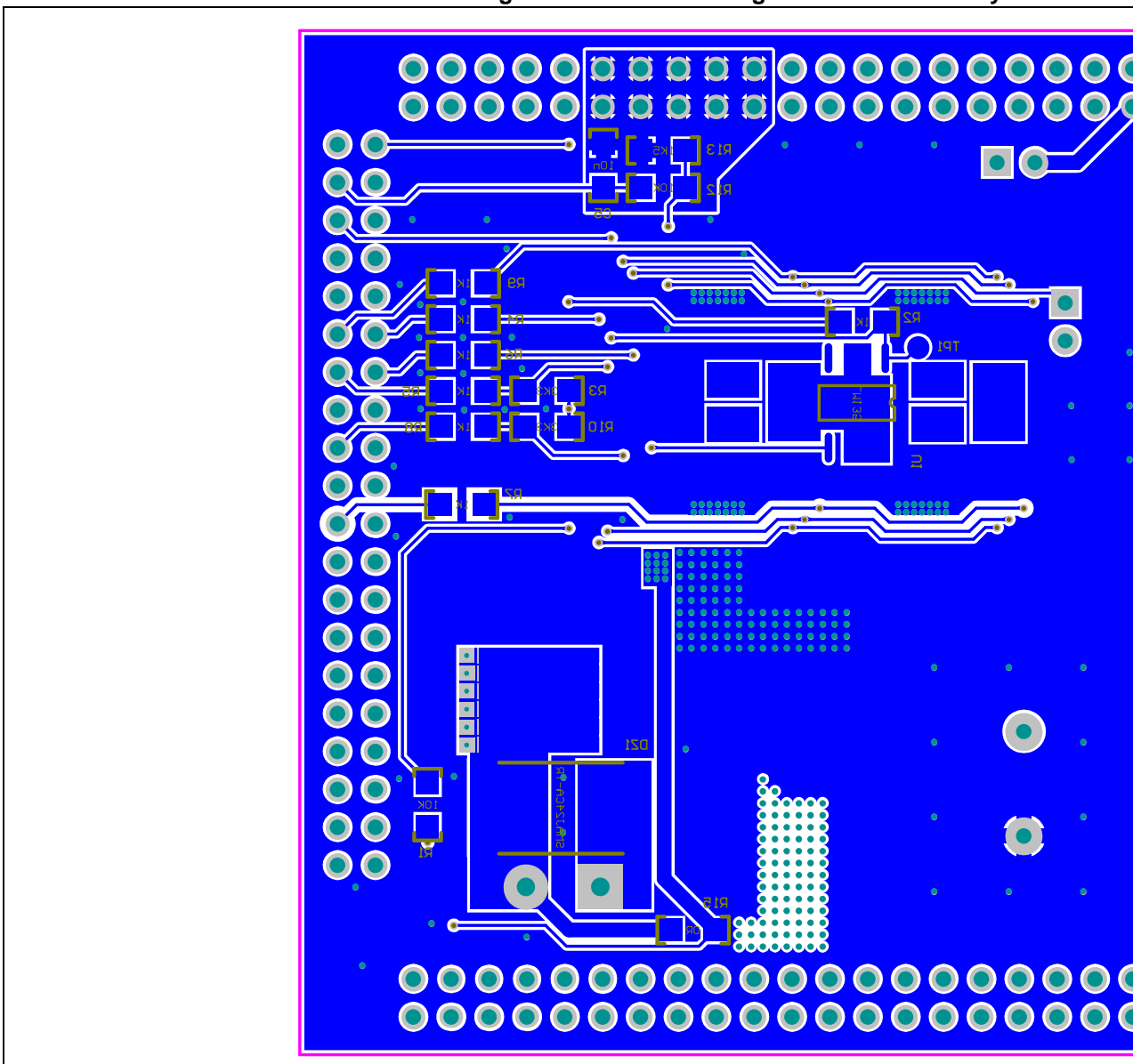
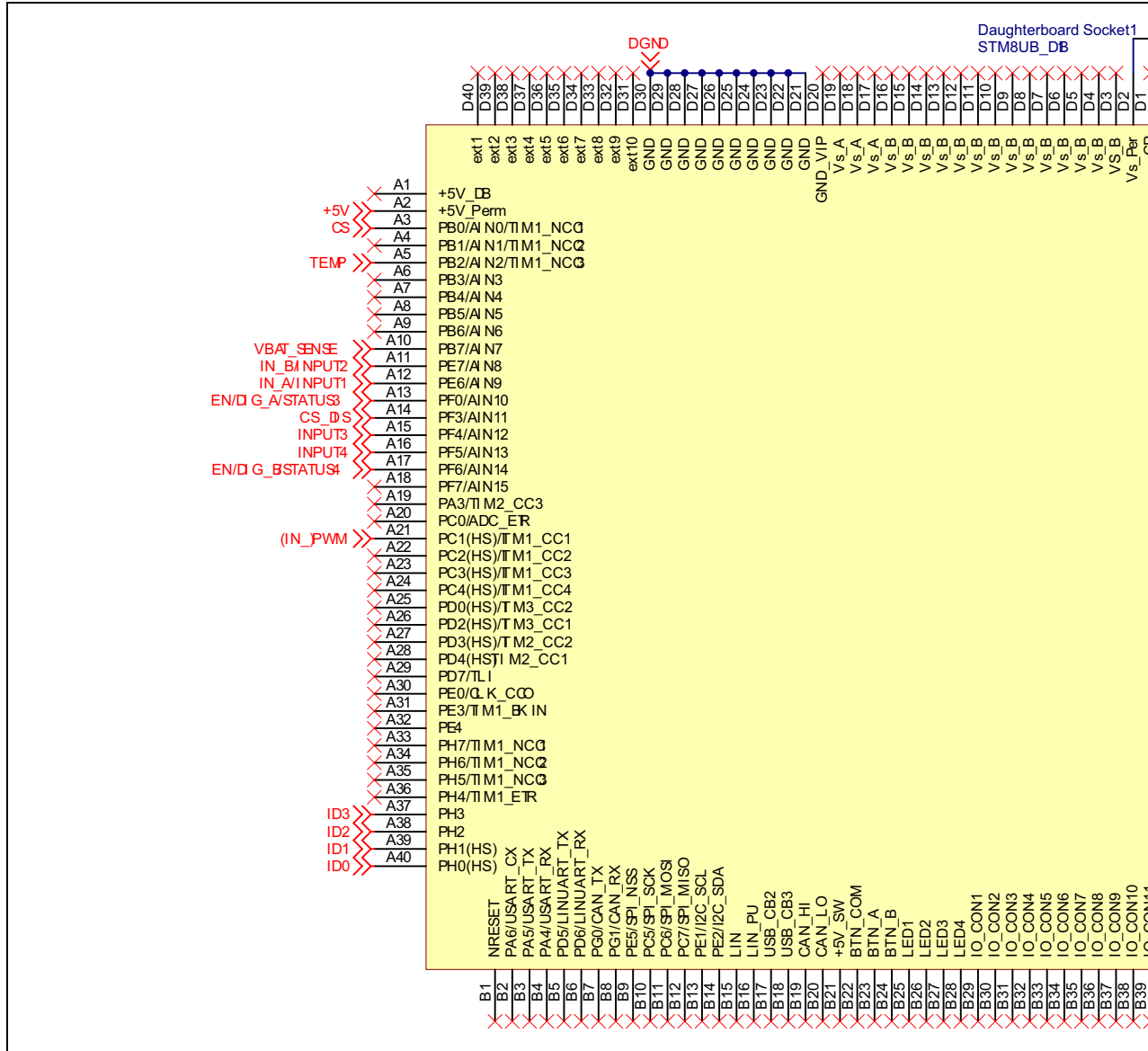




Figure 3. VNH5050A daughterboard application schematic (p

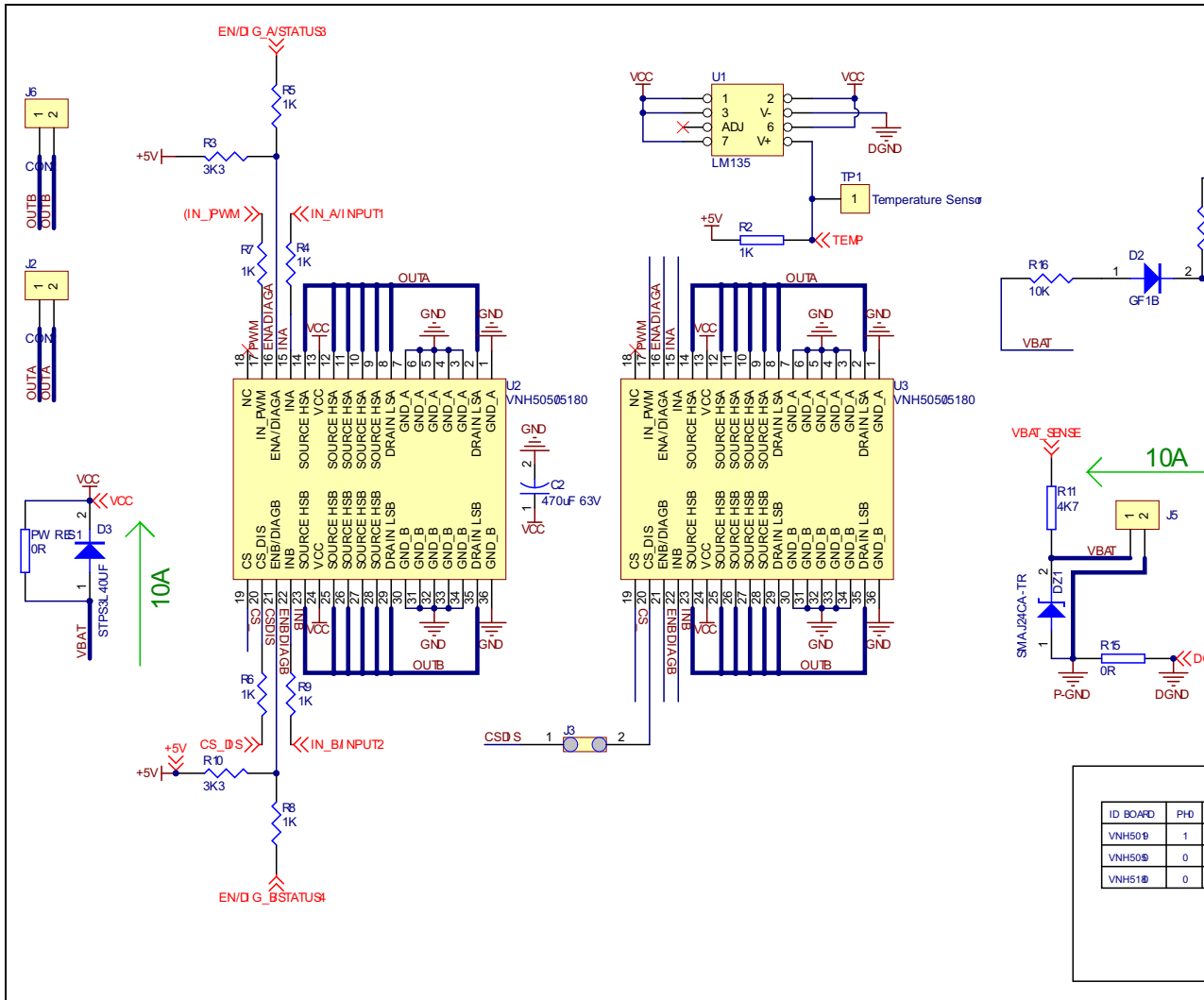




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Figure 4. VN5050A daughterboard application schematic (p



ID BOARD	PH0
VN5050B	1
VN5050	0
VN5051	0



## 1.2 STM8 motherboard

Figure 5. STM8 motherboard top layer

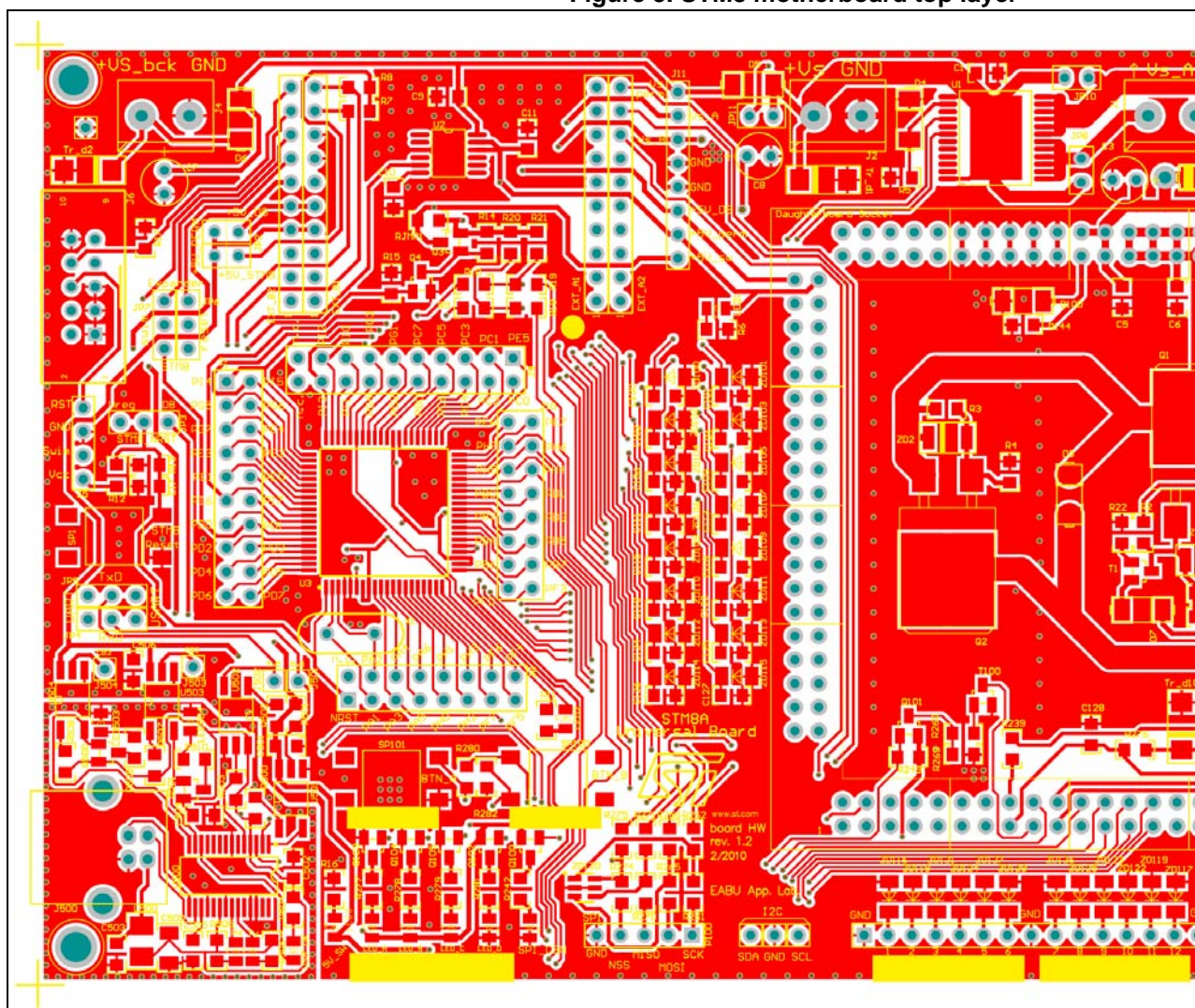


Figure 6. STM8 motherboard bottom layer

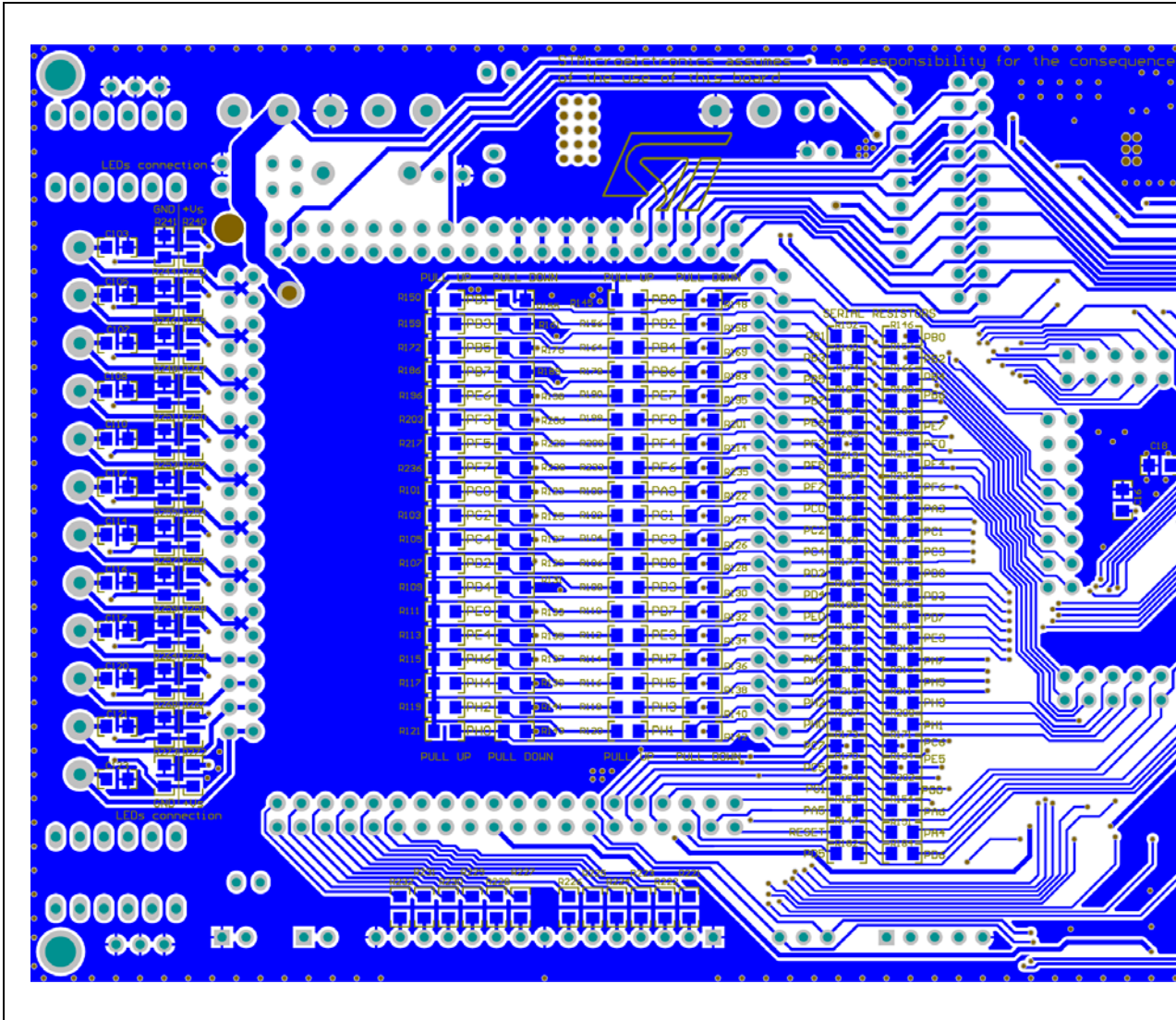




Figure 7. STM8 motherboard - I/O & Body application schematic

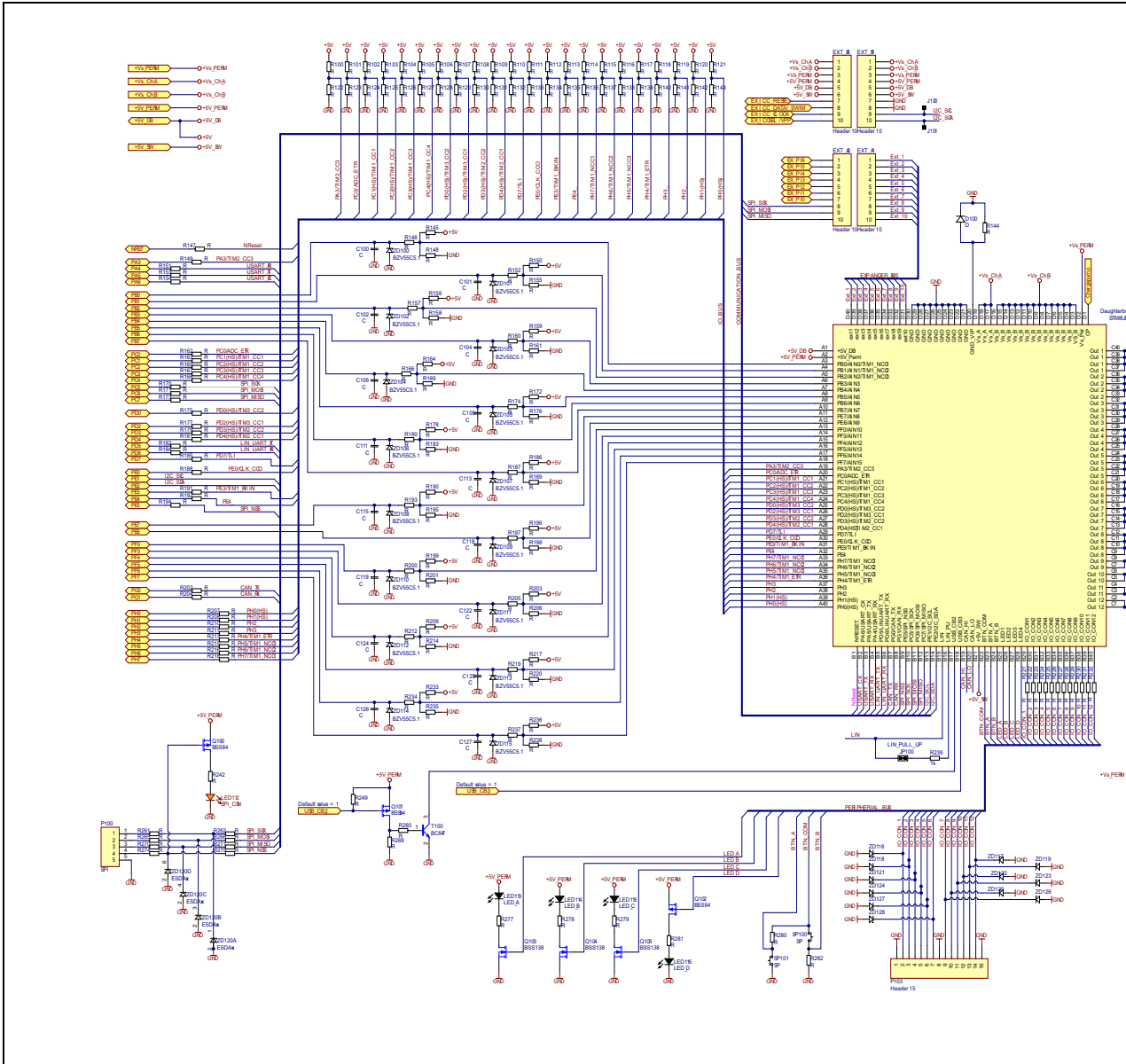






Figure 8. STM8 motherboard - STM8 & Supply application schematic

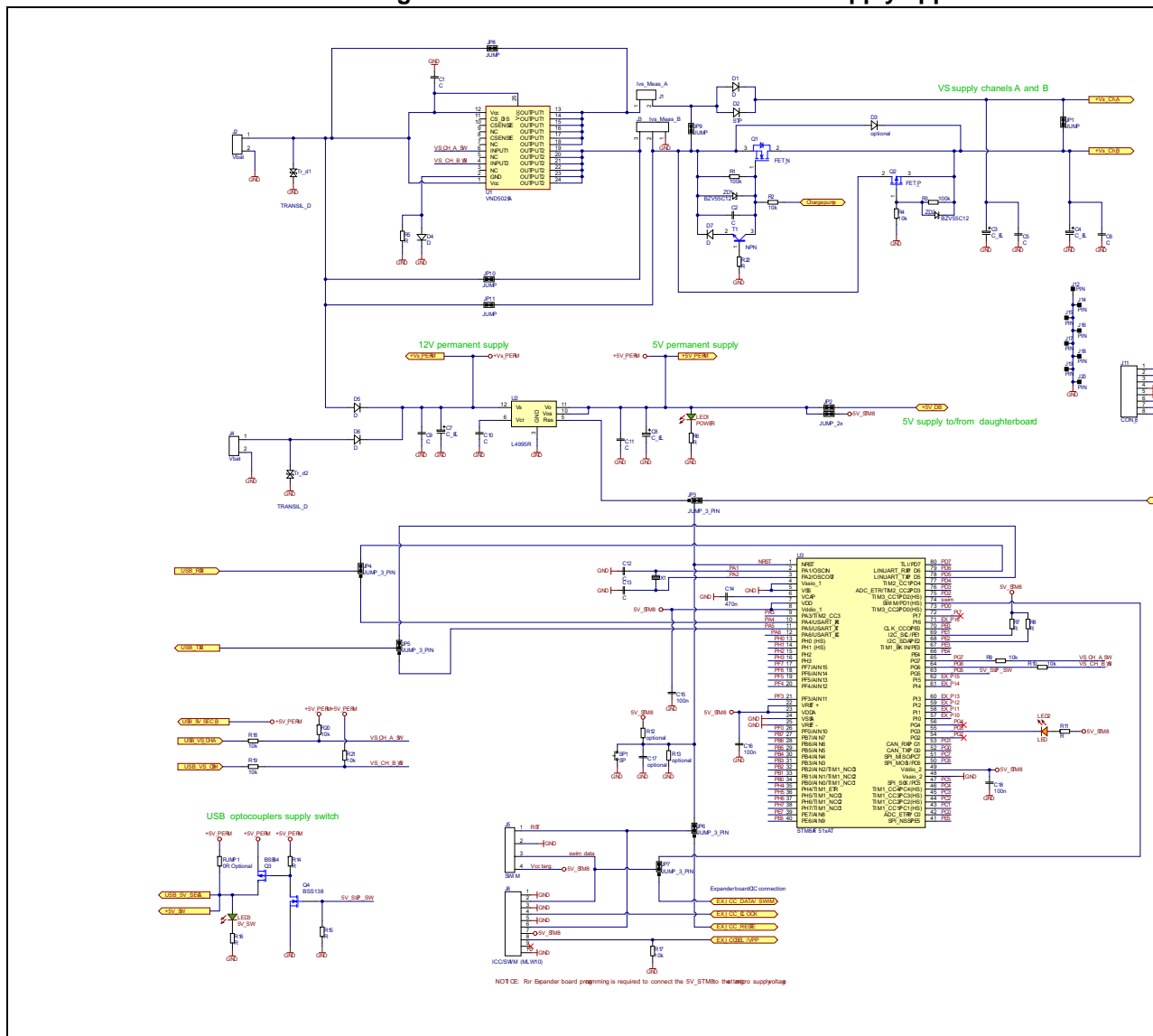
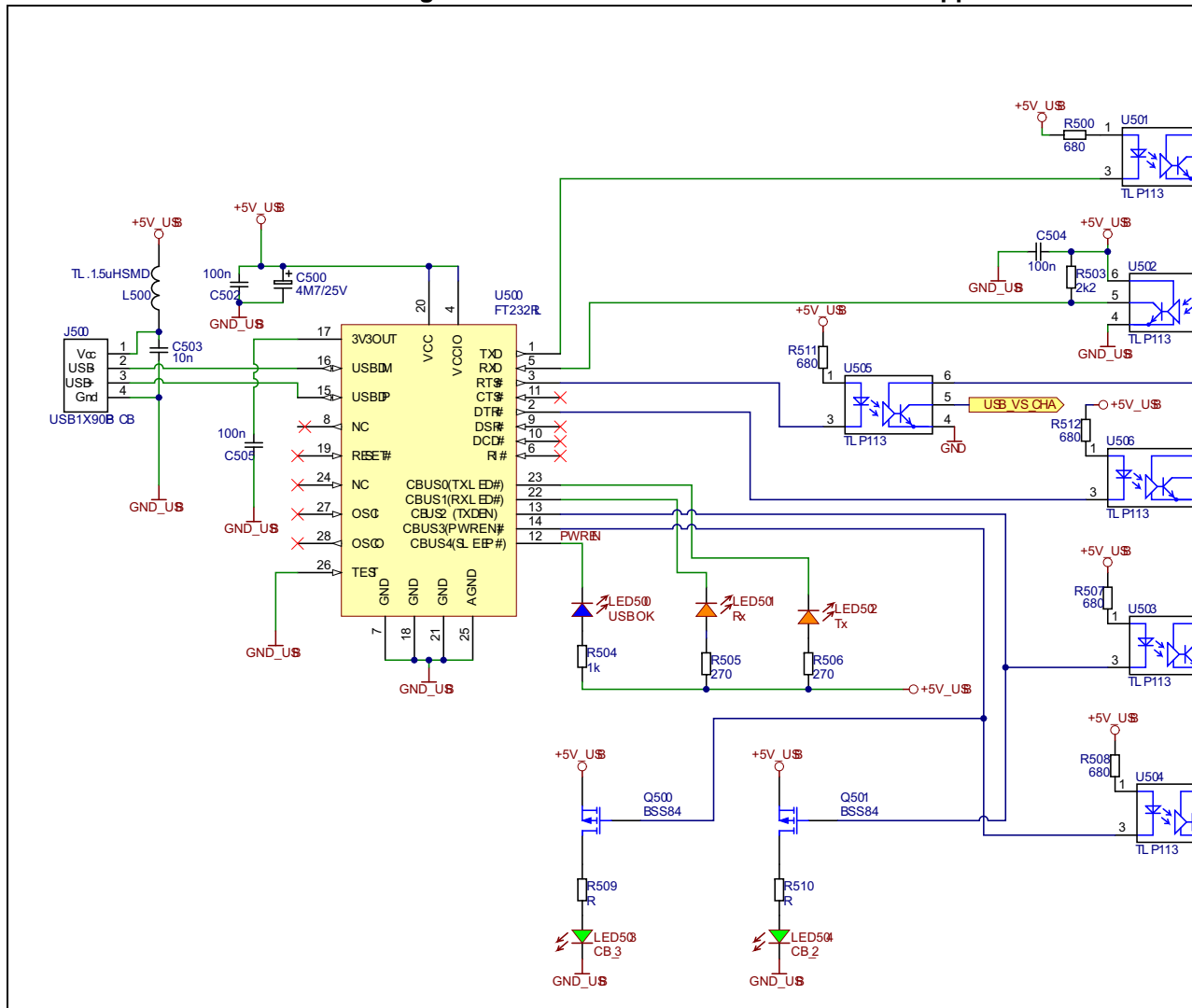




Figure 9. STM8 motherboard - USB Interface application schematic



## 2 Revision history

Table 2. Document revision history

Date	Revision	Changes
22-Jul-2013	1	Initial release.
06-Sep-2013	2	Updated <a href="#">Section 1.2: STM8 motherboard</a>
16-Sep-2013	3	Updated disclaimer.

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