



# STB11N52K3, STF11N52K3 STP11N52K3

N-channel 525 V, 0.41  $\Omega$ , 10 A SuperMESH3™ Power MOSFET  
in D<sup>2</sup>PAK, TO-220FP and TO-220 packages

Datasheet — production data

## Features

Order codes	V <sub>DSS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>	P <sub>w</sub>
STB11N52K3	525 V	< 0.51 $\Omega$	10 A	125 W
STF11N52K3				30 W
STP11N52K3				125 W

- 100% avalanche tested
- Extremely high dv/dt capability
- Gate charge minimized
- Very low intrinsic capacitance
- Improved diode reverse recovery characteristics
- Zener-protected

## Applications

- Switching applications

## Description

These devices are N-channel Power MOSFETs made using the SuperMESH3™ technology that is obtained via improvements applied to STMicroelectronics' SuperMESH™ technology combined with a new optimized vertical structure. The resulting transistor has an extremely low on resistance, superior dynamic performance and high avalanche capability, making it especially suitable for the most demanding applications.

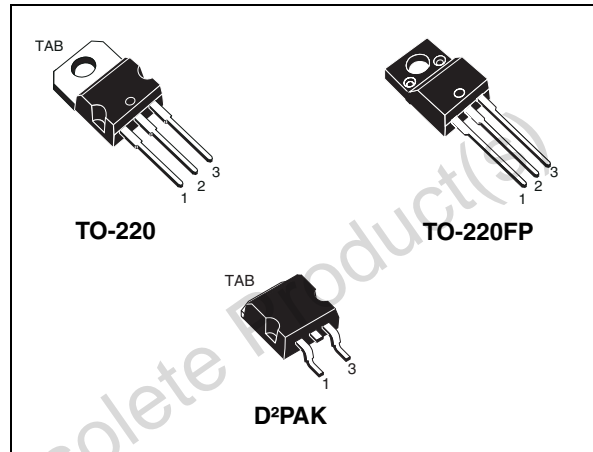


Figure 1. Internal schematic diagram

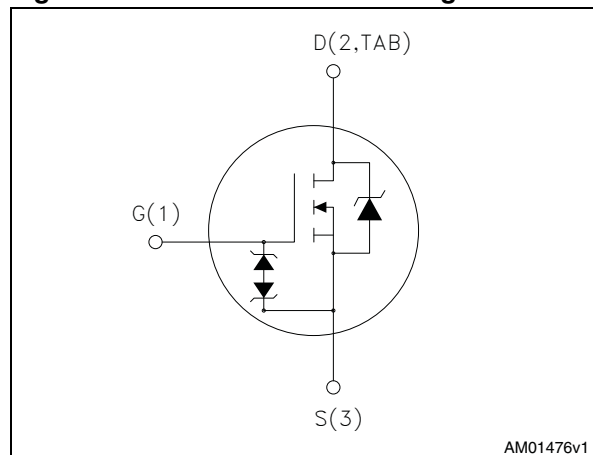


Table 1. Device summary

Order codes	Marking	Packages	Packaging
STB11N52K3	11N52K3	D <sup>2</sup> PAK	Tape and reel
STF11N52K3		TO-220FP	Tube
STP11N52K3		TO-220	Tube

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value		Unit
		TO-220, D <sup>2</sup> PAK	TO-220FP	
V <sub>DS</sub>	Drain- source voltage	525		V
V <sub>GS</sub>	Gate- source voltage	± 30		V
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 25 °C	10	10 <sup>(1)</sup>	A
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 100 °C	6	6 <sup>(1)</sup>	A
I <sub>DM</sub> <sup>(2)</sup>	Drain current (pulsed)	40	40 <sup>(1)</sup>	A
P <sub>TOT</sub>	Total dissipation at T <sub>C</sub> = 25 °C	125	30	W
I <sub>AR</sub>	Avalanche current, repetitive or not-repetitive (pulse width limited by T <sub>J</sub> max)	5		A
E <sub>AS</sub>	Single pulse avalanche energy (starting T <sub>J</sub> = 25 °C, I <sub>D</sub> = I <sub>AR</sub> , V <sub>DD</sub> = 50 V)	170		mJ
V <sub>ESD(G-S)</sub>	Gate source ESD(HBM-C = 100 pF, R = 1.5 kΩ)	2500		V
dv/dt <sup>(3)</sup>	Peak diode recovery voltage slope	12		V/ns
V <sub>ISO</sub>	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; T <sub>C</sub> = 25 °C)	2500		
T <sub>J</sub> T <sub>stg</sub>	Operating junction temperature Storage temperature	- 55 to 150		°C

1. Limited only by maximum temperature allowed
2. Pulse width limited by safe operating area
3. I<sub>SD</sub> ≤ 10 A, di/dt ≤ 400 A/μs, V<sub>DD</sub> = 80% V<sub>(BR)DSS</sub>

**Table 3. Thermal data**

Symbol	Parameter	Value			Unit
		TO-220	TO-220FP	D <sup>2</sup> PAK	
R <sub>thj-case</sub>	Thermal resistance junction-case max	1	4.17	1	°C/W
R <sub>thj-amb</sub>	Thermal resistance junction-amb max	62.50			°C/W
R <sub>thj-pcb</sub>	Thermal resistance junction-pcb max	30			°C/W
T <sub>J</sub>	Maximum lead temperature for soldering purpose	300			°C/W

## 2 Electrical characteristics

(T<sub>case</sub> = 25 °C unless otherwise specified)

**Table 4. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage	I <sub>D</sub> = 1 mA, V <sub>GS</sub> = 0	525			V
I <sub>DSS</sub>	Zero gate voltage drain current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = 525 V V <sub>DS</sub> = 525 V, T <sub>C</sub> = 125 °C			1 50	μA μA
I <sub>GSS</sub>	Gate-body leakage current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ± 20 V; V <sub>DS</sub> = 0			±10	μA
V <sub>GS(th)</sub>	Gate threshold voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 50 μA	3	3.75	4.5	V
R <sub>DS(on)</sub>	Static drain-source on resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 5 A		0.41	0.51	Ω

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C <sub>iss</sub>	Input capacitance	V <sub>DS</sub> = 50 V, f = 1 MHz, V <sub>GS</sub> = 0	-	1400	-	pF
C <sub>oss</sub>	Output capacitance			110		pF
C <sub>rss</sub>	Reverse transfer capacitance			22		pF
C <sub>oss eq.</sub> (1)	Equivalent output capacitance			V <sub>DS</sub> = 0 to 420 V, V <sub>GS</sub> = 0		83
R <sub>g</sub>	Gate input resistance	f = 1 MHz open drain	1	3	7	Ω
Q <sub>g</sub>	Total gate charge	V <sub>DD</sub> = 420 V, I <sub>D</sub> = 10 A,	-	51	-	nC
Q <sub>gs</sub>	Gate-source charge	V <sub>GS</sub> = 10 V		8		nC
Q <sub>gd</sub>	Gate-drain charge	(see Figure 18)		32		nC

1. C<sub>oss eq.</sub> is defined as a constant equivalent capacitance giving the same charging time as C<sub>oss</sub> when V<sub>DS</sub> increases from 0 to 80% V<sub>DS</sub>

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
t <sub>d(on)</sub>	Turn-on delay time	V <sub>DD</sub> = 210 V, I <sub>D</sub> = 5 A, R <sub>G</sub> = 4.7 Ω, V <sub>GS</sub> = 10 V (see Figure 17)	-	7	-	ns
t <sub>r</sub>	Rise time			18		ns
t <sub>d(off)</sub>	Turn-off-delay time			281		ns
t <sub>f</sub>	Fall time			42		ns

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$I_{SD}$	Source-drain current		-		10	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		40	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 10 \text{ A}, V_{GS} = 0$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 10 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$	-	270		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 60 \text{ V}$	-	2700		nC
$I_{RRM}$	Reverse recovery current	(see Figure 19)		20		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 10 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$	-	320		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 60 \text{ V } T_J = 150 \text{ }^\circ\text{C}$	-	3400		nC
$I_{RRM}$	Reverse recovery current	(see Figure 19)		22		A

1. Pulse width limited by safe operating area

2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

**Table 8. Gate-source Zener diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$BV_{GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1 \text{ mA}$ (open drain)	30	-	-	V

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220, D<sup>2</sup>PAK

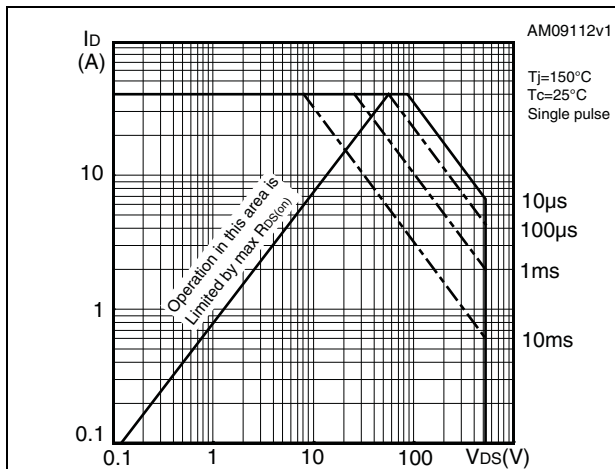


Figure 3. Thermal impedance for TO-220, D<sup>2</sup>PAK

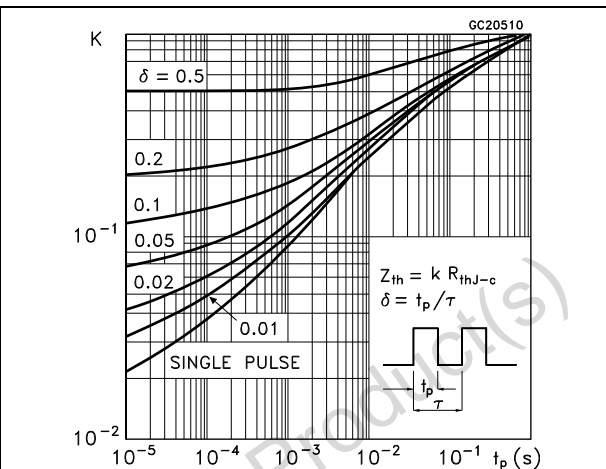


Figure 4. Safe operating area for TO-220FP

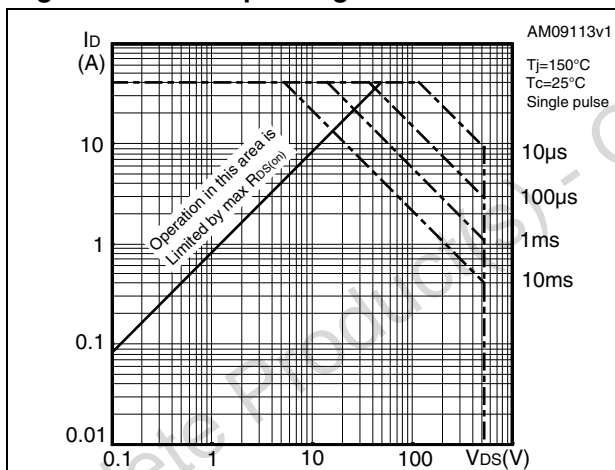


Figure 5. Thermal impedance for TO-220FP

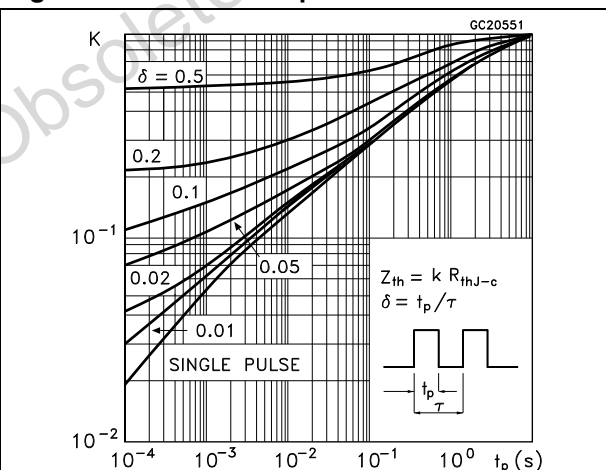


Figure 6. Output characteristics

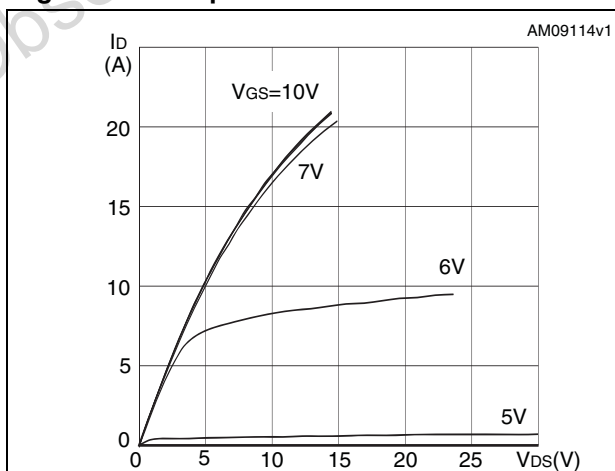


Figure 7. Transfer characteristics

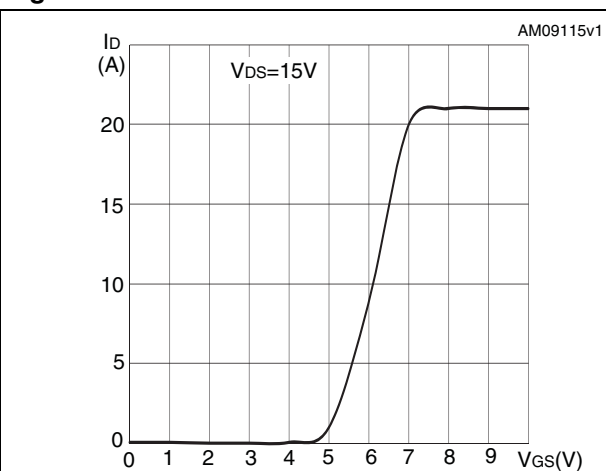


Figure 8. Gate charge vs gate-source voltage Figure 9. Static drain-source on resistance

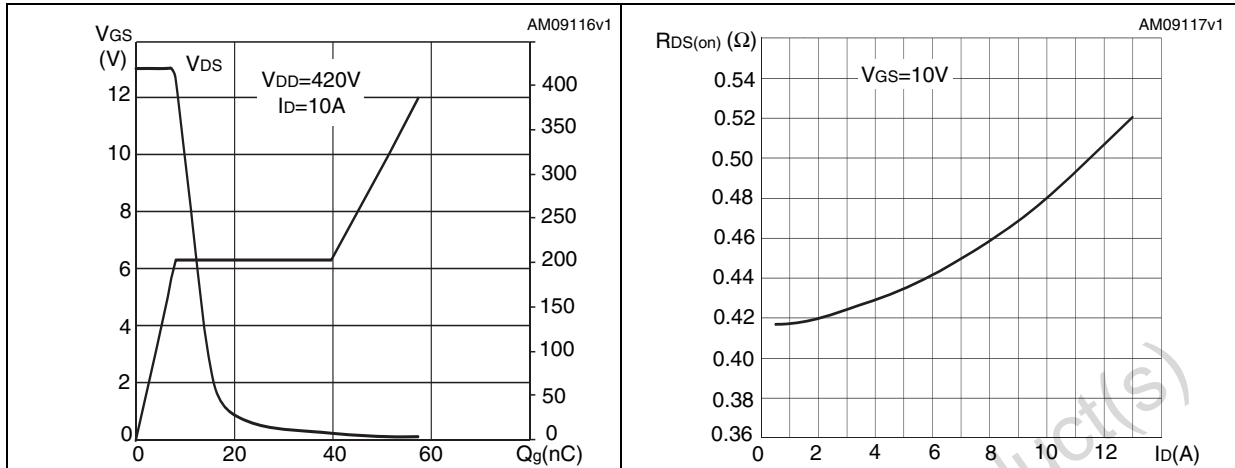


Figure 10. Capacitance variations Figure 11. Output capacitance stored energy

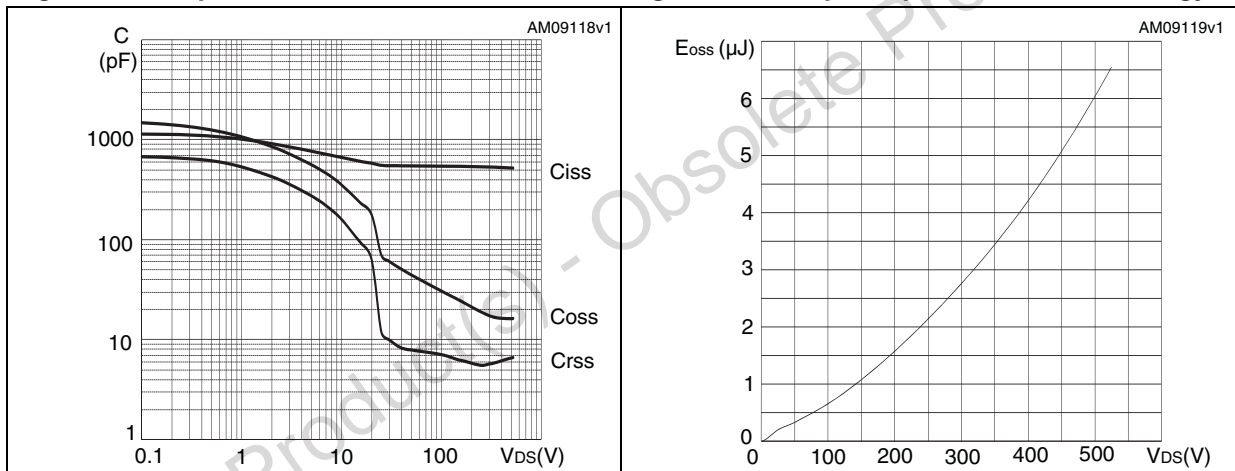


Figure 12. Normalized gate threshold voltage vs temperature Figure 13. Normalized on resistance vs temperature

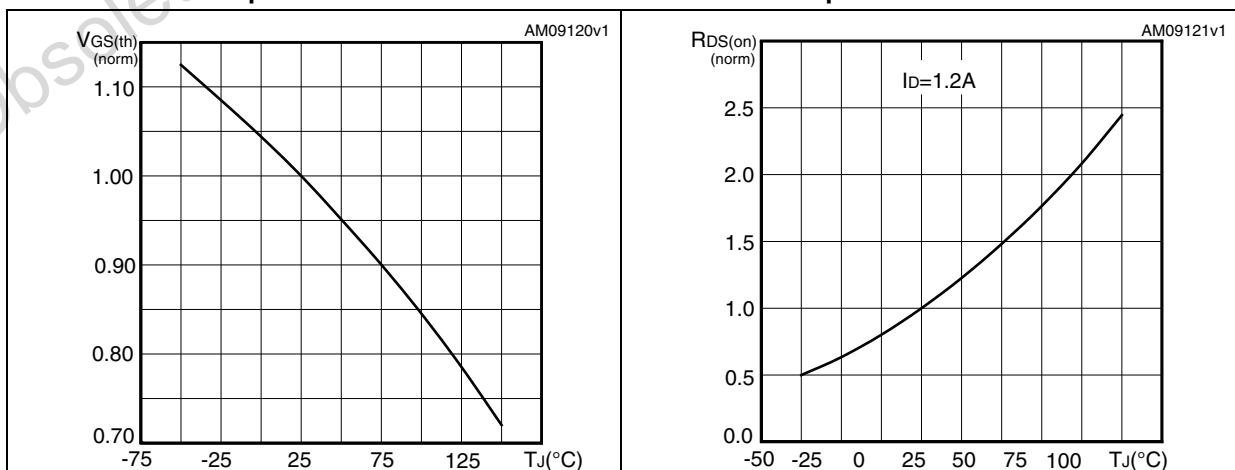


Figure 14. Source-drain diode forward characteristics

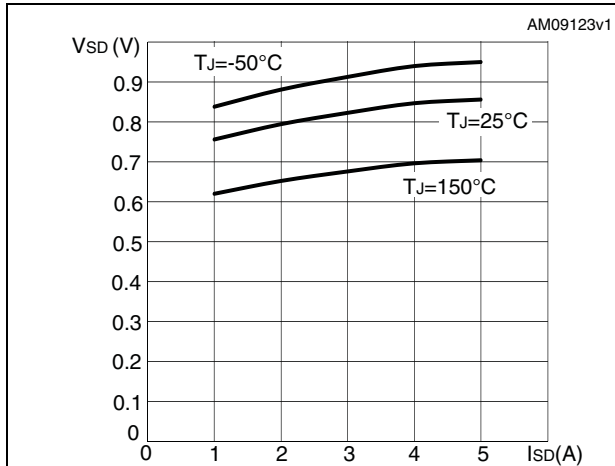


Figure 15. Normalized BV<sub>DSS</sub> vs temperature

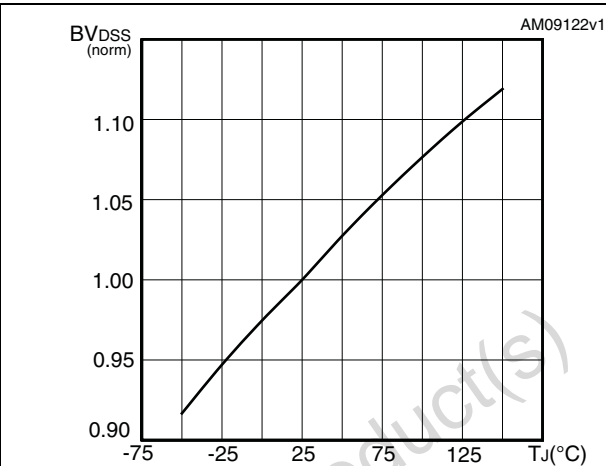
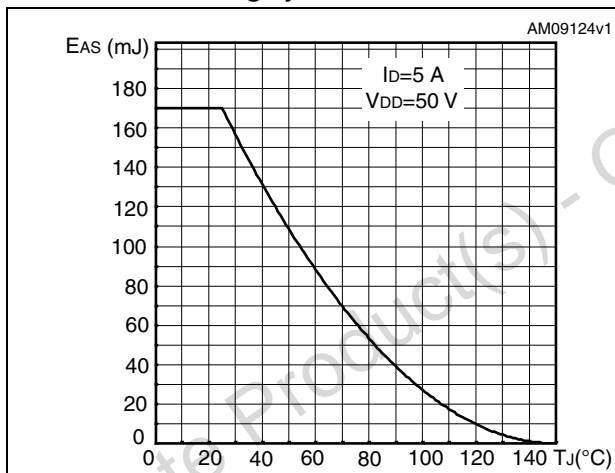


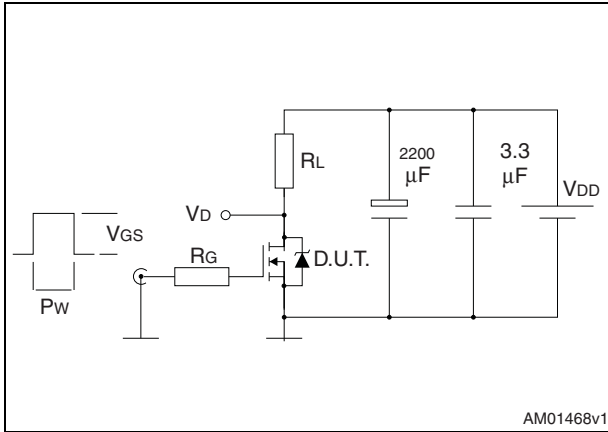
Figure 16. Maximum avalanche energy vs starting Tj





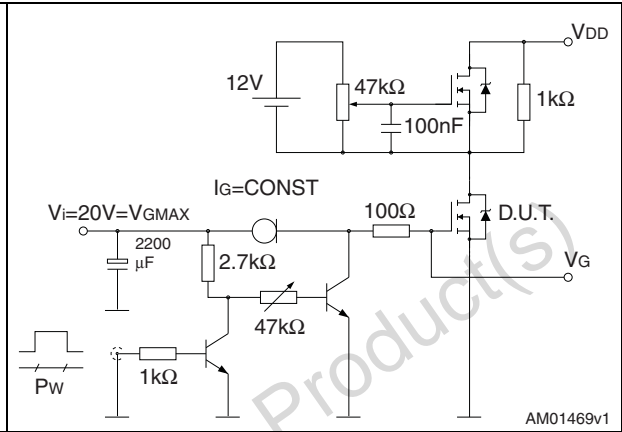
### 3 Test circuits

**Figure 17. Switching times test circuit for resistive load**



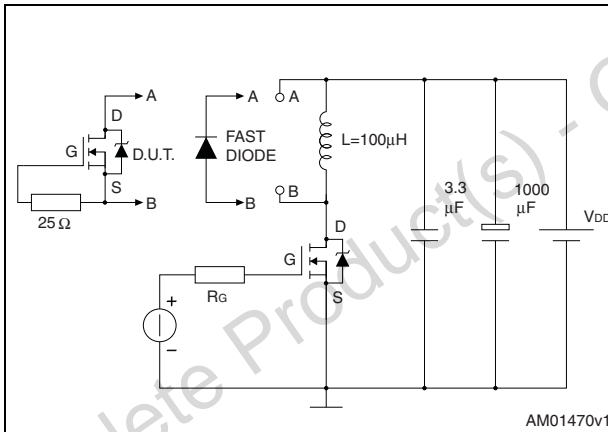
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**Figure 18. Gate charge test circuit**



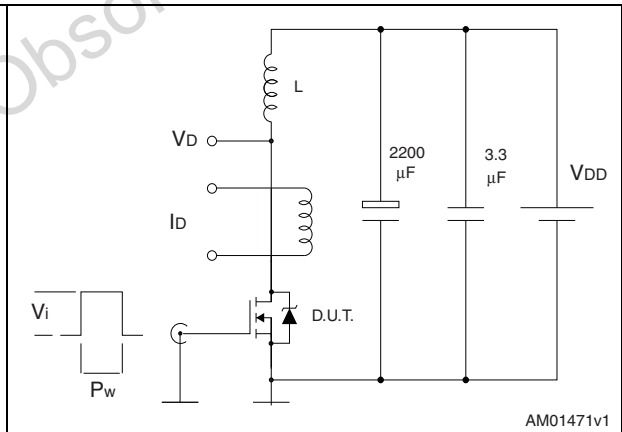
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**Figure 19. Test circuit for inductive load switching and diode recovery times**



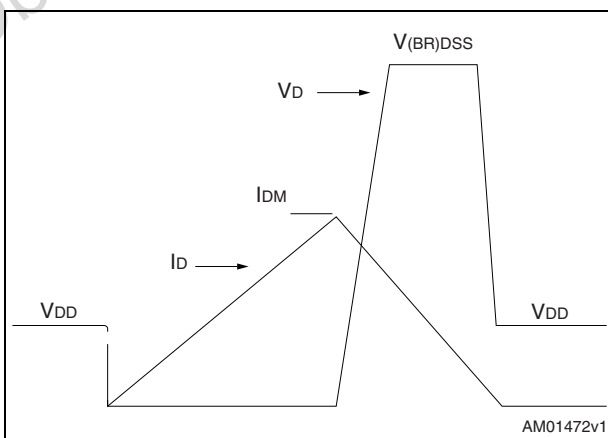
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**Figure 20. Unclamped inductive load test circuit**



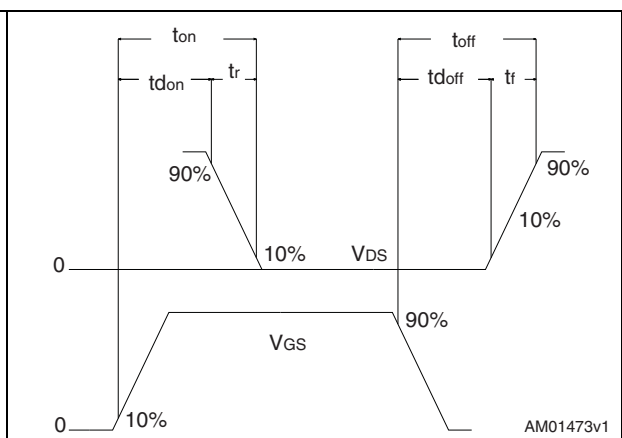
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**Figure 21. Unclamped inductive waveform**



AM01472v1

**Figure 22. Switching time waveform**



AM01473v1

## 4 Package mechanical data

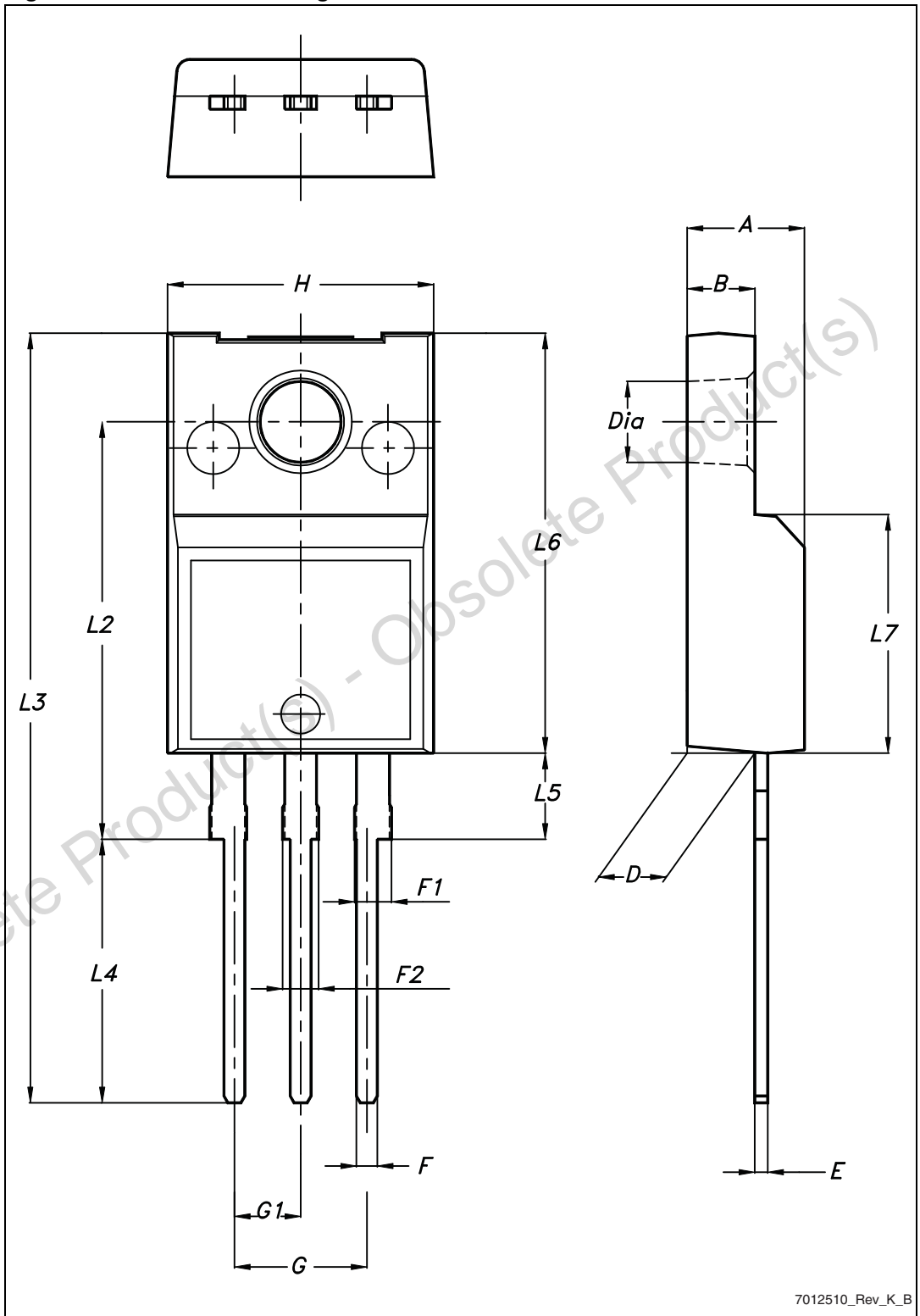
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Table 9. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Figure 23. TO-220FP drawing



7012510\_Rev\_K\_B

Table 10. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
ØP	3.75		3.85
Q	2.65		2.95

Figure 24. TO-220 type A drawing

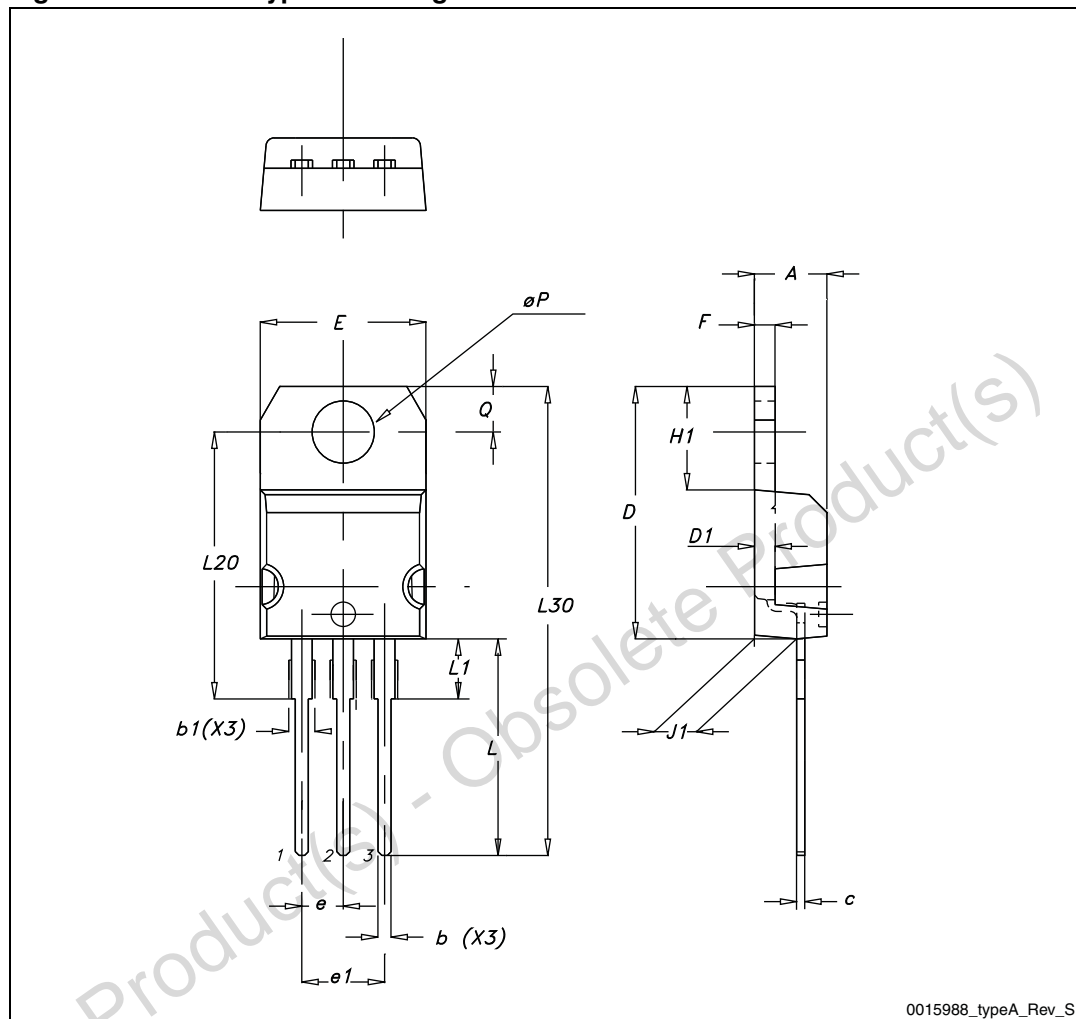


Table 11. D<sup>2</sup>PAK (TO-263) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50		
E	10		10.40
E1	8.50		
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

Figure 25. D<sup>2</sup>PAK (TO-263) drawing

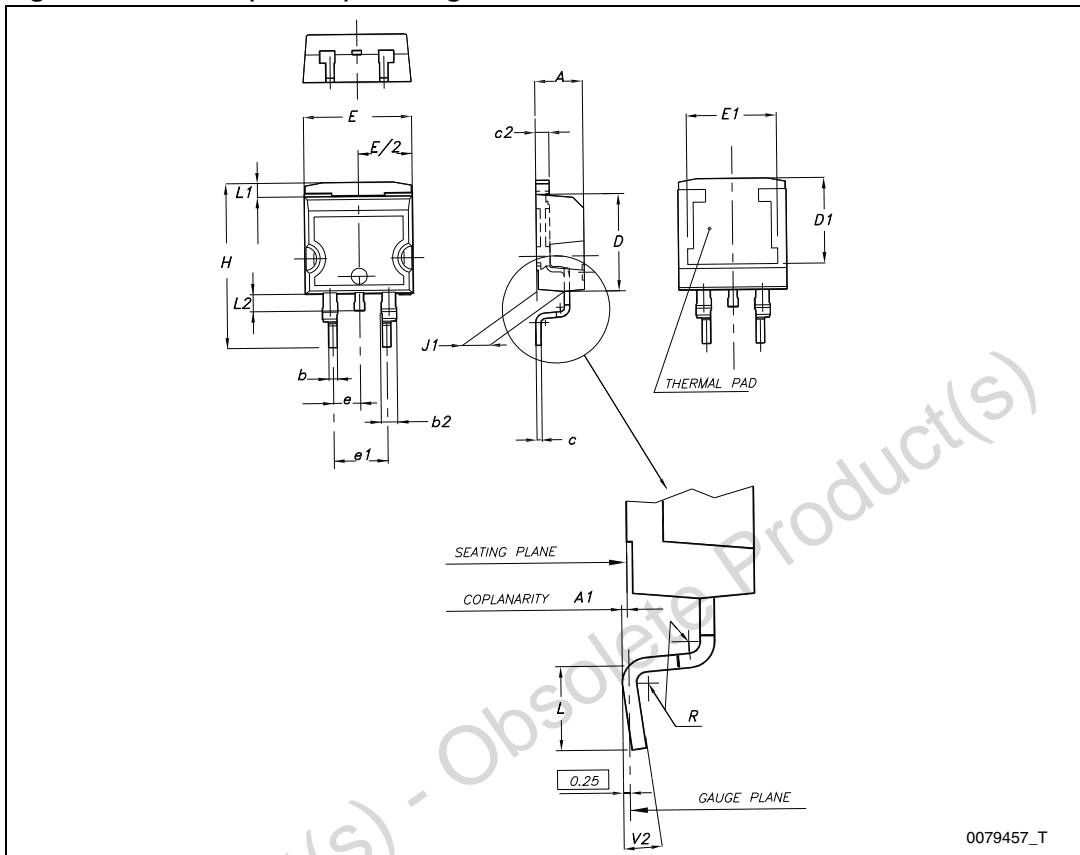
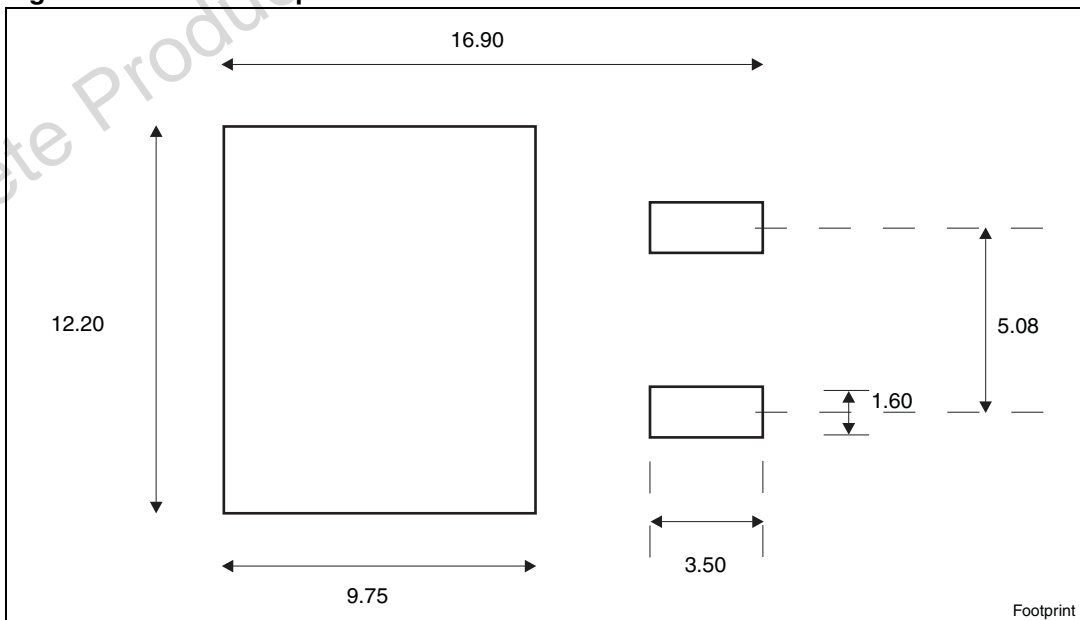


Figure 26. D<sup>2</sup>PAK footprint<sup>(a)</sup>



a. All dimension are in millimeters



## 5 Package mechanical data

Table 12. D<sup>2</sup>PAK (TO-263) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1		Base qty	1000
P2	1.9	2.1		Bulk qty	1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

Figure 27. Tape for D<sup>2</sup>PAK (TO-263)

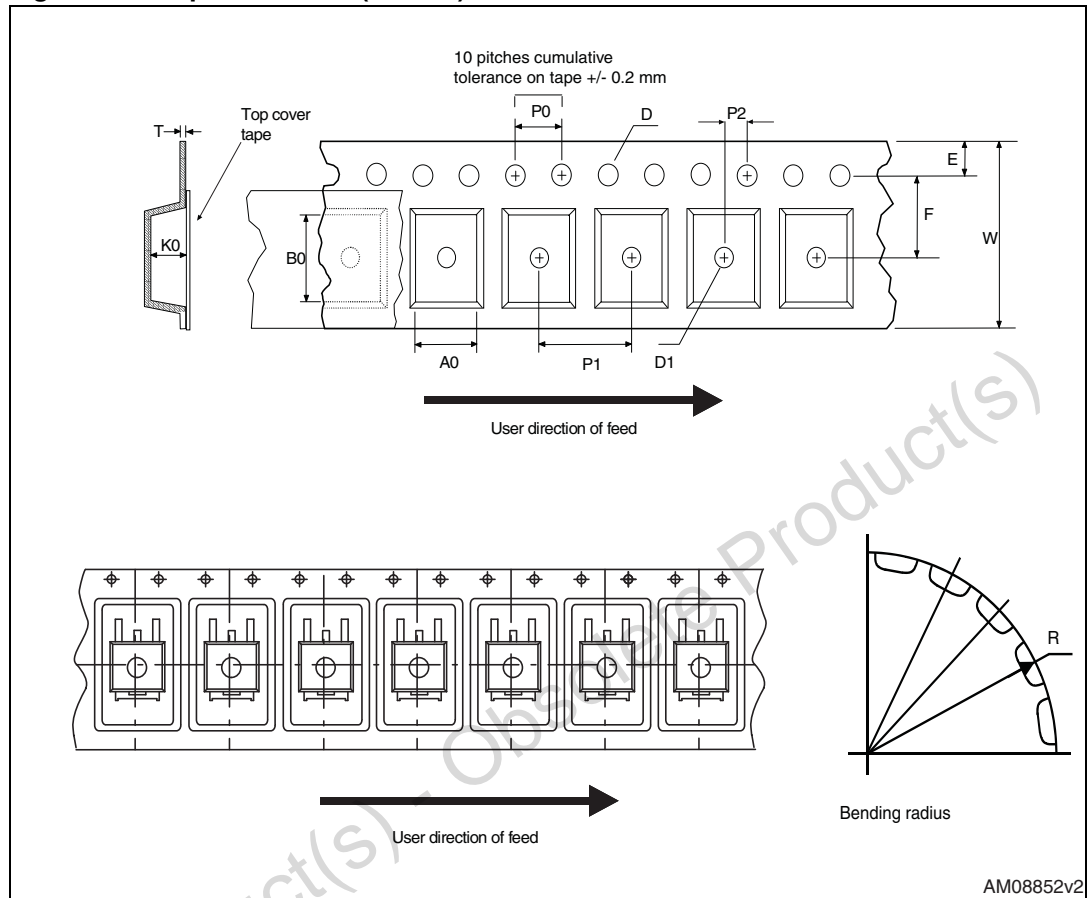
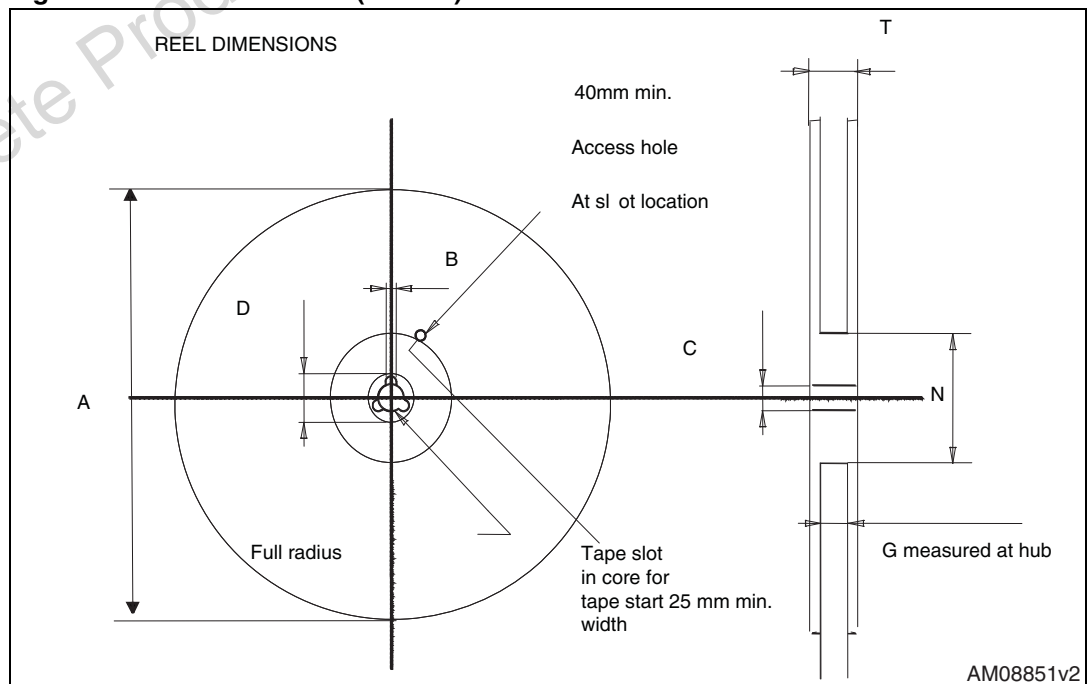


Figure 28. Reel for D<sup>2</sup>PAK (TO-263)



## 6 Revision history

Table 13. Document revision history

Date	Revision	Changes
20-May-2011	1	First release.
27-Mar-2012	2	Inserted max and min. values for $R_G$ in <a href="#">Table 5</a> . Updated <a href="#">Section 4: Package mechanical data</a> .

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