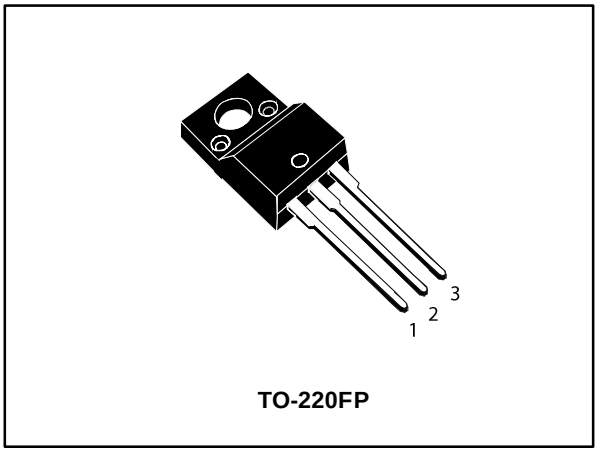
STF11NM50N

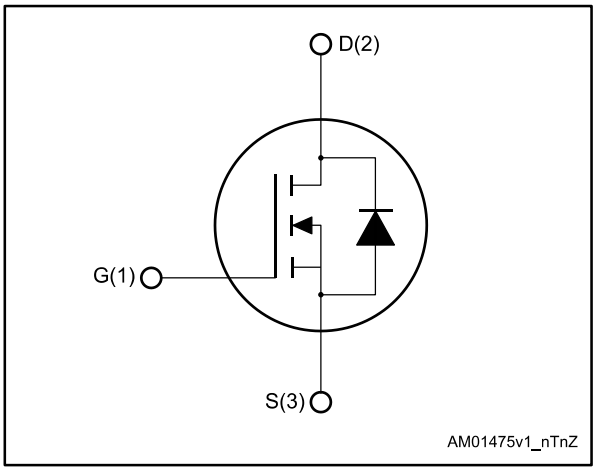
N-channel 500 V, 0.40 Ω typ., 8.5 A MDmesh™ II Power MOSFET in a TO-220FP package

Datasheet - production data



TO-220FP

Figure 1: Internal schematic diagram



Features

Order code	V_{DS} @ T_J max	$R_{DS(on)}$ max	I_D
STF11NM50N	550 V	0.47 Ω	8.5 A

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

Table 1: Device summary

Order code	Marking	Package	Packaging
STF11NM50N	11NM50N	TO-220FP	Tube

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	500	V
V_{GS}	Gate-source voltage	±25	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	8.5	A
I_D (1)	Drain current (continuous) at T_C = 100 °C	6	A
I_{DM} (1)(2)	Drain current (pulsed)	34	A
P_{TOT}	Total dissipation at T_C = 25 °C	25	W
dv/dt (3)	Peak diode recovery voltage slope	15	V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; T_C = 25 °C)	2500	V
T_{stg}	Storage temperature range	-55 to 150	°C
T_j	Operating junction temperature range		

Notes:

(1)Limited by maximum junction temperature

(2)Pulse width limited by safe operating area.

(3)I_{SD} ≤ 8.5 A, di/dt ≤ 400 A/µs, $V_{DS(peak)}$ ≤ $V_{(BR)DSS}$, V_{DD} ≤ 80% $V_{(BR)DSS}$

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	5	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient max	62.5	°C/W

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_{j\ max}$)	3	A
E_{AS}	Single pulse avalanche energy (starting T_J=25 °C, I_D=I_{AR}, V_{DD}=50 V)	150	mJ

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 5: On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0 V	500			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 500 V			1	µA
		V_{GS} = 0 V, V_{DS} = 500 V, T_C= 125 °C (1)			100	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 4.5 A		0.40	0.47	Ω

Notes:

(1)Defined by design, not subject to production test.

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 50 V, f = 1 MHz, V_{GS} = 0 V	-	547	-	pF
C_{oss}	Output capacitance		-	42	-	pF
C_{rss}	Reverse transfer capacitance		-	2	-	pF
$C_{oss\ eq.}$ (1)	Equivalent output capacitance	V_{GS} = 0 V, V_{DS} = 0 to 400 V	-	210	-	pF
Q_g	Total gate charge	V_{DD} = 400 V, I_D = 8.5 A, V_{GS} = 10 V (see *Figure 14: "Test circuit for gate charge behavior"*	-	19	-	nC
Q_{gs}	Gate-source charge		-	3.7	-	nC
Q_{gd}	Gate-drain charge		-	10	-	nC
R_G	Gate input resistance	f=1 MHz, I_D=0 A	-	5.8	-	Ω

Notes:

(1)$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DS}

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 250 V, I_D = 4.25 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 13: "Test circuit for resistive load switching times"* and *Figure 18: "Switching time waveform"*)	-	8	-	ns
t_r	Rise time		-	10	-	ns
$t_{d(off)}$	Turn-off delay time		-	33	-	ns
t_f	Fall time		-	10	-	ns

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}(1) I_{SDM}	Source-drain current Source-drain current (pulsed)		-		8.5 34	A A
V_{SD}(2)	Forward on voltage	I_{SD} = 8.5 A, V_{GS} = 0 V	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 8.5 A, di/dt = 100 A/µs V_{DD} = 60 V (see *Figure 15: "Test circuit for inductive load switching and diode recovery times"*)	-	230		ns
Q_{rr}	Reverse recovery charge		-	2.1		µC
I_{RRM}	Reverse recovery current		-	18		A
t_{rr}	Reverse recovery time	I_{SD} = 8.5 A, di/dt = 100 A/µs V_{DD} = 60 V, T_j = 150 °C (see *Figure 15: "Test circuit for inductive load switching and diode recovery times"*)	-	275		ns
Q_{rr}	Reverse recovery charge		-	2.5		µC
I_{RRM}	Reverse recovery current		-	18		A

Notes:

(1)Pulse width limited by safe operating area.

(2)Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

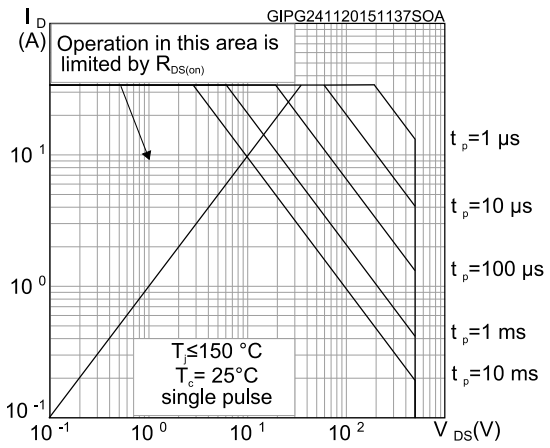


Figure 3: Thermal impedance

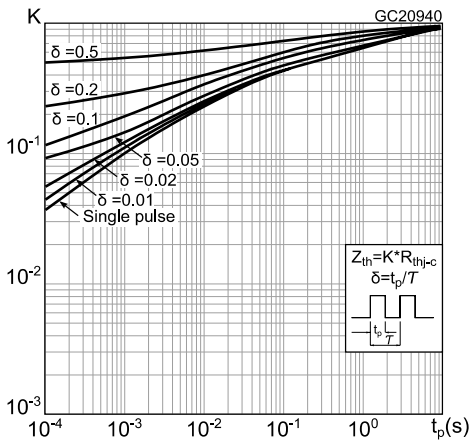


Figure 4: Output characteristics

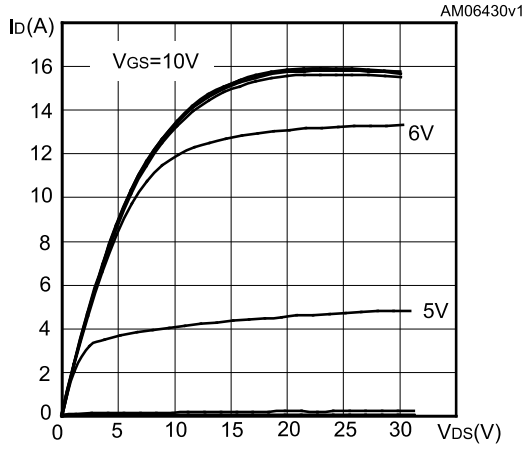


Figure 5: Transfer characteristics

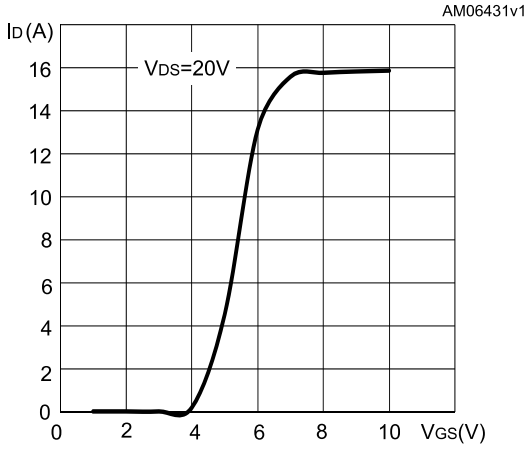


Figure 6: Gate charge vs gate-source voltage

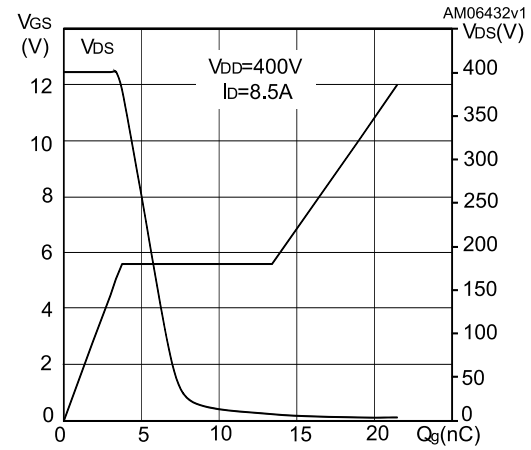


Figure 7: Static drain-source on resistance

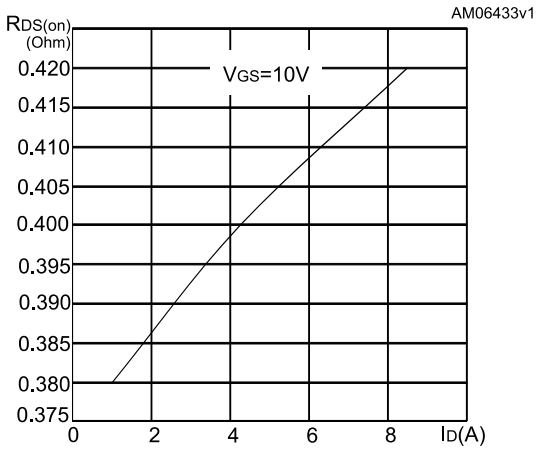


Figure 8: Capacitance variations

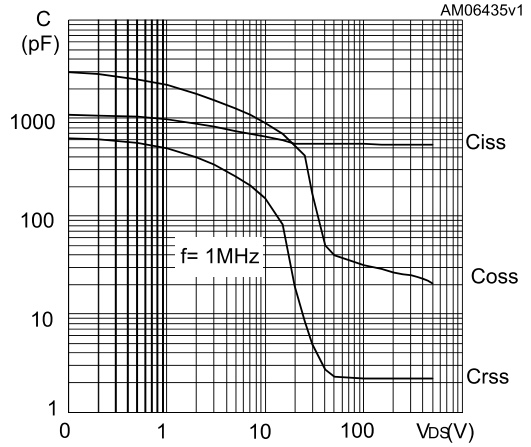


Figure 9: Output capacitance stored energy

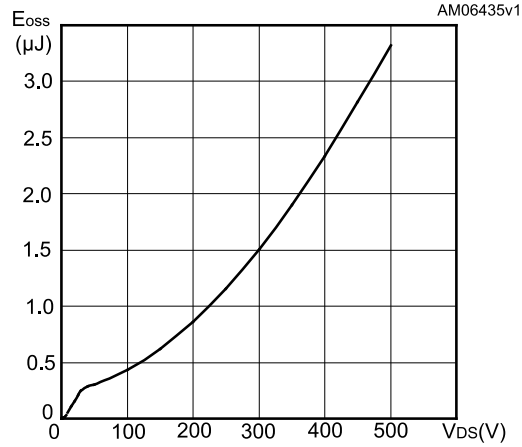


Figure 10: Normalized gate threshold voltage vs temperature

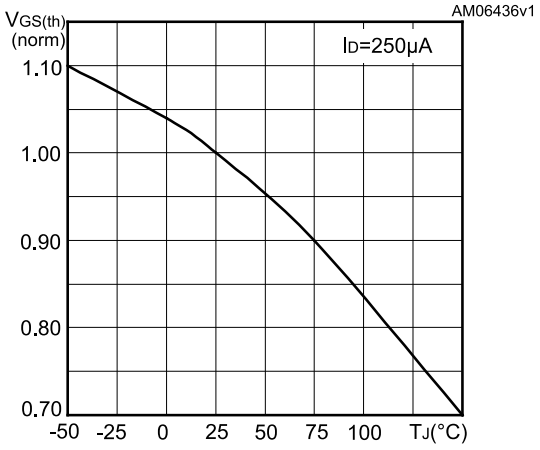


Figure 11: Normalized on-resistance vs temperature

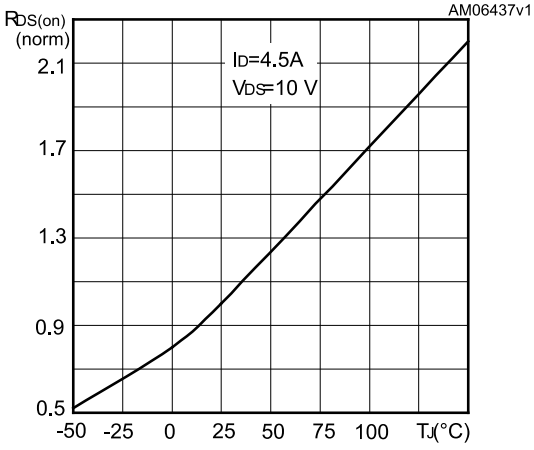
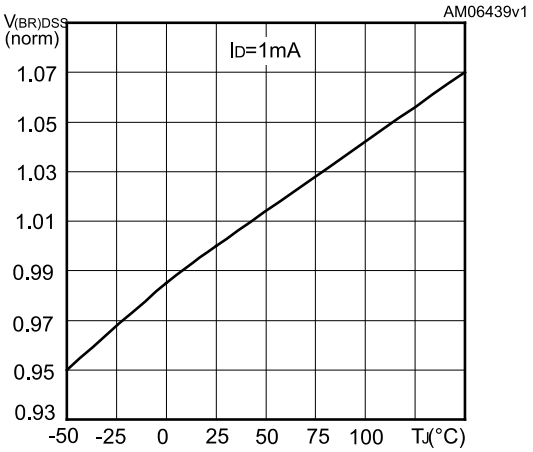


Figure 12: Normalized V(BR)DSS vs temperature



3 Test circuits

Figure 13: Test circuit for resistive load switching times

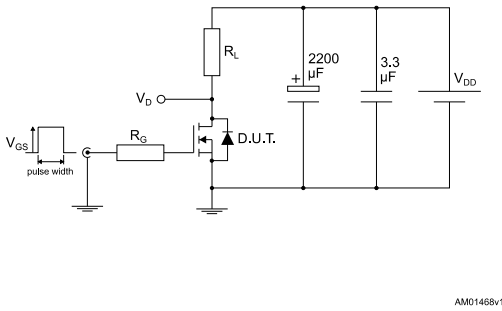


Figure 14: Test circuit for gate charge behavior

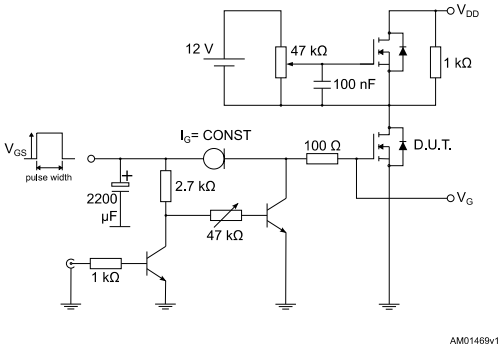


Figure 15: Test circuit for inductive load switching and diode recovery times

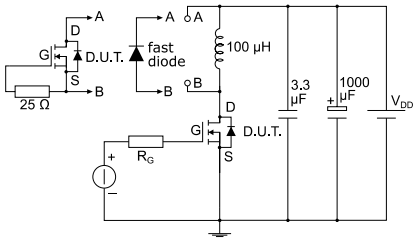


Figure 16: Unclamped inductive load test circuit

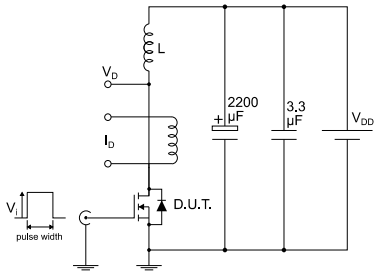


Figure 17: Unclamped inductive waveform

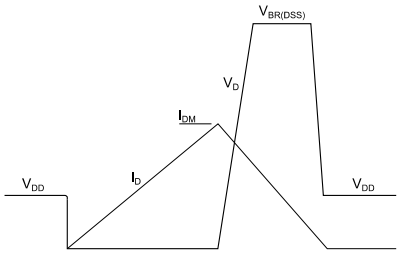
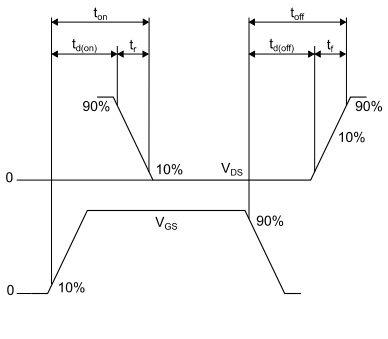


Figure 18: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 TO-220FP package information

Figure 19: TO-220FP package outline

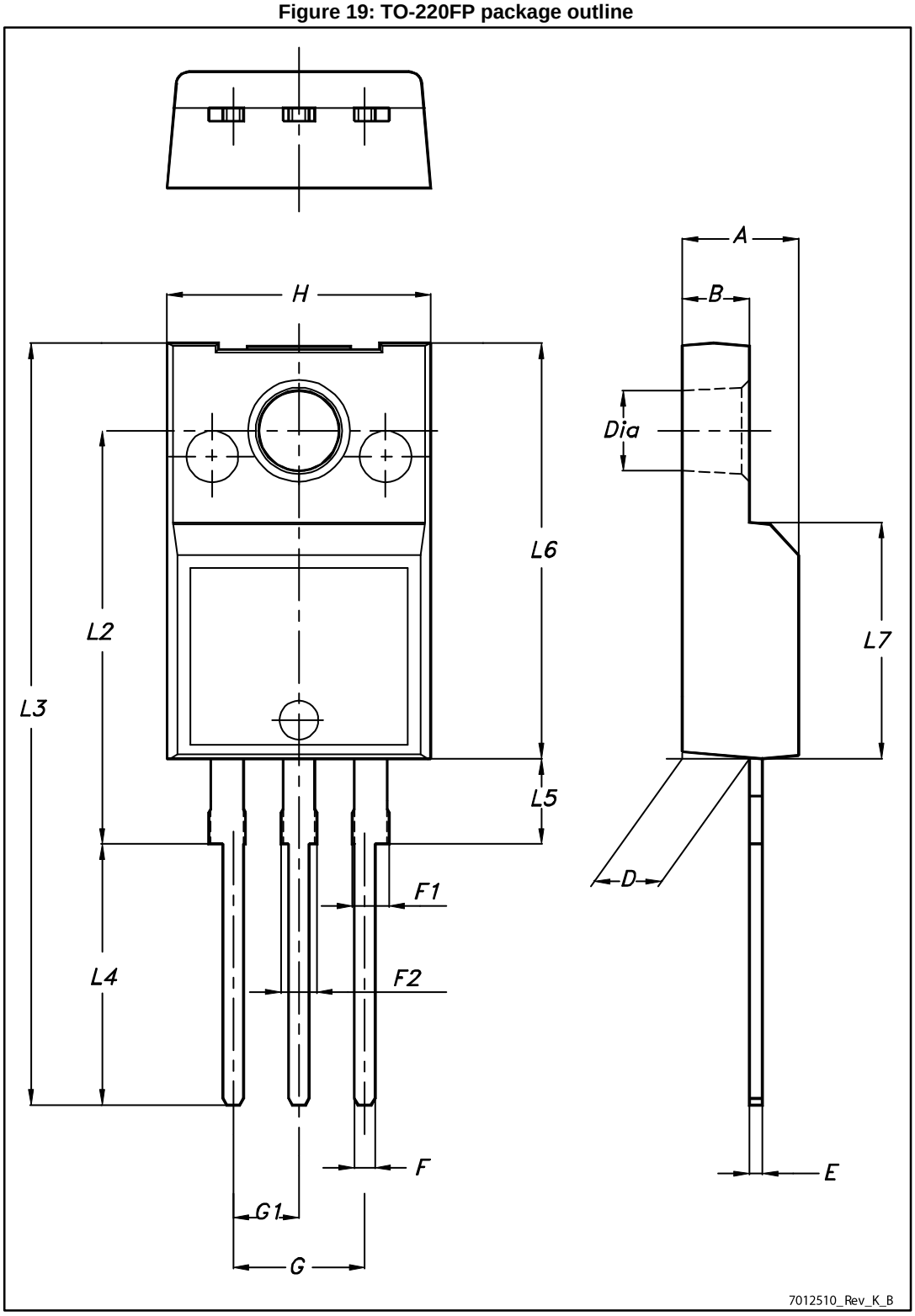


Table 9: TO-220FP package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

5 Revision history

Table 10: Document revision history

Date	Revision	Changes
25-Nov-2015	1	First release. Part number previously included in datasheet DocID17156.
09-Jun-2016	2	Updated I_{GSS} unit from µA to nA in *Table 5: "On/off states"* . Updated *Table 7: "Switching times"* modifying references in test conditions. Document reformatted with the current standard with minor text changes to improve readability.

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