STF19NM50N, STP19NM50N, STW19NM50N

N-channel 500 V, 0.2 Ω typ., 14 A MDmesh™ II Power MOSFETs in TO-220FP, TO-220 and TO-247 packages

Datasheet - production data

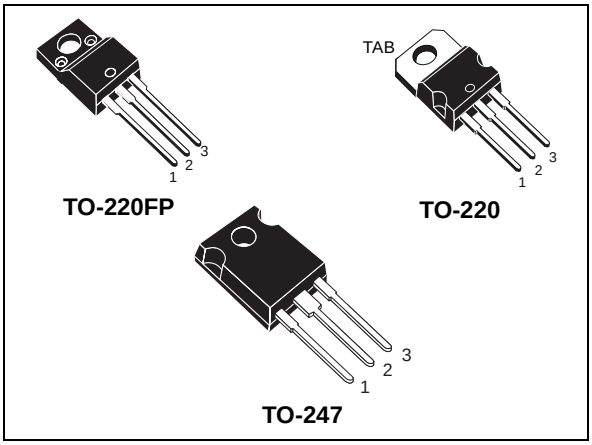
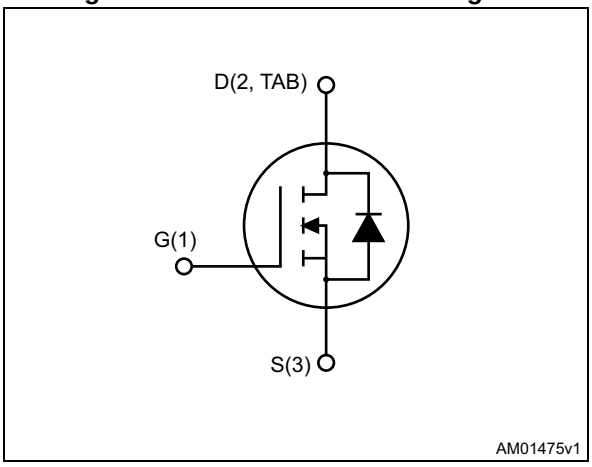


Figure 1. Internal schematic diagram



Features

Order codes	V_{DS} @ T_{Jmax}	$R_{DS(on)}$ max	I_D
STF19NM50N	550 V	0.25 Ω	14 A
STP19NM50N			
STW19NM50N			

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Applications

- Switching applications

Description

These devices are N-channel Power MOSFETs developed using the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

Table 1. Device summary

Order codes	Marking	Packages	Packaging
STF19NM50N	19NM50N	TO-220FP	Tube
STP19NM50N		TO-220	
STW19NM50N		TO-247	

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value			Unit
		TO-220	TO-247	TO-220FP	
V_{DS}	Drain-source voltage	500			V
V_{GS}	Gate-source voltage	± 25			V
I_D	Drain current (continuous) at T_C = 25 °C	14		14 (1)	A
I_D	Drain current (continuous) at T_C = 100 °C	10		10 (1)	A
I_{DM} (2)	Drain current (pulsed)	56		56 (1)	A
P_{TOT}	Total dissipation at T_C = 25 °C	110		30	W
dv/dt (3)	Peak diode recovery voltage slope	15			V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; Tc = 25 °C)			2500	V
T_{stg}	Storage temperature	- 55 to 150			°C
T_j	Max. operating junction temperature	150			°C

1. Limited by maximum junction temperature
2. Pulse width limited by safe operating area
3. $I_{SD} \leq 14$ A, di/dt $\leq$ 400 A/µs, V_{DS} peak $\leq V_{(BR)DSS}$, V_{DD} = 80% $V_{(BR)DSS}$.

Table 3. Thermal data

Symbol	Parameter	Value			Unit
		TO-220	TO-247	TO-220FP	
$R_{thj\text{-}case}$	Thermal resistance junction-case max	1.14		4.17	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient max	62.5	50	62.5	°C/W

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	6	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25°C, $I_D = I_{AR}$, V_{DD} = 50 V)	208	mJ

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 5. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	500			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 500 V V_{DS} = 500 V, T_C=125 °C			1 100	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 25 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 7 A		0.2	0.25	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 50 V, f = 1 MHz, V_{GS} = 0	-	1000	-	pF
C_{oss}	Output capacitance		-	72	-	pF
C_{rss}	Reverse transfer capacitance		-	3	-	pF
$C_{oss\ eq}$ (1)	Equivalent output capacitance	V_{DS} = 0 to 400 V, V_{GS} = 0	-	202	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz, I_D=0	-	4.4	-	Ω
Q_g	Total gate charge	V_{DD} = 400 V, I_D = 14 A, V_{GS} = 10 V (see *Figure 17*)	-	34	-	nC
Q_{gs}	Gate-source charge		-	5	-	nC
Q_{gd}	Gate-drain charge		-	18	-	nC

1. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DS}

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 250 V, I_D = 7 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 18*)	-	12	-	ns
t_r	Rise time		-	16	-	ns
$t_{d(off)}$	Turn-off-delay time		-	61	-	ns
t_f	Fall time		-	17	-	ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		14	A
I_{SDM} (1)	Source-drain current (pulsed)		-		56	A
V_{SD} (2)	Forward on voltage	I_{SD} = 14 A, V_{GS} = 0	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 14 A, di/dt = 100 A/µs V_{DD} = 60 V (see *Figure 21*)	-	296		ns
Q_{rr}	Reverse recovery charge		-	3.5		µC
I_{RRM}	Reverse recovery current		-	23		A
t_{rr}	Reverse recovery time	I_{SD} = 14 A, di/dt = 100 A/µs V_{DD} = 60 V, T_j = 150 °C (see *Figure 21*)	-	346		ns
Q_{rr}	Reverse recovery charge		-	4		µC
I_{RRM}	Reverse recovery current		-	24		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220FP

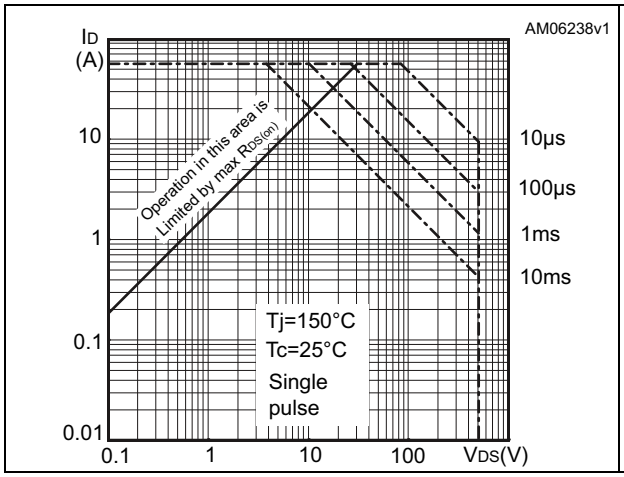


Figure 3. Thermal impedance for TO-220FP

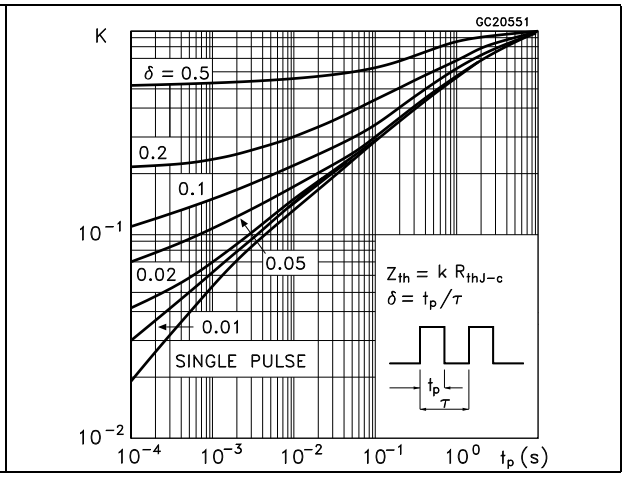


Figure 4. Safe operating area for TO-220

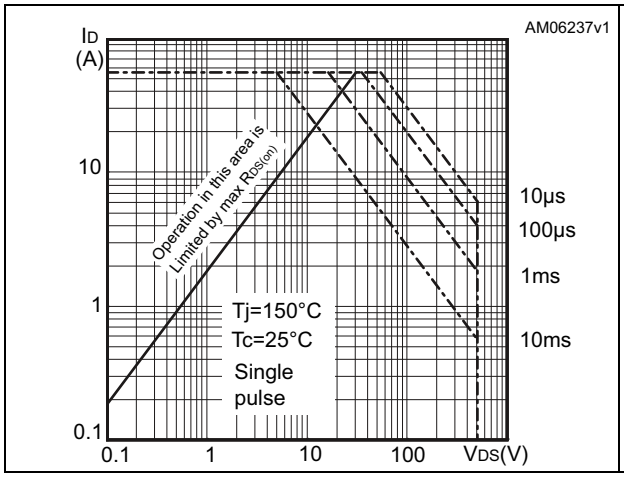


Figure 5. Thermal impedance for TO-220

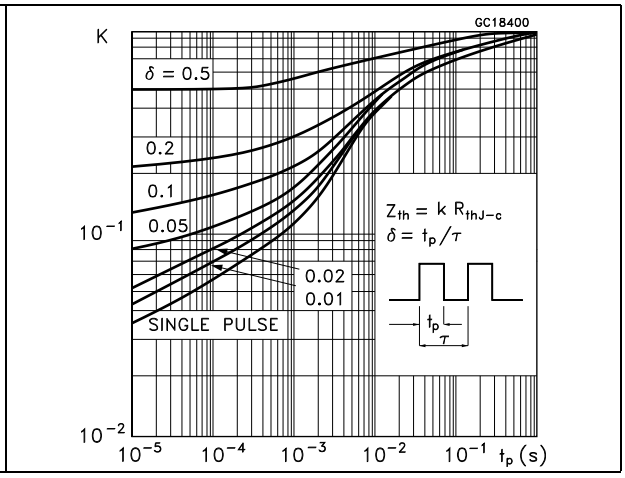


Figure 6. Safe operating area for TO-247

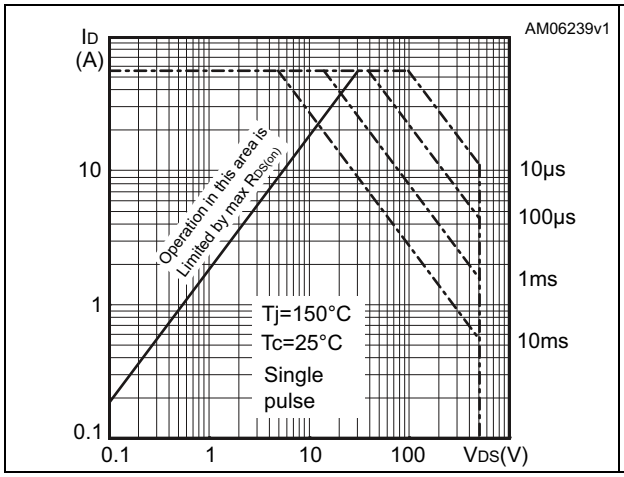


Figure 7. Thermal impedance for TO-247

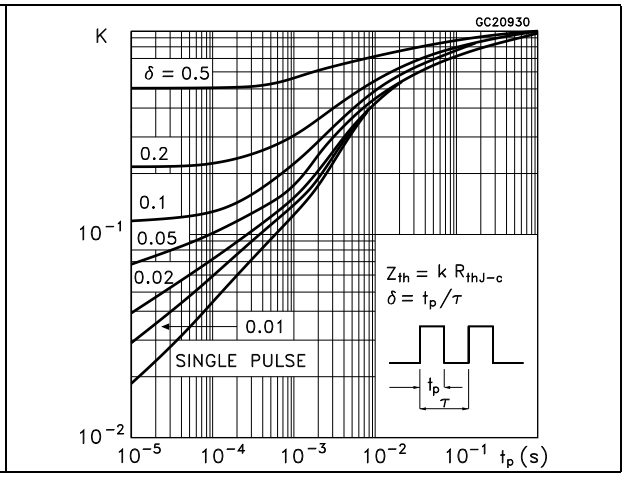


Figure 8. Output characteristics

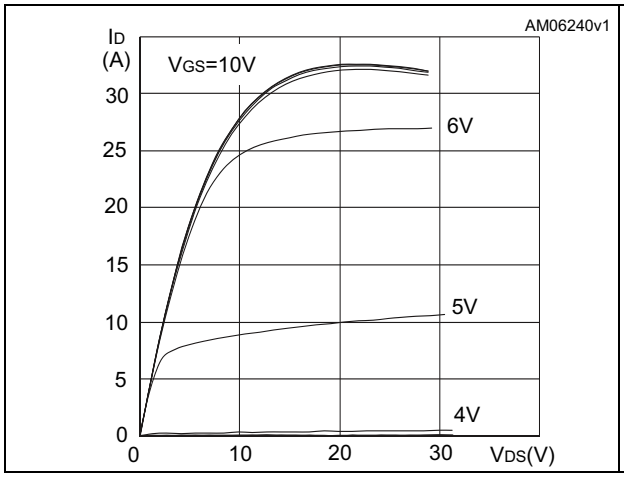


Figure 9. Transfer characteristics

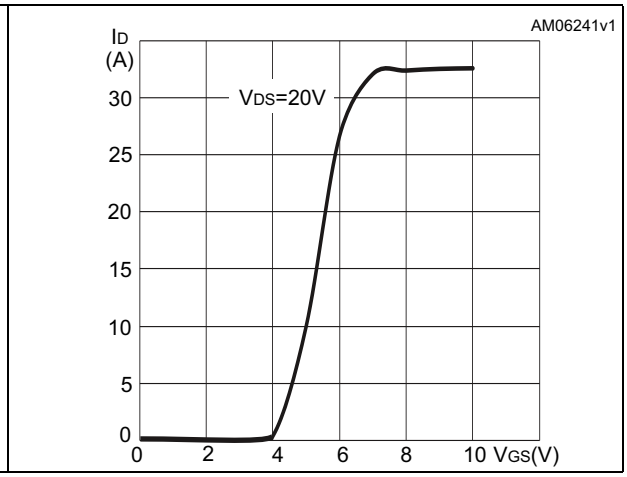


Figure 10. Normalized V_{DS} vs temperature

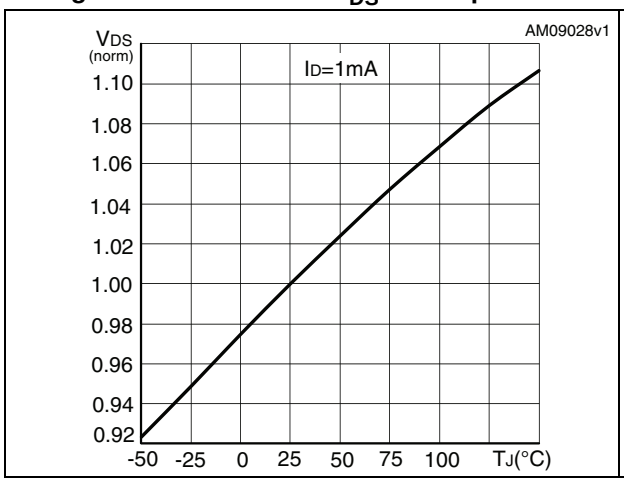


Figure 11. Static drain-source on resistance

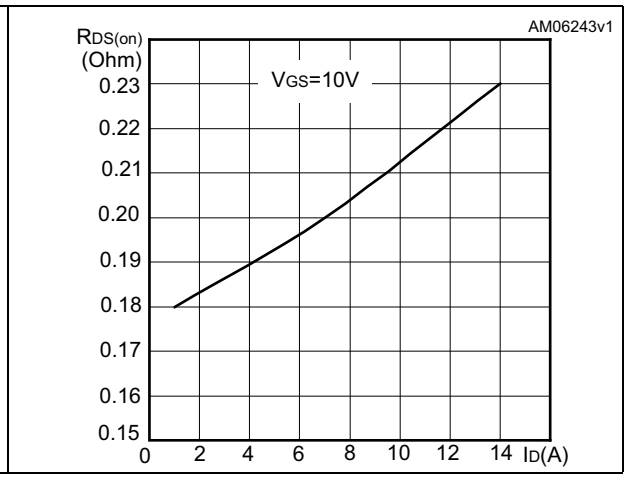


Figure 12. Gate charge vs gate-source voltage

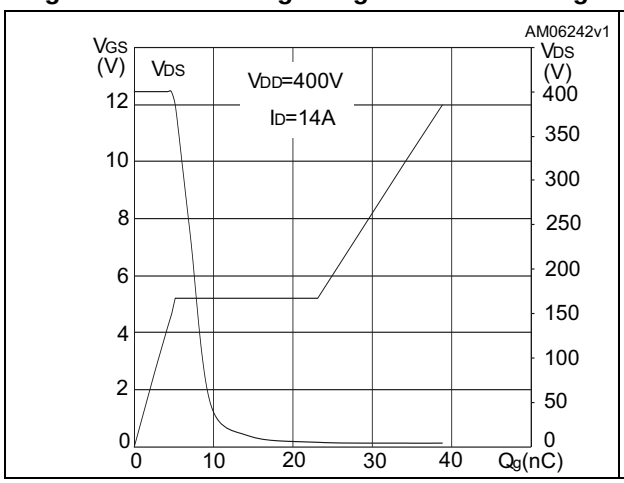


Figure 13. Capacitance variations

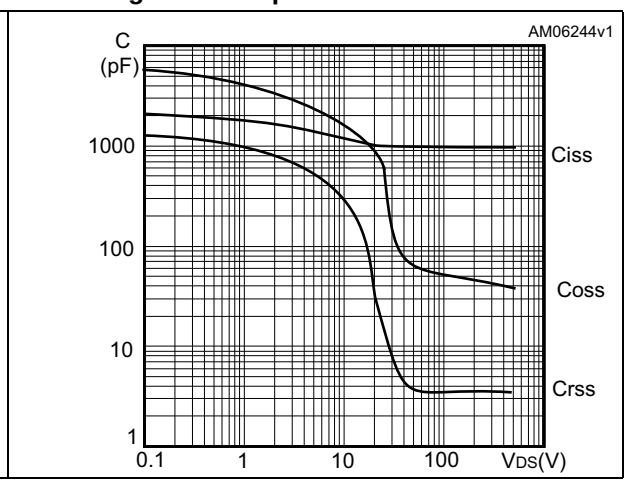


Figure 14. Normalized gate threshold voltage vs temperature

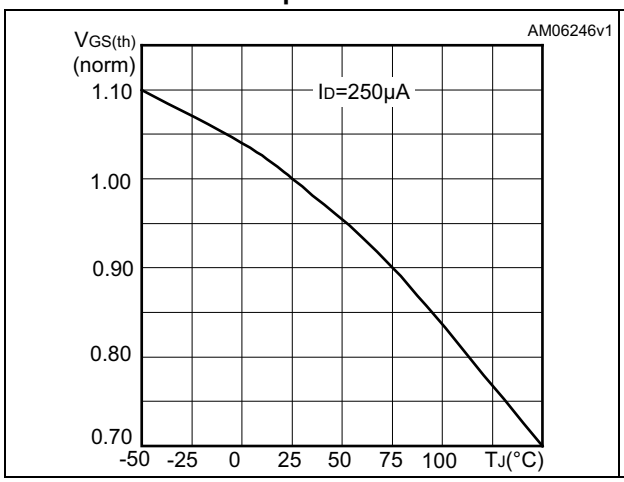
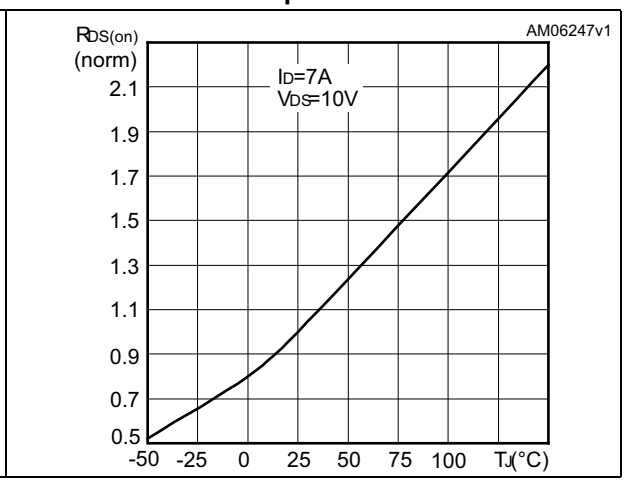


Figure 15. Normalized on-resistance vs temperature



3 Test circuits

Figure 16. Switching times test circuit for resistive load

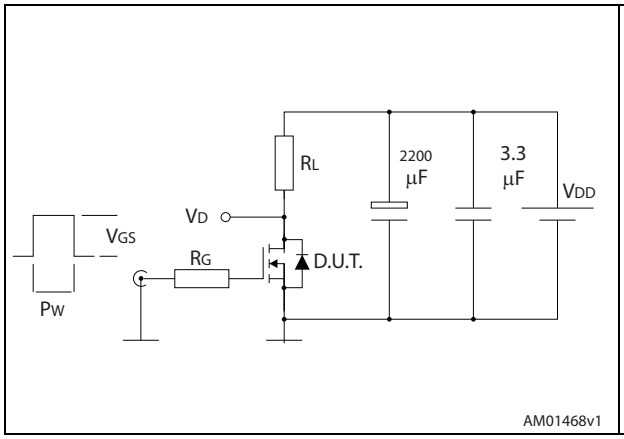


Figure 17. Gate charge test circuit

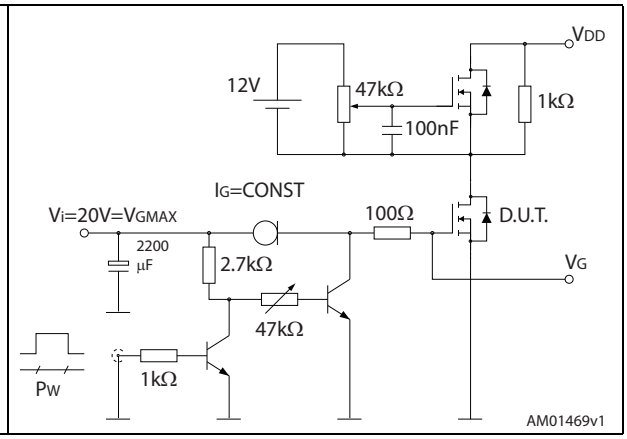


Figure 18. Test circuit for inductive load switching and diode recovery times

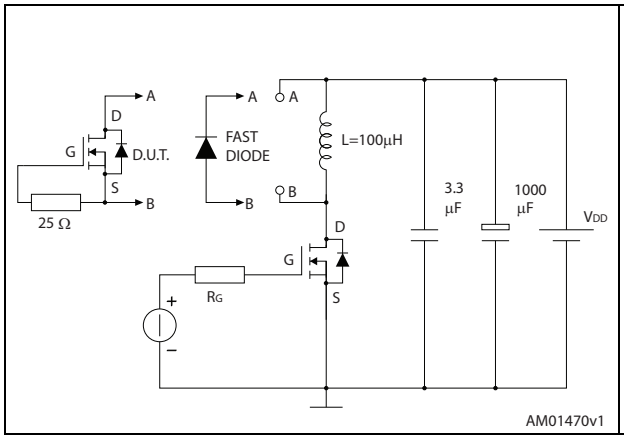


Figure 19. Unclamped inductive load test circuit

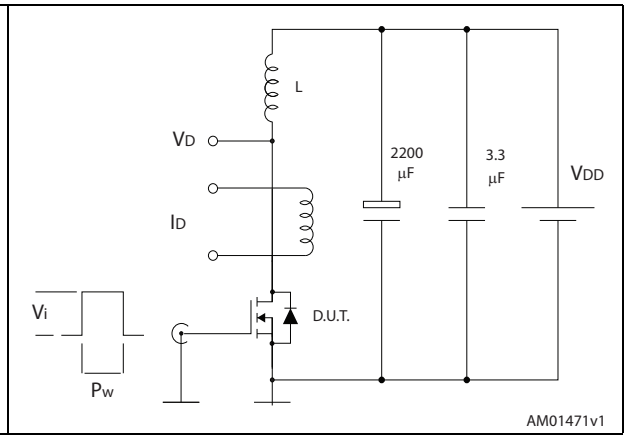


Figure 20. Unclamped inductive waveform

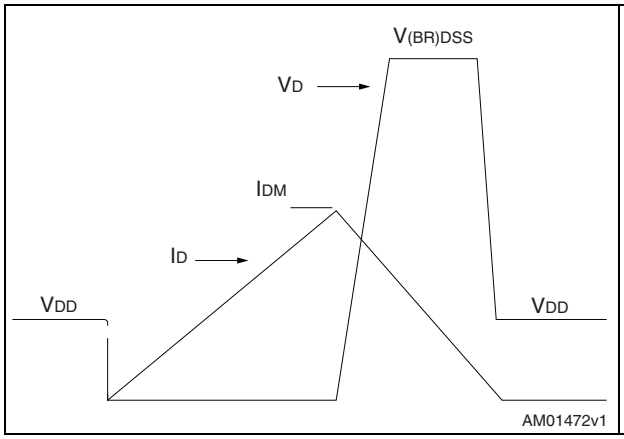
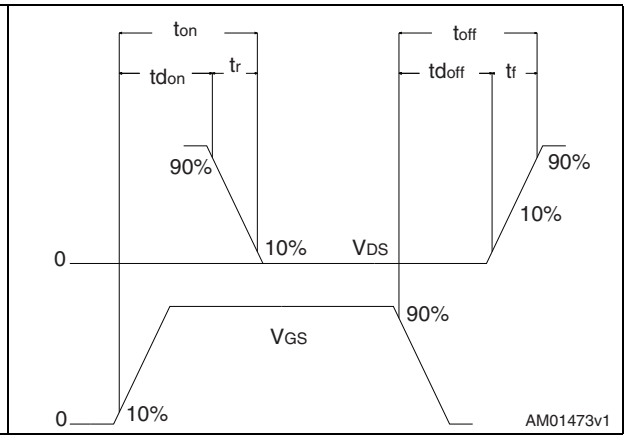


Figure 21. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Table 9. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Figure 22. TO-220FP drawing

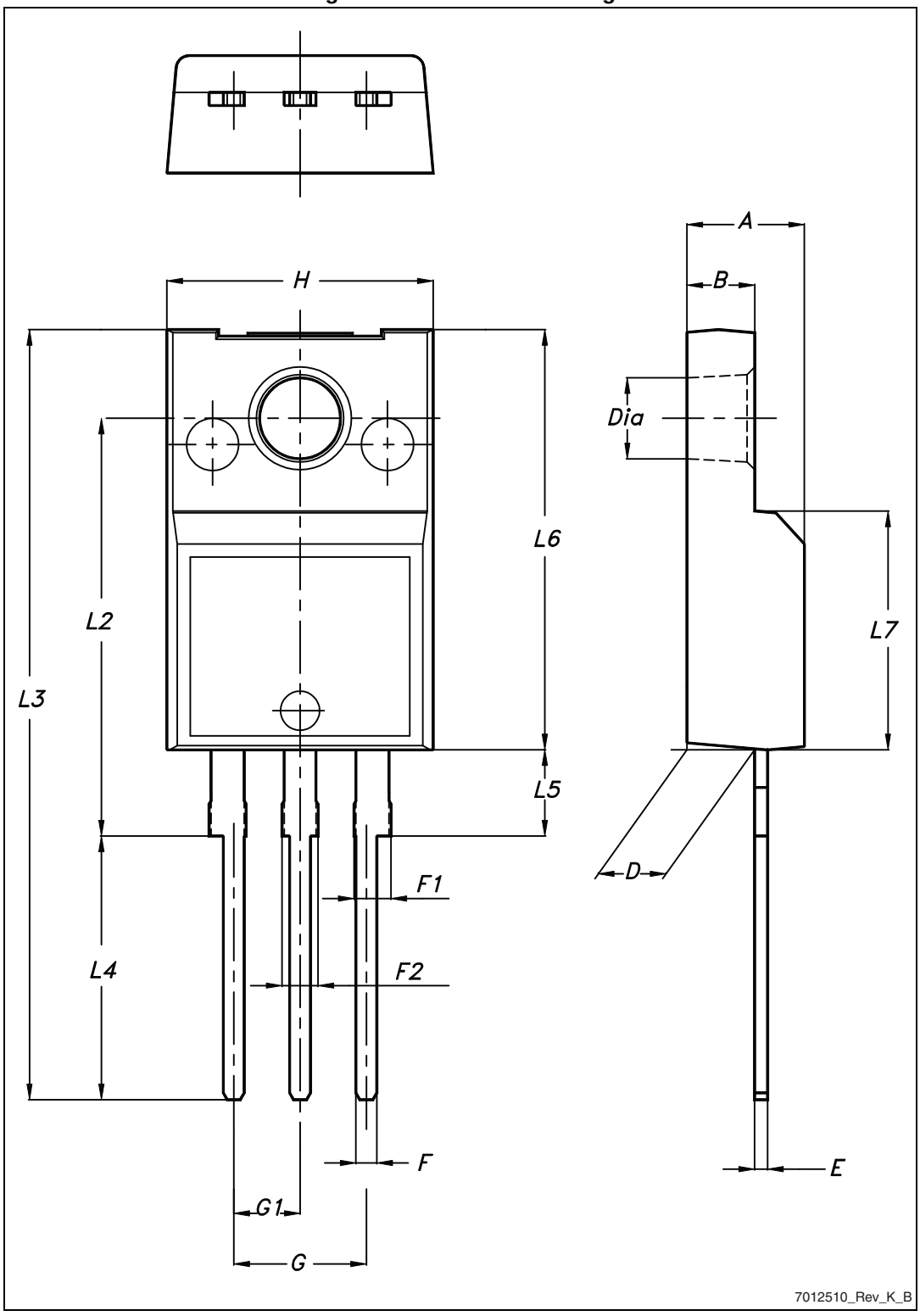


Table 10. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
∅P	3.75		3.85
Q	2.65		2.95

Figure 23. TO-220 type A drawing

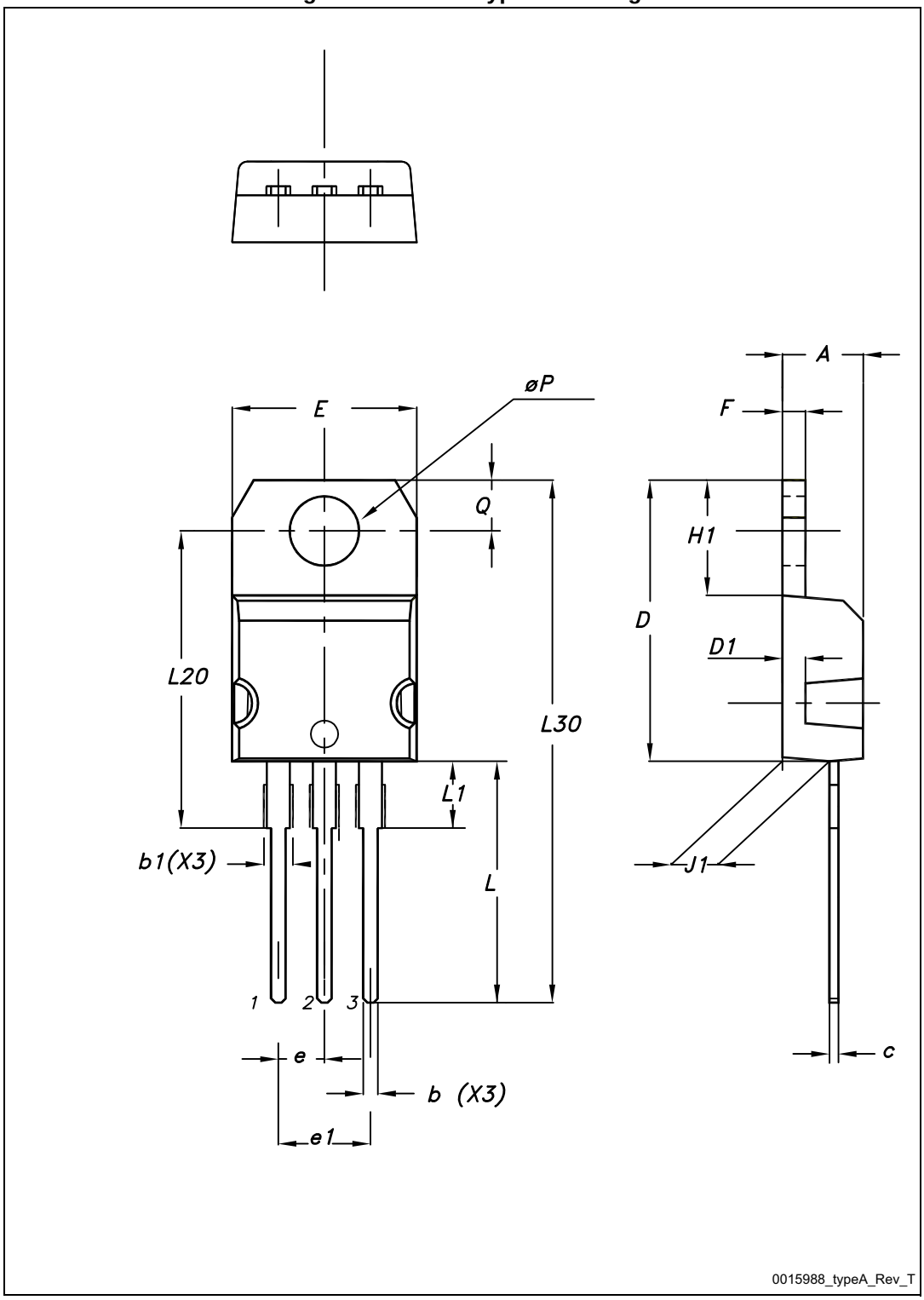
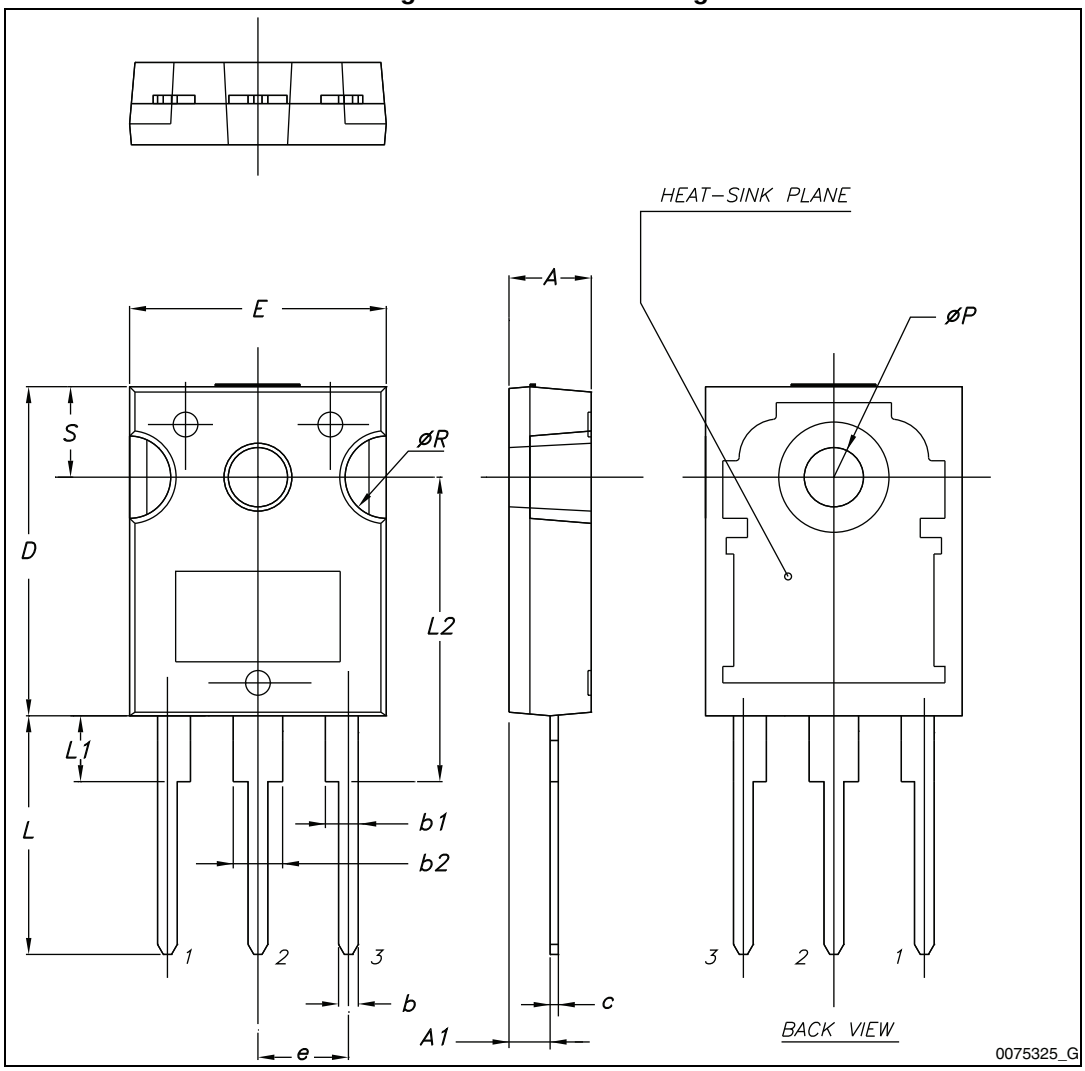


Table 11. TO-247 mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
∅P	3.55		3.65
∅R	4.50		5.50
S	5.30	5.50	5.70

Figure 24. TO-247 drawing



5 Revision history

Table 12. Document revision history

Date	Revision	Changes
09-Feb-2010	1	First release
03-Sep-2013	2	– Updated: *Section 2.1: Electrical characteristics (curves)* – Updated: *Section 4: Package mechanical data* – Minor text changes.

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