



# N-channel 600 V, 0.175 Ω typ., 18 A MDmesh™ DM2 Power MOSFET in a TO-220FP package

Datasheet - production data

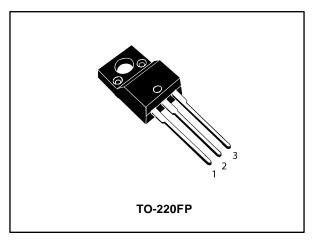
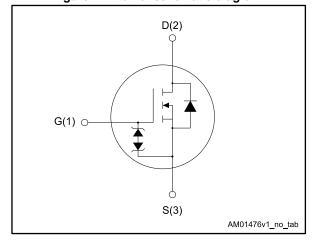


Figure 1: Internal schematic diagram



### **Features**

Order code	V <sub>DS</sub> @ T <sub>Jmax</sub>	R <sub>DS(on)</sub> max.	ΙD
STF24N60DM2	650 V	0.200 Ω	18 A

- Fast-recovery body diode
- Extremely low gate charge and input capacitance
- Low on-resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected

### **Applications**

Switching applications

## **Description**

This high voltage N-channel Power MOSFET is part of the MDmesh  $^{\text{TM}}$  DM2 fast recovery diode series. It offers very low recovery charge (Q<sub>rr</sub>) and time (t<sub>rr</sub>) combined with low R<sub>DS(on)</sub>, rendering it suitable for the most demanding high efficiency converters and ideal for bridge topologies and ZVS phase-shift converters.

**Table 1: Device summary** 

Order code	Marking	Package	Packing
STF24N60DM2	24N60DM2	TO-220FP	Tube

Contents STF24N60DM2

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STF24N60DM2 Electrical ratings

# 1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V <sub>G</sub> s	Gate-source voltage	± 25	V
Ip <sup>(1)</sup>	Drain current (continuous) at T <sub>C</sub> = 25 °C	18	Λ
ID(*/	Drain current (continuous) at T <sub>C</sub> = 100 °C	11	Α
I <sub>DM</sub> <sup>(2)(1)</sup>	Drain current (pulsed)	72	Α
P <sub>TOT</sub>	Total dissipation at T <sub>C</sub> = 25 °C	30	W
dv/dt <sup>(3)</sup>	Peak diode recovery voltage slope	40	V/ns
dv/dt <sup>(4)</sup>	MOSFET dv/dt ruggedness	50	V/IIS
V <sub>ISO</sub>	Insulation with stand voltage (RMS) from all three leads to external heat sink (t = 1 s; $T_c$ = 25 °C)		V
T <sub>stg</sub>	Storage temperature range	55 to 150	°C
Tj	Max. operating junction temperature range	–55 to 150	

### Notes:

Table 3: Thermal data

Symbol	Parameter	Value	Unit
R <sub>thj-case</sub>	Thermal resistance junction-case max.		°C/W
R <sub>thj-amb</sub>	Thermal resistance junction-ambient max. 62.5		C/VV

**Table 4: Avalanche characteristics** 

Symbol	Parameter	Value	Unit
I <sub>AR</sub>	AR Avalanche current, repetitive or not repetitive (pulse width limited by T <sub>Jmax</sub> )		А
Eas	Single pulse avalanche energy (starting T <sub>J</sub> =25 °C, I <sub>D</sub> = I <sub>AR</sub> ; V <sub>DD</sub> = 50 V)		mJ

<sup>&</sup>lt;sup>(1)</sup> Limited by package.

 $<sup>^{\</sup>left( 2\right) }$  Pulse width is limited by safe operating area.

 $<sup>^{(3)}</sup>$  I<sub>SD</sub>  $\leq$  18 A, di/dt  $\leq$  400 A/µS, V<sub>DS(peak)</sub> < V<sub>(BR)DSS</sub>, V<sub>DD</sub> = 400 V.

 $<sup>^{(4)}</sup>$  V<sub>DS</sub>  $\leq 480$  V.

## 2 Electrical characteristics

(T<sub>case</sub>= 25 °C unless otherwise specified)

Table 5: On /off states

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage	$V_{GS} = 0 \text{ V}, I_D = 1 \text{ mA}$	600			٧
	Zara gata valtaga drain	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 600 V			1.5	μΑ
IDSS	Zero gate voltage drain current	$V_{GS} = 0 \text{ V}, V_{DS} = 600 \text{ V},$ $T_{C} = 125 \text{ °C} \text{ (1)}$			100	μΑ
Igss	Gate-body leakage current	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±25 V			±10	μΑ
V <sub>GS(th)</sub>	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250 \mu A$	3	4	5	V
R <sub>DS(on)</sub>	Static drain-source on- resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 9 A		0.175	0.200	Ω

#### Notes:

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
Ciss	Input capacitance		-	1055	ı	pF
Coss	Output capacitance	V <sub>DS</sub> = 100 V, f = 1 MHz,	-	56	ı	pF
Crss	Reverse transfer capacitance	Ves = 0 V	-	2.4	-	pF
Coss eq. (1)	Equivalent output capacitance	V <sub>DS</sub> = 0 to 480 V, V <sub>GS</sub> = 0 V	-	259	-	pF
Rg	Intrinsic gate resistance	nce f = 1 MHz, I <sub>D</sub> = 0 A		7	1	Ω
$Q_g$	Total gate charge	$V_{DD} = 480 \text{ V}, I_D = 18 \text{ A},$	-	29	ı	nC
Q <sub>gs</sub>	Gate-source charge	V <sub>G</sub> S = 10 V	-	6	-	nC
$Q_{gd}$	Gate-drain charge	(see Figure 15: "Test circuit for gate charge behavior")	-	12	-	nC

#### Notes:

 $<sup>^{(1)}</sup>$ Defined by design, not subject to production test.

 $<sup>^{(1)}</sup>C_{oss\ eq.}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{OSS}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ .

### Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t <sub>d(on)</sub>	Turn-on delay time	V <sub>DD</sub> = 300 V, I <sub>D</sub> = 9 A	ı	15	-	ns
tr	Rise time	$R_G = 4.7 \Omega$ , $V_{GS} = 10 V$	ı	8.7	-	ns
t <sub>d(off)</sub>	Turn-off-delay time	(see Figure 14: "Test circuit for resistive load switching times"	-	60	-	ns
t <sub>f</sub>	Fall time	and Figure 19: "Switching time waveform")	-	15	-	ns

### Table 8: Source-drain diode

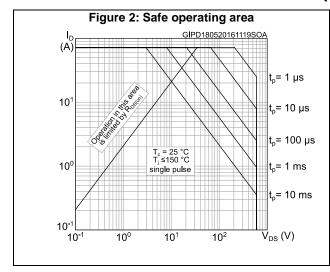
Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I <sub>SD</sub>	Source-drain current		ı		18	Α
I <sub>SDM</sub> <sup>(1)</sup>	Source-drain current (pulsed)		-		72	Α
V <sub>SD</sub> (2)	Forward on voltage	V <sub>GS</sub> = 0 V, I <sub>SD</sub> = 18 A	ı		1.6	V
t <sub>rr</sub>	Reverse recovery time	I <sub>SD</sub> = 18 A, di/dt = 100 A/µs,	1	155		ns
Qrr	Reverse recovery charge	V <sub>DD</sub> = 60 V (see Figure 16: "Test circuit for inductive load switching and diode recovery times")		956		nC
I <sub>RRM</sub>	Reverse recovery current			12.5		Α
t <sub>rr</sub>	Reverse recovery time	I <sub>SD</sub> = 18 A, di/dt = 100 A/μs,	-	200		ns
Qrr	Reverse recovery charge	$V_{DD} = 60 \text{ V}, T_j = 150 \text{ °C (see}$ Figure 16: "Test circuit for	ı	1450		nC
I <sub>RRM</sub>	Reverse recovery current	inductive load switching and diode recovery times")	-	13		Α

### Notes:

 $<sup>^{\</sup>left( 1\right) }$  Pulse width is limited by safe operating area.

 $<sup>^{(2)}</sup>$  Pulse test: pulse duration = 300  $\mu s,$  duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)



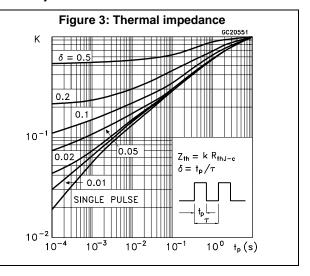
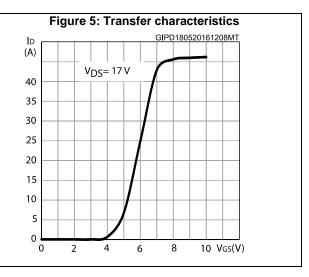
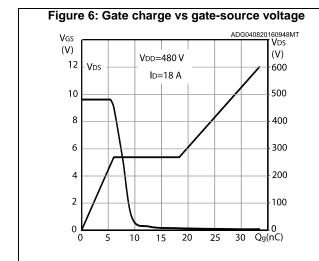
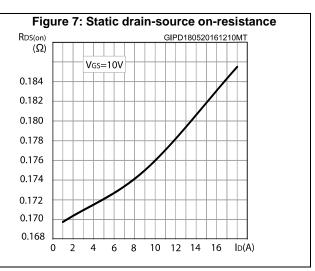


Figure 4: Output characteristics GIPD180520161207MT V<sub>GS</sub>= 8, 9, 10 V (A)  $V_{GS} = 7 V$ 40 35 30 25 V<sub>GS</sub>= 6 V 20 15 10  $V_{GS} = 5 V$ 5  $V_{GS} = 4 V$ 0 5 10 15 20 VDS(V)







STF24N60DM2 Electrical characteristics

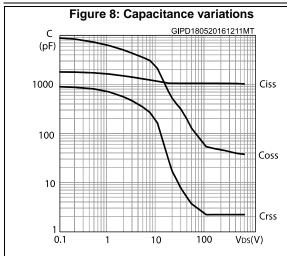
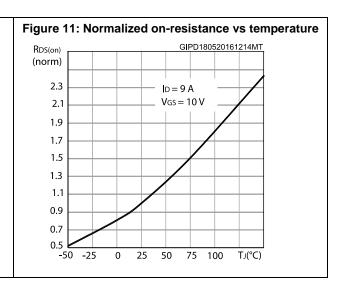
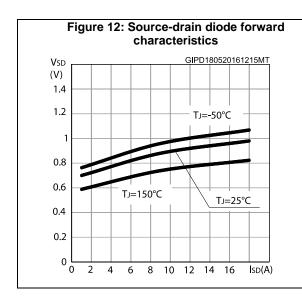


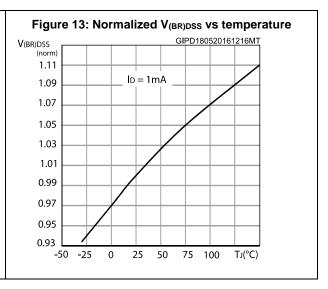
Figure 9: Output capacitance stored energy

Eoss (μ) 8 7 6 5 4 4 3 2 1 0 0 100 200 300 400 500 600 Vos(V)

Figure 10: Normalized gate threshold voltage vs temperature  $V_{GS(th)}$ GIPD180520161213MT (norm)  $I_D = 250 \; \mu A$ 1.1 1.0 0.9 0.8 0.7 0.6 0 25 50 75 100





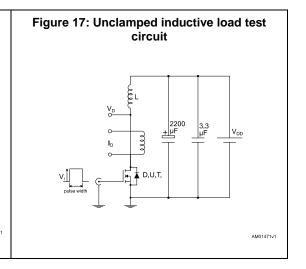


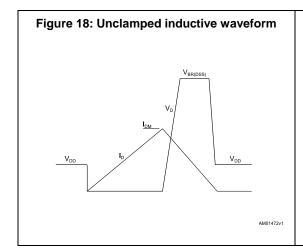
Test circuits STF24N60DM2

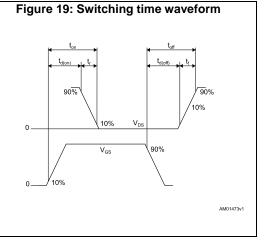
## 3 Test circuits

Figure 14: Test circuit for resistive load switching times

Figure 16: Test circuit for inductive load switching and diode recovery times







# 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: **www.st.com**. ECOPACK® is an ST trademark.



# 4.1 TO-220FP package information

Figure 20: TO-220FP package outline

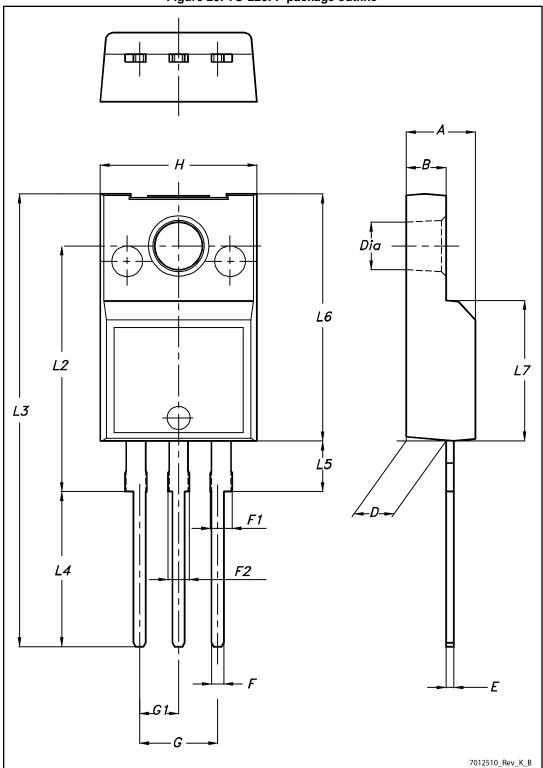


Table 9: TO-220FP package mechanical data

D!		mm	
Dim.	Min.	Тур.	Max.
A	4.4		4.6
В	2.5		2.7
D	2.5		2.75
Е	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
Н	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Revision history STF24N60DM2

# 5 Revision history

Table 10: Document revision history

Date	Revision	Changes
12-Nov-2013	1	First release.
21-Jan-2014	2	<ul> <li>Modified: dv/dt value in Table 2</li> <li>Modified: I<sub>AR</sub> value in Table 4</li> <li>Modified: I<sub>DSS</sub> and V<sub>GS(th)</sub> in Table 5</li> <li>Minor text changes</li> </ul>
03-Mar-2014	3	- Modified: Figure 1  - Modified: P <sub>TOT</sub> value and note 1 in Table 2  - Modified: R <sub>thj-case</sub> value in Table 3  - Modified: I <sub>AR</sub> value in Table 4  - Minor text changes
05-Mar-2015	4	<ul><li>Document status promoted from preliminary to production data.</li><li>Updated title, features and description in cover page.</li></ul>
20-Sep-2016	5	Updated Figure 2: "Safe operating area". Minor text changes

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