N-channel 650 V, 0.156 Ω typ., 20 A, MDmesh™ DM2 Power MOSFET in a TO-220FP package
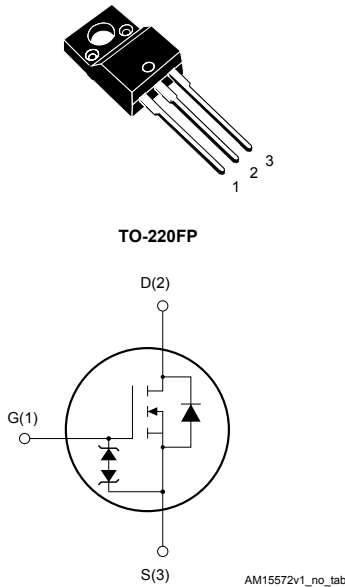

TO-220FP

Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STF26N65DM2	650 V	0.190 Ω	20 A	30 W

- Fast-recovery body diode
- Extremely low gate charge and input capacitance
- Low on-resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected

Applications

- Switching applications

Description

This high-voltage N-channel Power MOSFET is part of the MDmesh™ DM2 fast-recovery diode series. It offers very low recovery charge (Q_{rr}) and time (t_{rr}) combined with low $R_{DS(on)}$, rendering it suitable for the most demanding high-efficiency converters and ideal for bridge topologies and ZVS phase-shift converters.

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Product status link
STF26N65DM2

Product summary	
Order code	STF26N65DM2
Marking	26N65DM2
Package	TO-220FP
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±25	V
I_D [1]	Drain current (continuous) at T_{case} = 25 °C	20	A
	Drain current (continuous) at T_{case} = 100 °C	12.6	
I_{DM} [2]	Drain current (pulsed)	53	A
P_{TOT}	Total dissipation at T_{case} = 25 °C	30	W
dv/dt [3]	Peak diode recovery voltage slope	50	V/ns
dv/dt [4]	MOSFET dv/dt ruggedness	50	
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heatsink (t = 1 s, T_C = 25 °C)	2500	V
T_{stg}	Storage temperature range	-55 to 150	°C
T_j	Operating junction temperature range		

1. Limited by maximum junction temperature
2. Pulse width is limited by safe operating area.
3. $I_{SD} \leq 20$ A, di/dt=900 A/µs, V_{DS} peak < $V_{(BR)DSS}$, V_{DD} = 400 V
4. $V_{DS} \leq 520$ V

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	4.2	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient	62.5	

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR} [1]	Avalanche current, repetitive or not repetitive	3	A
E_{AS} [2]	Single pulse avalanche energy	530	mJ

1. Pulse width is limited by T_{Jmax}.
2. Starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V

2 Electrical characteristics

(T_{case} = 25 °C unless otherwise specified)

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	650			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 650 V			1	μA
		V_{GS} = 0 V, V_{DS} = 650 V, T_{case} = 125 °C[1]			100	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±5	μA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 μA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 10 A		0.156	0.190	Ω

1. *Defined by design, not subject to production test.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	1480	-	pF
C_{oss}	Output capacitance		-	62	-	
C_{rss}	Reverse transfer capacitance		-	2	-	
$C_{oss\ eq.}$[1]	Equivalent output capacitance	V_{DS} = 0 to 520 V, V_{GS} = 0 V	-	140	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	-	4.6	-	Ω
Q_g	Total gate charge	V_{DD} = 520 V, I_D = 20 A,	-	35.5	-	nC
Q_{gs}	Gate-source charge	V_{GS} = 0 to 10 V	-	8.2	-	
Q_{gd}	Gate-drain charge	(see Figure 14. Test circuit for gate charge behavior)	-	17.6	-	

1. *$C_{oss\ eq.}$ is defined as the constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 325 V, I_D = 10 A,	-	17	-	ns
t_r	Rise time	R_G = 4.7 Ω, V_{GS} = 10 V	-	7	-	
$t_{d(off)}$	Turn-off delay time	(see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	51	-	
t_f	Fall time		-	10	-	

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		20	A
I_{SDM}[1]	Source-drain current (pulsed)		-		53	A
V_{SD}[2]	Forward on voltage	V_{GS} = 0 V, I_{SD} = 20 A	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 20 A, di/dt = 100 A/µs,	-	100		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 100 V	-	0.365		µC
I_{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	7.3		A
t_{rr}	Reverse recovery time	I_{SD} = 20 A, di/dt = 100 A/µs,	-	200		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 100 V, T_J = 150 °C	-	1.39		µC
I_{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	13.9		A

1. *Pulse width is limited by safe operating area.*

2. *Pulse test: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

Figure 2. Thermal impedance

Figure 3. Output characteristics
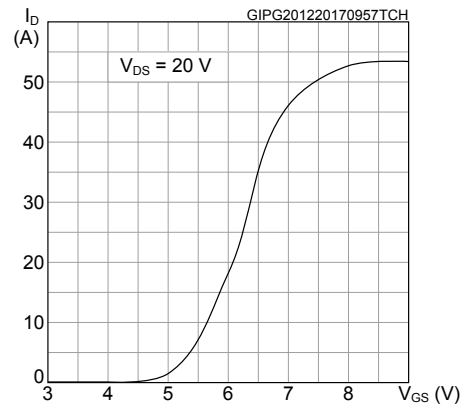

Figure 4. Transfer characteristics

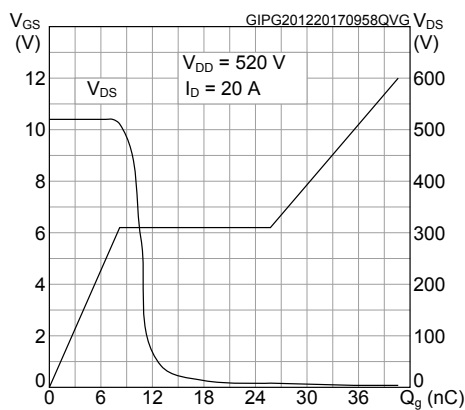**Figure 5. Gate charge vs gate-source voltage**

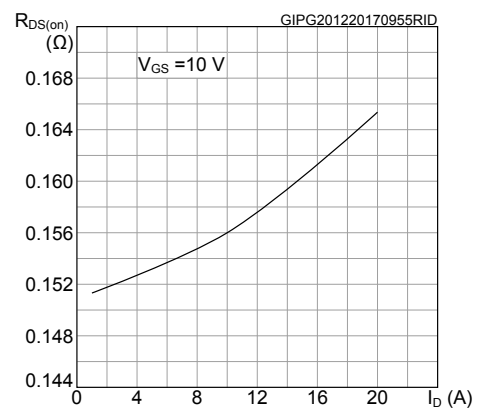

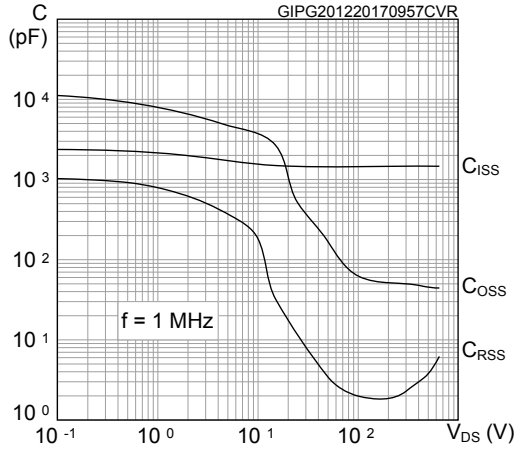**Figure 6. Static drain-source on-resistance**

Figure 7. Capacitance variations

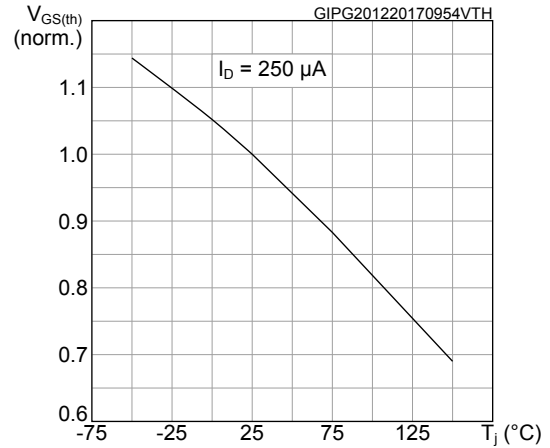**Figure 8. Normalized gate threshold voltage vs temperature**
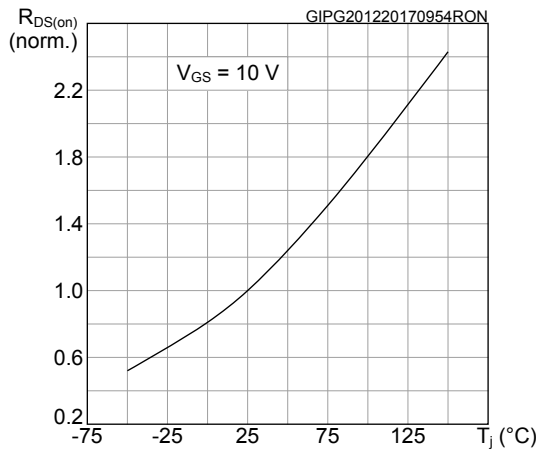

Figure 9. Normalized on-resistance vs temperature

Figure 10. Normalized V$_{(BR)DSS}$ vs temperature
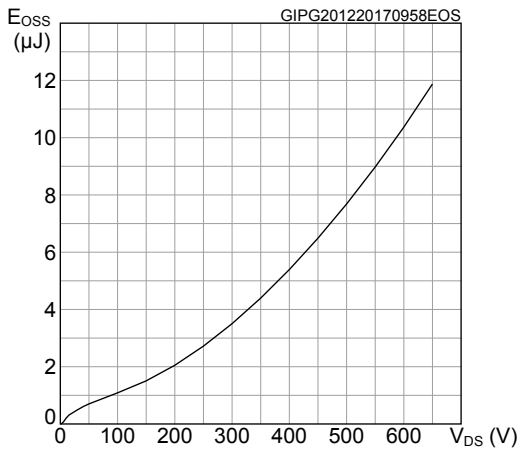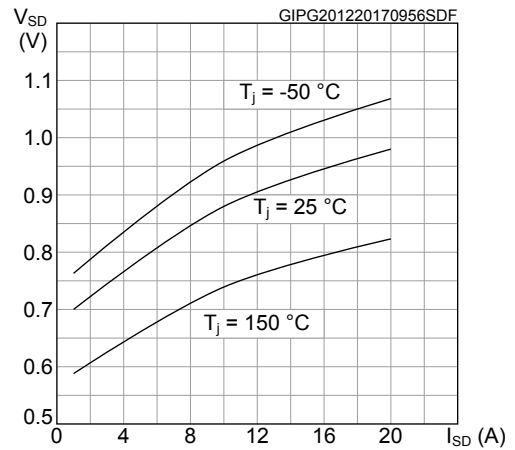

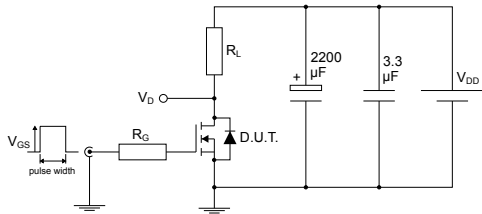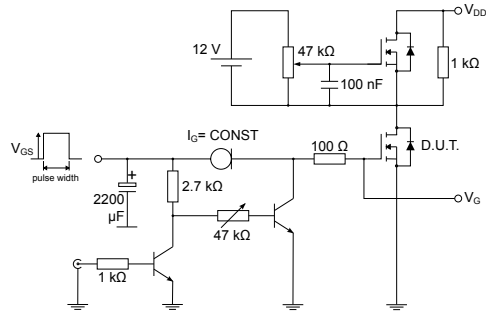**Figure 11. Output capacitance stored energy**

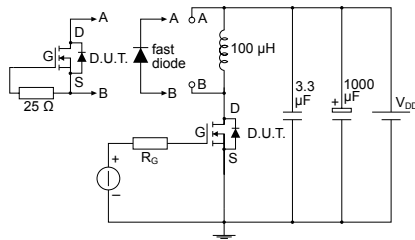**Figure 12. Source-drain diode forward characteristics**

3   Test circuits

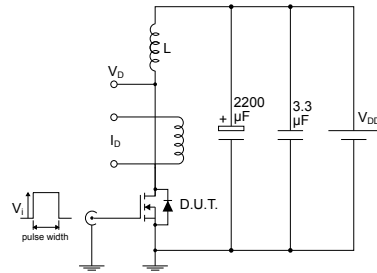**Figure 13. Test circuit for resistive load switching times**

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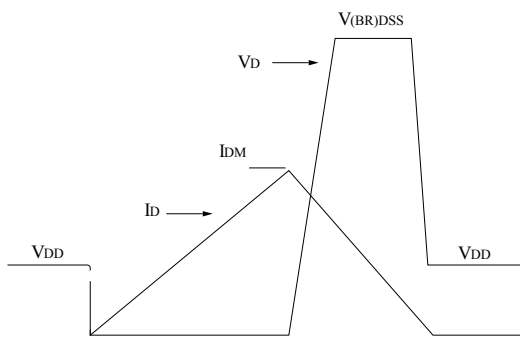**Figure 14. Test circuit for gate charge behavior**

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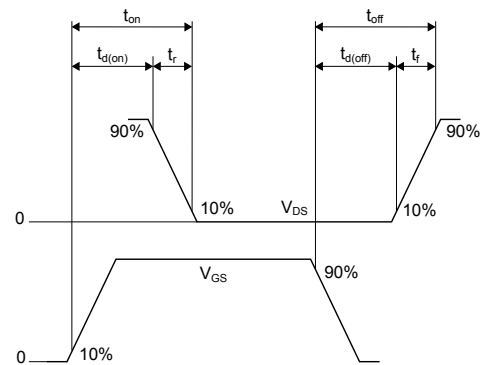**Figure 15. Test circuit for inductive load switching and diode recovery times**

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Figure 16. Unclamped inductive load test circuit

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Figure 17. Unclamped inductive waveform

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Figure 18. Switching time waveform

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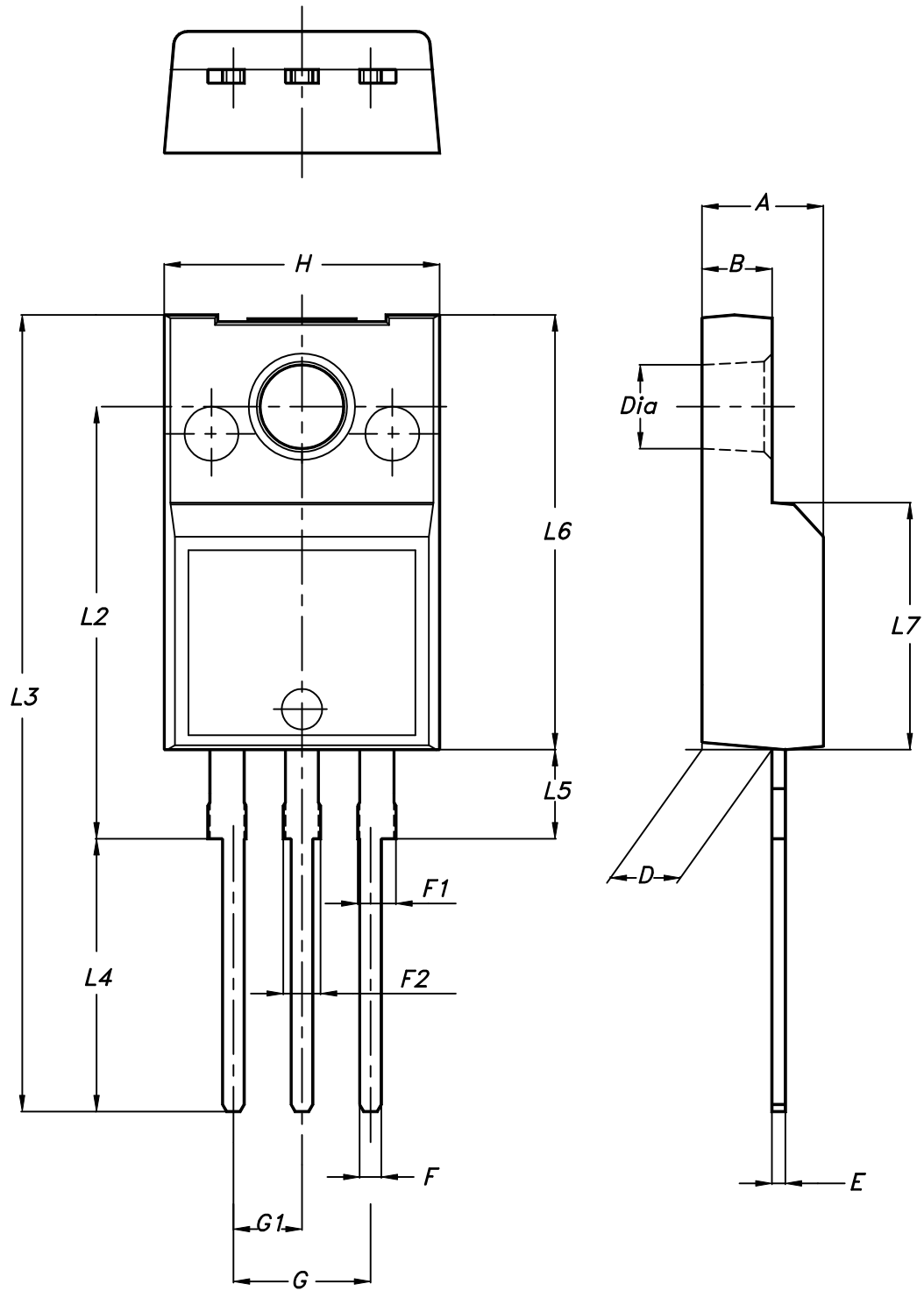# 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 TO-220FP package information

Figure 19. TO-220FP package outline

7012510_Rev_12_B

Table 8. **TO-220FP package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Revision history

Table 9. Document revision history

Date	Version	Changes
08-Jan-2018	1	First release.
03-Jul-2018	2	Removed maturity status indication from cover page. The document status is production data. Updated Table 6. Switching times. Minor text changes

Contents

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