



## STF40NF06

N-channel 60V - 0.024Ω - 23A - TO-220FP  
STripFET™ II Power MOSFET

### General features

| Type      | V <sub>DSS</sub> | R <sub>DS(on)</sub> | I <sub>D</sub> |
|-----------|------------------|---------------------|----------------|
| STF40NF06 | 60V              | <0.028Ω             | 23A            |

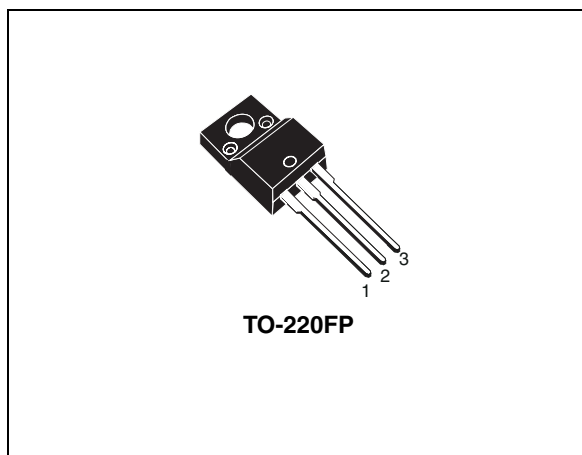
- Exceptional dv/dt capability
- Low gate charge at 100°C
- Application oriented characterization
- 100% avalanche tested

### Description

This MOSFET is the latest development of STMicroelectronics unique “Single Feature Size™” strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

### Applications

- Switching application



### Internal schematic diagram



### Order codes

| Part number | Marking | Package  | Packaging |
|-------------|---------|----------|-----------|
| STF40NF06   | F40NF06 | TO-220FP | Tube      |

## Contents

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# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

| Symbol             | Parameter  | Value      | Unit                |
|--------------------|--|------------|---------------------|
| $V_{DS}$           | Drain-source voltage ( $V_{GS} = 0$ )  | 60         | V                   |
| $V_{GS}$           | Gate-source voltage  | $\pm 20$   | V                   |
| $I_D$              | Drain current (continuous) at $T_C = 25^\circ\text{C}$   | 23         | A                   |
| $I_D$              | Drain current (continuous) at $T_C = 100^\circ\text{C}$  | 16         | A                   |
| $I_{DM}^{(1)}$     | Drain current (pulsed)   | 92         | A                   |
| $P_{TOT}$          | Total dissipation at $T_C = 25^\circ\text{C}$  | 30         | W                   |
|                    | Derating Factor  | 0.2        | W/ $^\circ\text{C}$ |
| $dv/dt^{(2)}$      | Peak diode recovery voltage slope  | 10         | V/ns                |
| $E_{AS}^{(3)}$     | Single pulse avalanche energy  | 250        | mJ                  |
| $V_{ISO}$          | Insulation withstand voltage (RMS) from all three leads to external heat sink ( $t=1\text{s}$ ; $T_C = 25^\circ\text{C}$ ) | 2500       | V                   |
| $T_J$<br>$T_{stg}$ | Operating junction temperature<br>Storage temperature  | -55 to 175 | $^\circ\text{C}$    |

1. Pulse width limited by safe operating area
2.  $I_{SD} \leq 40\text{A}$ ,  $di/dt \leq 300\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_J \leq T_{JMAX}$
3. Starting  $T_J = 25^\circ\text{C}$ ,  $I_D = 20\text{A}$ ,  $V_{DD} = 30\text{V}$

**Table 2. Thermal data**

|                |  |     |                           |
|----------------|--|-----|---------------------------|
| $R_{thj-case}$ | Thermal resistance junction-case Max           | 5.0 | $^\circ\text{C}/\text{W}$ |
| $T_l$          | Maximum lead temperature for soldering purpose | 275 | $^\circ\text{C}$          |

## 2 Electrical characteristics

(T<sub>CASE</sub>=25°C unless otherwise specified)

**Table 3. On/off states**

| Symbol               | Parameter   | Test conditions   | Min. | Typ.  | Max.    | Unit     |
|----------------------|---|---|------|-------|---------|----------|
| V <sub>(BR)DSS</sub> | Drain-source breakdown voltage                        | I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0                          | 60   |       |         | V        |
| I <sub>DSS</sub>     | Zero gate voltage drain current (V <sub>GS</sub> = 0) | V <sub>DS</sub> = Max rating,<br>V <sub>DS</sub> = Max rating @ 125°C |      |       | 1<br>10 | μA<br>μA |
| I <sub>GSS</sub>     | Gate body leakage current (V <sub>DS</sub> = 0)       | V <sub>GS</sub> = ±20V  |      |       | ± 100   | nA       |
| V <sub>GS(th)</sub>  | Gate threshold voltage                                | V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA            | 2    |       | 4       | V        |
| R <sub>DS(on)</sub>  | Static drain-source on resistance                     | V <sub>GS</sub> = 10V, I <sub>D</sub> = 11.5A                         |      | 0.024 | 0.028   | Ω        |

**Table 4. Dynamic**

| Symbol   | Parameter   | Test conditions  | Min. | Typ.             | Max. | Unit           |
|--|---|--|------|------------------|------|----------------|
| g <sub>fs</sub> <sup>(1)</sup>                           | Forward transconductance  | V <sub>DS</sub> = 30V, I <sub>D</sub> = 11.5A                        |      | 12               |      | S              |
| C <sub>iss</sub><br>C <sub>oss</sub><br>C <sub>rss</sub> | Input capacitance<br>Output capacitance<br>Reverse transfer capacitance | V <sub>DS</sub> = 25V, f = 1 MHz,<br>V <sub>GS</sub> = 0             |      | 920<br>225<br>80 |      | pF<br>pF<br>pF |
| Q <sub>g</sub><br>Q <sub>gs</sub><br>Q <sub>gd</sub>     | Total gate charge<br>Gate-source charge<br>Gate-drain charge            | V <sub>DD</sub> = 48V, I <sub>D</sub> = 10A<br>V <sub>GS</sub> = 10V |      | 32<br>6.5<br>15  | 43   | nC<br>nC<br>nC |

1. Pulsed: pulse duration = 300μs, duty cycle 1.5%

**Table 5. Switching times**

| Symbol                                | Parameter                        | Test conditions   | Min. | Typ.     | Max. | Unit     |
|---------------------------------------|----------------------------------|---|------|----------|------|----------|
| t <sub>d(on)</sub><br>t <sub>r</sub>  | Turn-on Delay Time<br>Rise Time  | V <sub>DD</sub> = 30V, I <sub>D</sub> = 20A,<br>R <sub>G</sub> = 4.7Ω, V <sub>GS</sub> = 10V<br>(see Figure 13) |      | 27<br>11 |      | ns<br>ns |
| t <sub>d(off)</sub><br>t <sub>f</sub> | Turn-off-delay time<br>Fall time | V <sub>DD</sub> = 30V, I <sub>D</sub> = 20A,<br>R <sub>G</sub> = 4.7Ω, V <sub>GS</sub> = 10V<br>(see Figure 13) |      | 27<br>11 |      | ns<br>ns |

**Table 6. Source drain diode**

| Symbol                            | Parameter  | Test conditions  | Min | Typ.             | Max | Unit          |
|-----------------------------------|--|--|-----|------------------|-----|---------------|
| $I_{SD}$                          | Source-drain current   |  |     |                  | 23  | A             |
| $I_{SDM}^{(1)}$                   | Source-drain current (pulsed)  |  |     |                  | 92  | A             |
| $V_{SD}^{(2)}$                    | Forward on voltage   | $I_{SD}=23A, V_{GS}=0$   |     |                  | 1.3 | V             |
| $t_{rr}$<br>$Q_{rr}$<br>$I_{RRM}$ | Reverse recovery time<br>Reverse recovery charge<br>Reverse recovery current | $I_{SD}=40A,$<br>$di/dt = 100A/\mu s,$<br>$V_{DD}=10V, T_j=150^\circ C$<br>(see Figure 15) |     | 63<br>150<br>4.8 |     | ns<br>nC<br>A |

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 $\mu s$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

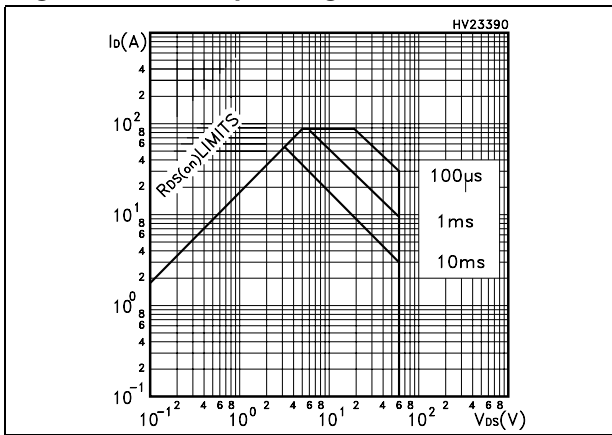


Figure 2. Thermal impedance

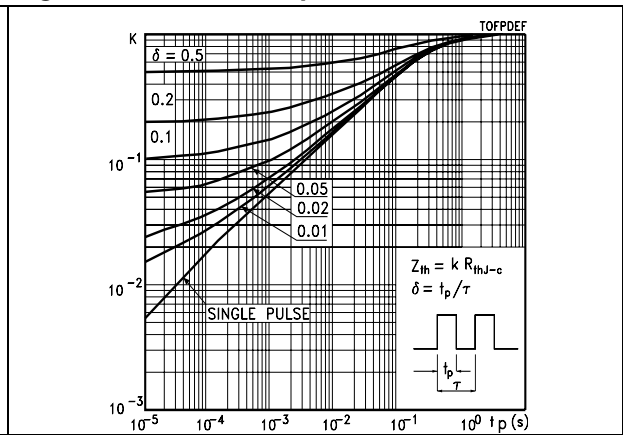


Figure 3. Output characteristics

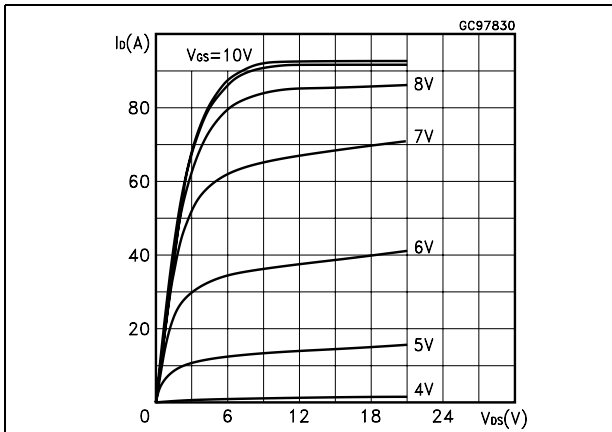


Figure 4. Transfer characteristics

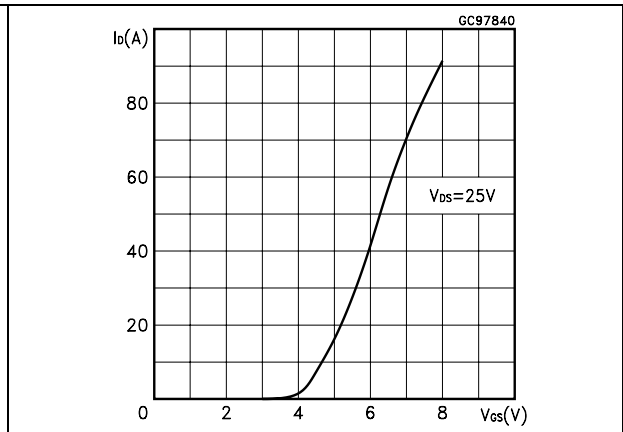


Figure 5. Transconductance

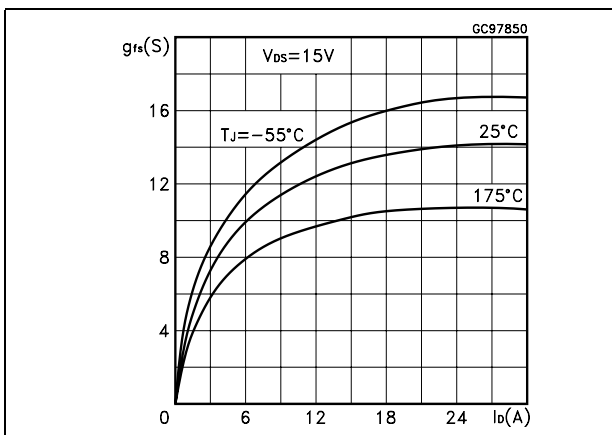


Figure 6. Static drain-source on resistance

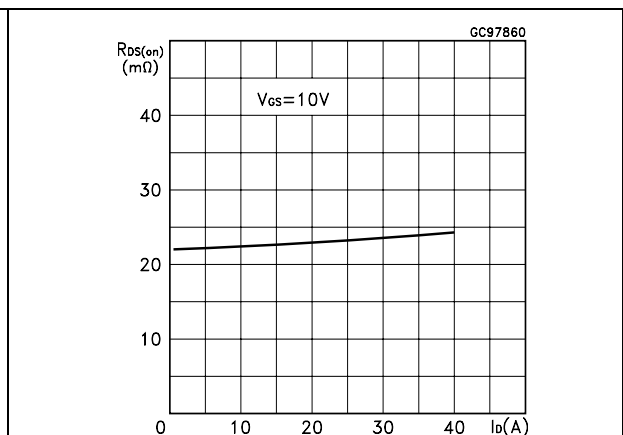


Figure 7. Gate charge vs gate-source voltage Figure 8. Capacitance variations

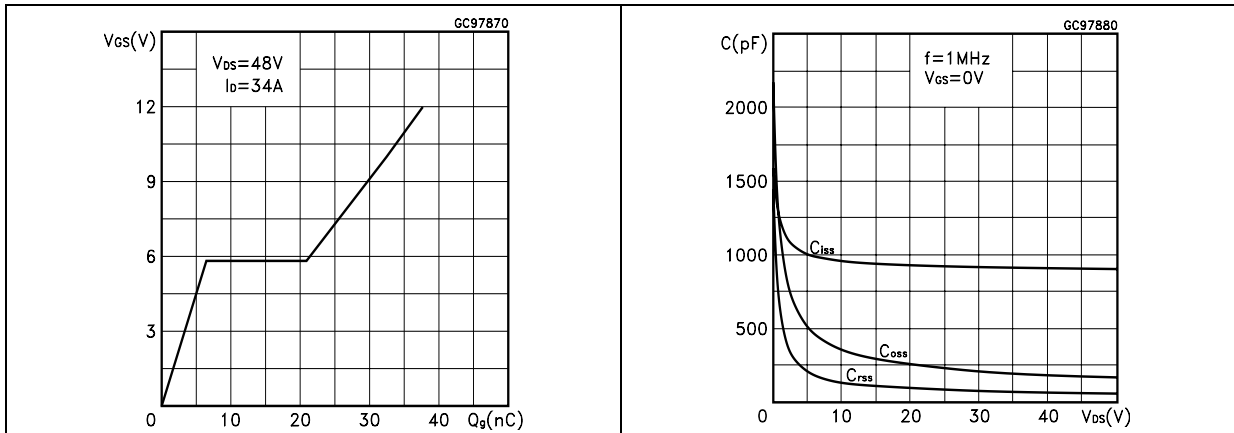


Figure 9. Normalized gate threshold voltage vs temperature Figure 10. Normalized on resistance vs temperature

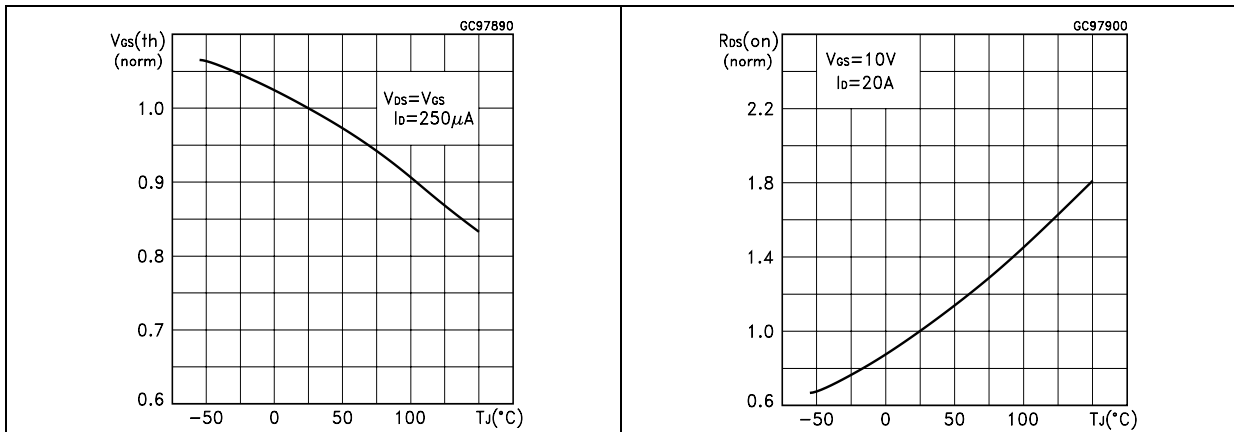
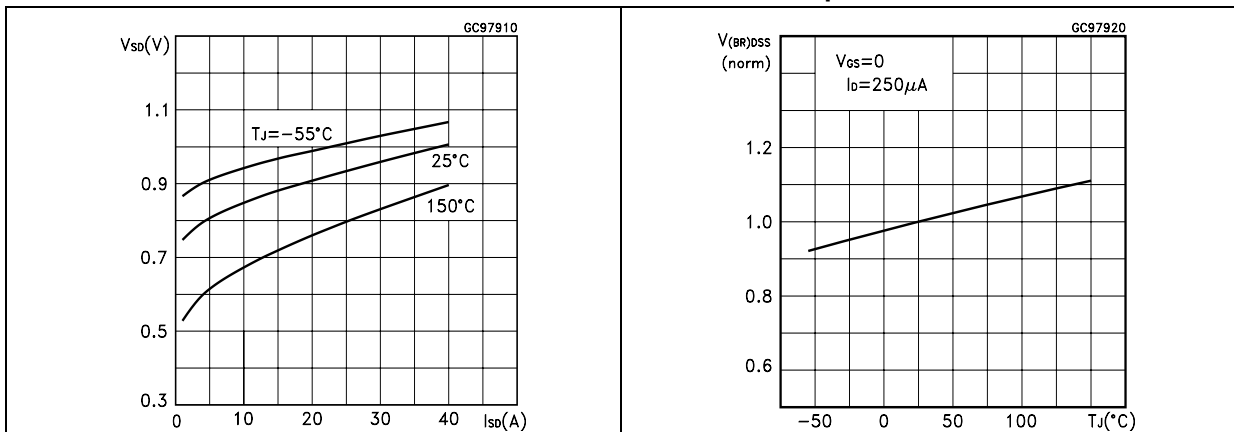


Figure 11. Source-drain diode forward characteristics Figure 12. Normalized breakdown voltage vs temperature



### 3 Test circuit

Figure 13. Switching times test circuit for resistive load

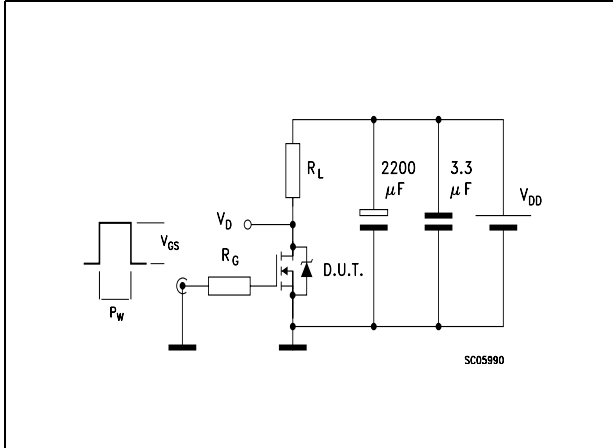


Figure 14. Gate charge test circuit

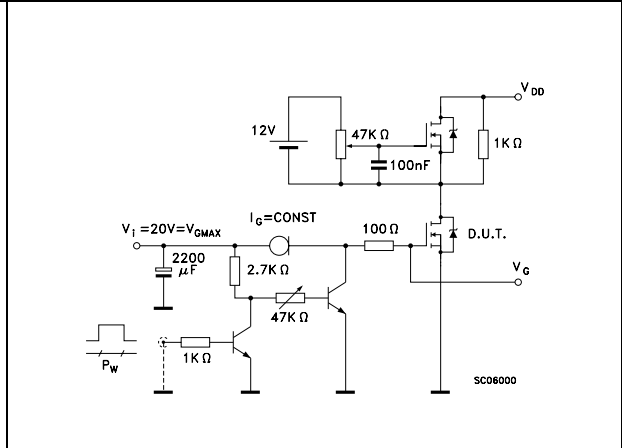


Figure 15. Test circuit for inductive load switching and diode recovery times



Figure 16. Unclamped Inductive load test circuit

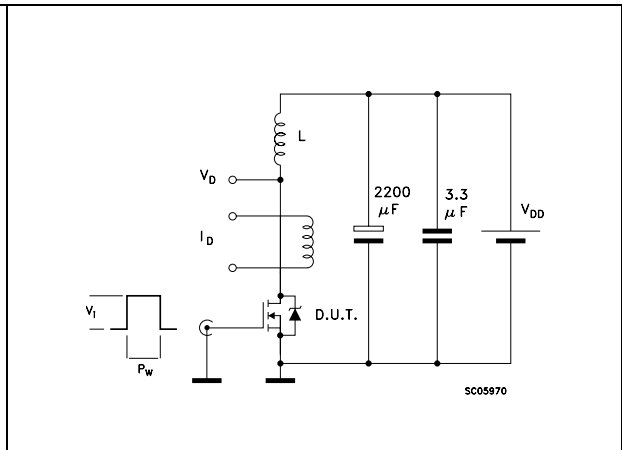


Figure 17. Unclamped inductive waveform

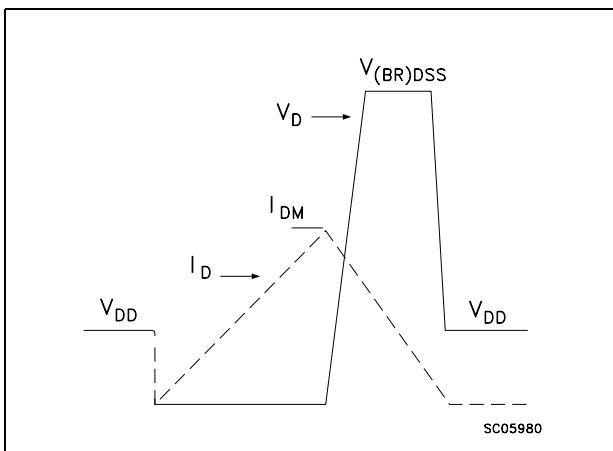
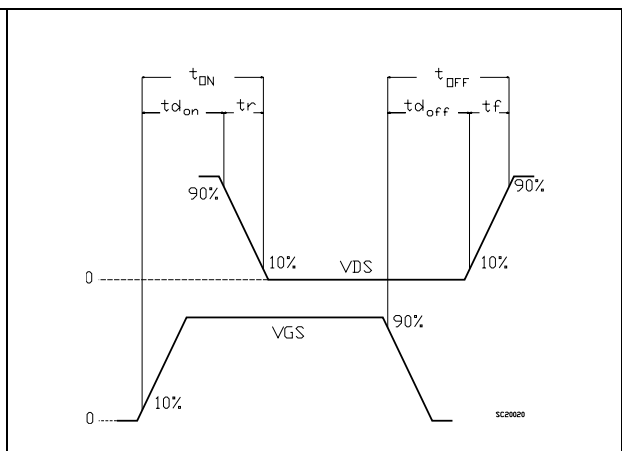


Figure 18. Switching time waveform



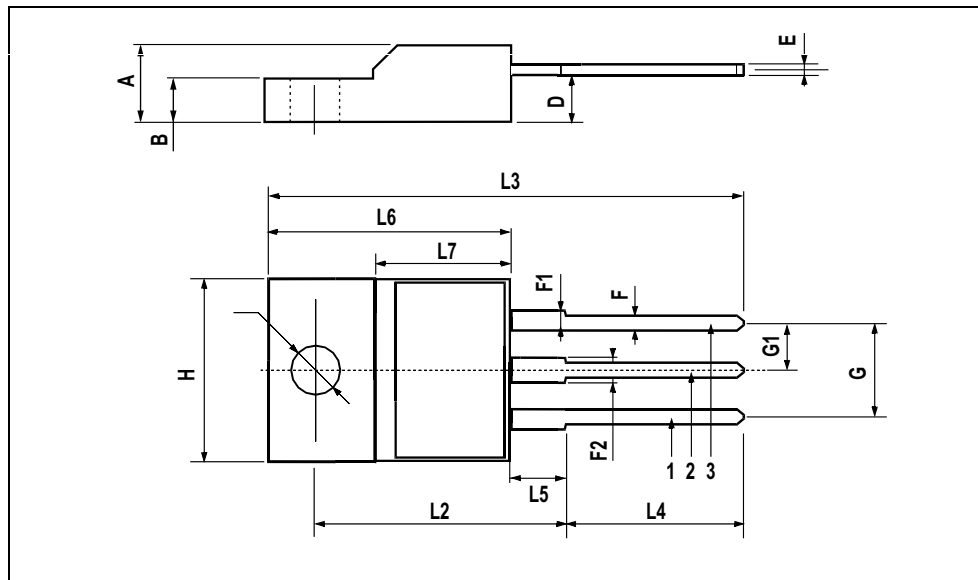


## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

**TO-220FP MECHANICAL DATA**

| DIM. | mm.  |      |      | inch  |       |       |
|------|------|------|------|-------|-------|-------|
|      | MIN. | TYP. | MAX. | MIN.  | TYP.  | MAX.  |
| A    | 4.4  |      | 4.6  | 0.173 |       | 0.181 |
| B    | 2.5  |      | 2.7  | 0.098 |       | 0.106 |
| D    | 2.5  |      | 2.75 | 0.098 |       | 0.108 |
| E    | 0.45 |      | 0.7  | 0.017 |       | 0.027 |
| F    | 0.75 |      | 1    | 0.030 |       | 0.039 |
| F1   | 1.15 |      | 1.7  | 0.045 |       | 0.067 |
| F2   | 1.15 |      | 1.7  | 0.045 |       | 0.067 |
| G    | 4.95 |      | 5.2  | 0.195 |       | 0.204 |
| G1   | 2.4  |      | 2.7  | 0.094 |       | 0.106 |
| H    | 10   |      | 10.4 | 0.393 |       | 0.409 |
| L2   |      | 16   |      |       | 0.630 |       |
| L3   | 28.6 |      | 30.6 | 1.126 |       | 1.204 |
| L4   | 9.8  |      | 10.6 | .0385 |       | 0.417 |
| L5   | 2.9  |      | 3.6  | 0.114 |       | 0.141 |
| L6   | 15.9 |      | 16.4 | 0.626 |       | 0.645 |
| L7   | 9    |      | 9.3  | 0.354 |       | 0.366 |
| Ø    | 3    |      | 3.2  | 0.118 |       | 0.126 |



## 5 Revision history

**Table 7. Revision history**

| <b>Date</b> | <b>Revision</b> | <b>Changes</b>                  |
|-------------|-----------------|---------------------------------|
| 12-Nov-2004 | 1               | First release                   |
| 27-May-2005 | 2               | Final datasheet                 |
| 04-Sep-2006 | 3               | New template, no content change |

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