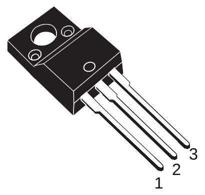
STF6N95K5

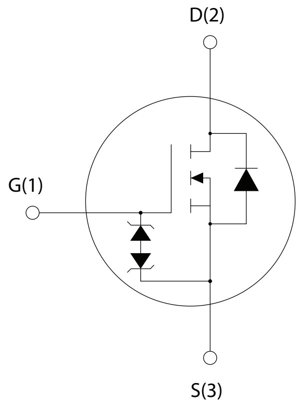
N-channel 950 V, 1 Ω typ., 9 A MDmesh™ K5 Power MOSFET in a TO-220FP package

Datasheet - production data



TO-220FP

Figure 1. Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STF6N95K5	950 V	1.25 Ω	9 A	25 W

- Industry's lowest $R_{DS(on)}$ * area
- Industry's best figure of merit (FoM)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This very high voltage N-channel Power MOSFET is designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Table 1. Device summary

Order code	Marking	Packages	Packaging
STF6N95K5	6N95K5	TO-220FP	Tube

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate- source voltage	± 30	V
I_D	Drain current (continuous) at T_C = 25 °C	9(1)	A
I_D	Drain current (continuous) at T_C = 100 °C	6(1)	A
I_{DM}(2)	Drain current (pulsed)	36	A
P_{TOT}	Total dissipation at T_C = 25 °C	25	W
I_{AR}(3)	Max current during repetitive or single pulse avalanche	3	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D=I_{AS}, V_{DD}= 50 V)	90	mJ
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s; T_C=25 °C)	2500	V
dv/dt (4)	Peak diode recovery voltage slope	4.5	V/ns
dv/dt (5)	MOSFET dv/dt ruggedness	50	V/ns
T_j T_{stg}	Operating junction temperature Storage temperature	- 55 to 150	°C

1. Limited by package.
2. Pulse width limited by safe operating area.
3. Pulse width limited by $T_{Jmax.}$
4. $I_{SD} \leq$ 9 A, di/dt $\leq$ 100 A/µs, $V_{DS(peak)} \leq V_{(BR)DSS}$
5. $V_{DS} \leq$ 760 V

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	5	°C/W
$R_{thj-amb}$	Thermal resistance junction-amb max	62.5	°C/W

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS}= 0, I_D = 1 mA	950			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0, V_{DS} = 950 V			1	µA
		V_{GS} = 0, V_{DS} = 950 V, Tc=125 °C			50	µA
I_{GSS}	Gate body leakage current	V_{DS} = 0, V_{GS} = ± 20 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D= 3 A		1	1.25	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{GS}=0, V_{DS} =100 V, f=1 MHz	-	450	-	pF
C_{oss}	Output capacitance		-	30	-	pF
C_{rss}	Reverse transfer capacitance		-	1.6	-	pF
$C_{o(tr)}$(1)	Equivalent capacitance time related	V_{GS} = 0, V_{DS} = 0 to 760 V	-	45	-	pF
$C_{o(er)}$(2)	Equivalent capacitance energy related		-	19	-	pF
R_G	Intrinsic gate resistance	f = 1MHz, I_D=0	-	7	-	Ω
Q_g	Total gate charge	V_{DD} = 760 V, I_D = 6 A, V_{GS} =10 V, *(see Figure 16)*	-	13	-	nC
Q_{gs}	Gate-source charge		-	3	-	nC
Q_{gd}	Gate-drain charge		-	7	-	nC

1. Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}
2. energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 475 V, I_D = 3 A, R_G=4.7 Ω, V_{GS}=10 V (*see Figure 18*)	-	12	-	ns
t_r	Rise time		-	12	-	ns
$t_{d(off)}$	Turn-off delay time		-	33	-	ns
t_f	Fall time		-	21	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		9	A
I_{SDM}	Source-drain current (pulsed)		-		36	A
V_{SD}(1)	Forward on voltage	I_{SD}= 6 A, V_{GS}=0	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD}= 6 A, V_{DD}= 60 V di/dt = 100 A/µs, (*see Figure 17*)	-	372		ns
Q_{rr}	Reverse recovery charge		-	4		µC
I_{RRM}	Reverse recovery current		-	22		A
t_{rr}	Reverse recovery time	I_{SD}= 6 A,V_{DD}= 60 V di/dt=100 A/µs, Tj=150 °C (*see Figure 17*)	-	522		ns
Q_{rr}	Reverse recovery charge		-	5		µC
I_{RRM}	Reverse recovery current		-	20		A

1. Pulsed: pulse duration = 300µs, duty cycle 1.5%

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	I_{GS} = ± 1mA, I_D=0	30	-	-	V

The built-in back-to-back Zener diodes have specifically been designed to enhance the device's ESD capability. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

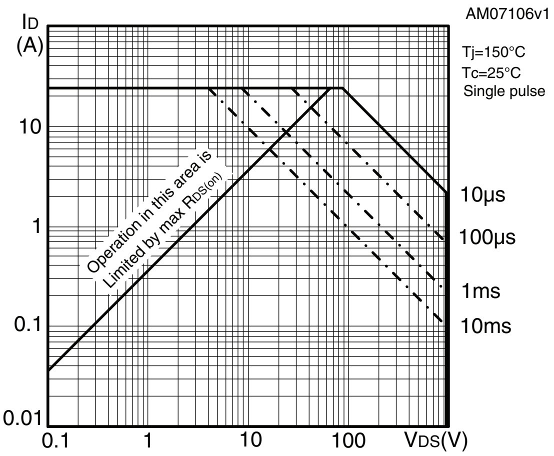


Figure 3. Thermal impedance

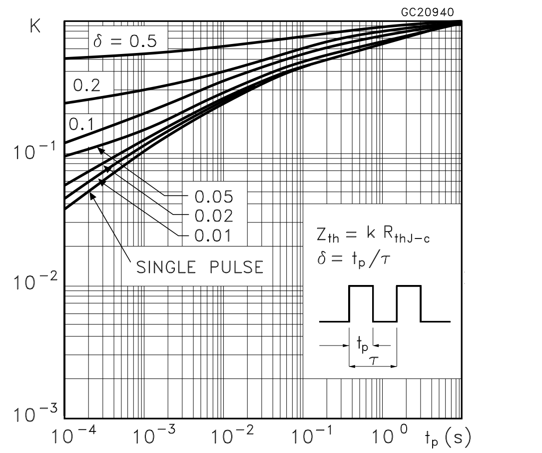


Figure 4. Output characteristics

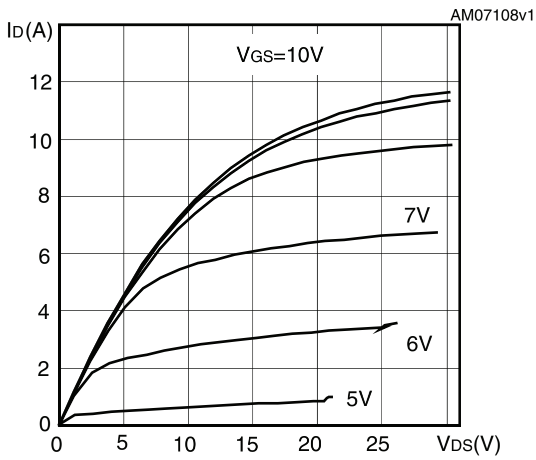


Figure 5. Transfer characteristics

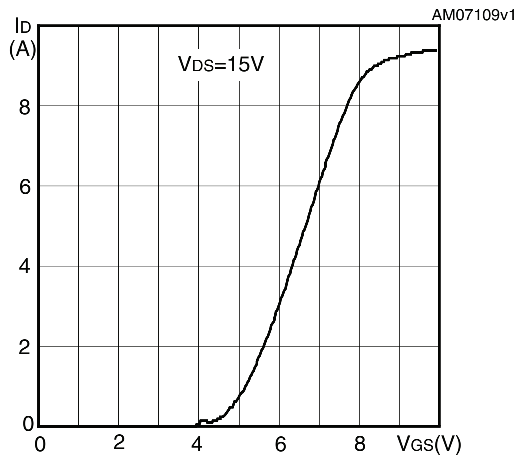


Figure 6. Gate charge vs gate-source voltage

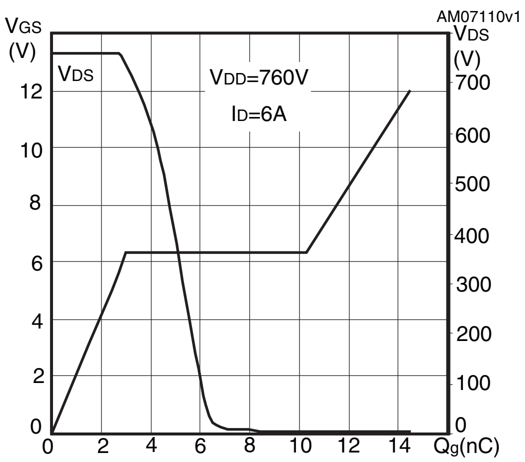


Figure 7. Static drain-source on-resistance

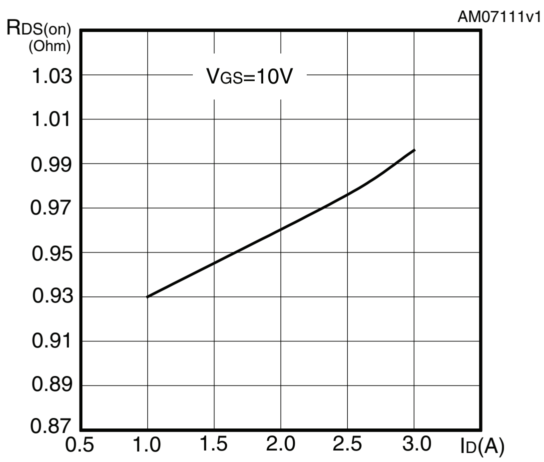


Figure 8. Capacitance variations

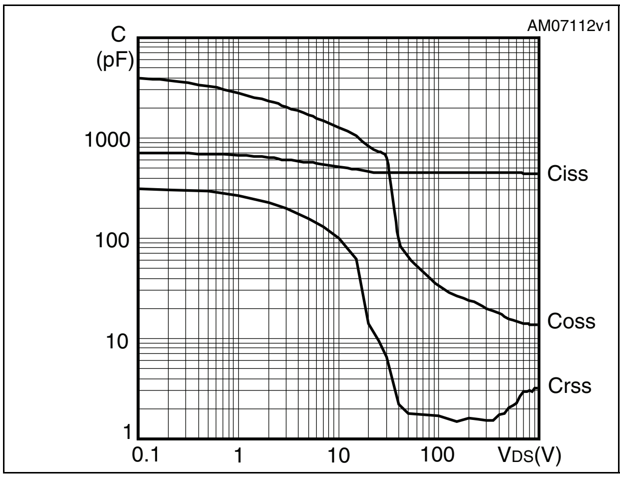


Figure 9. Output capacitance stored energy

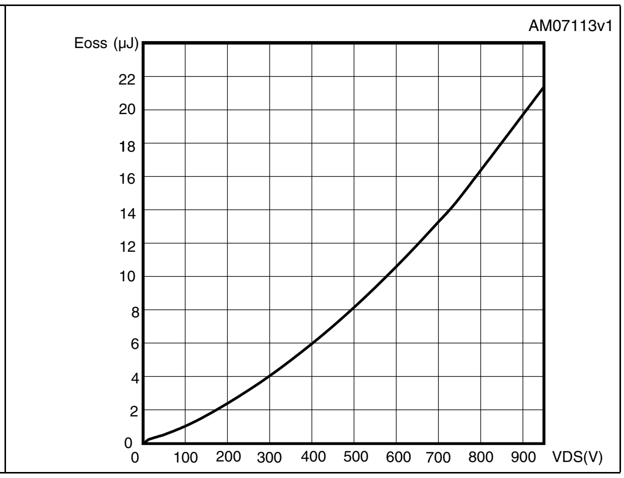


Figure 10. Normalized gate threshold voltage vs temperature

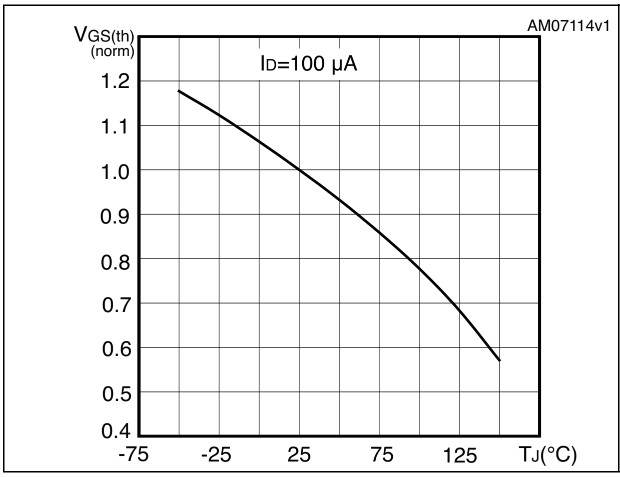


Figure 11. Normalized on-resistance vs temperature

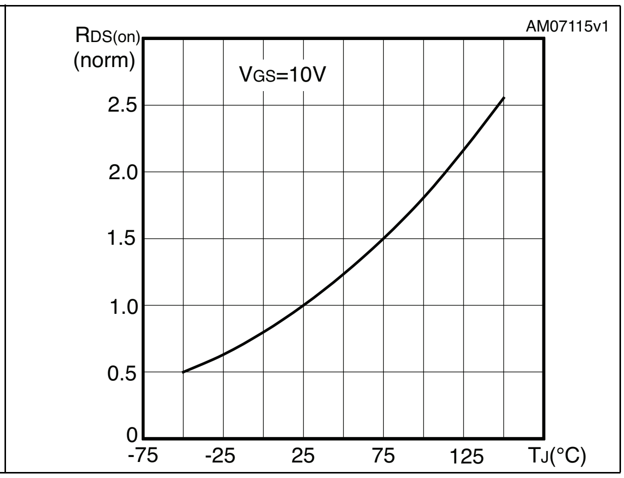


Figure 12. Source-drain diode forward characteristics

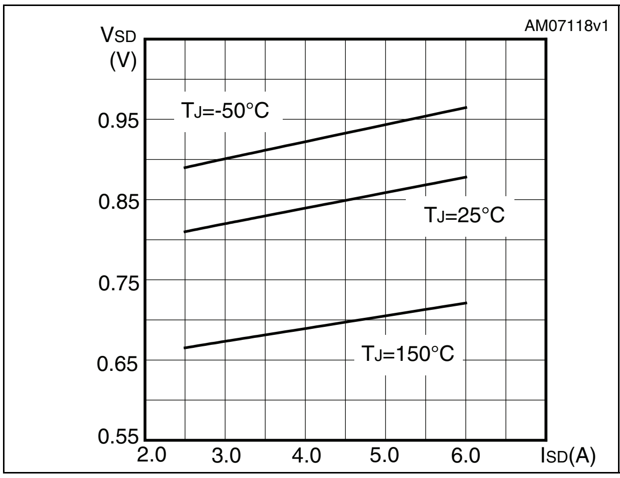


Figure 13. Normalized $V_{(BR)DSS}$ vs temperature

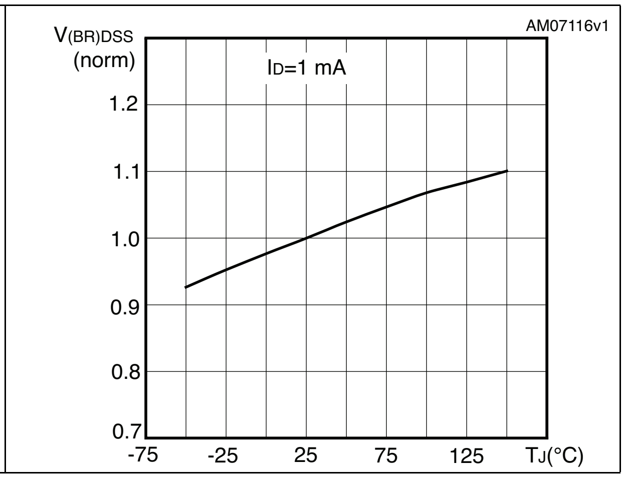
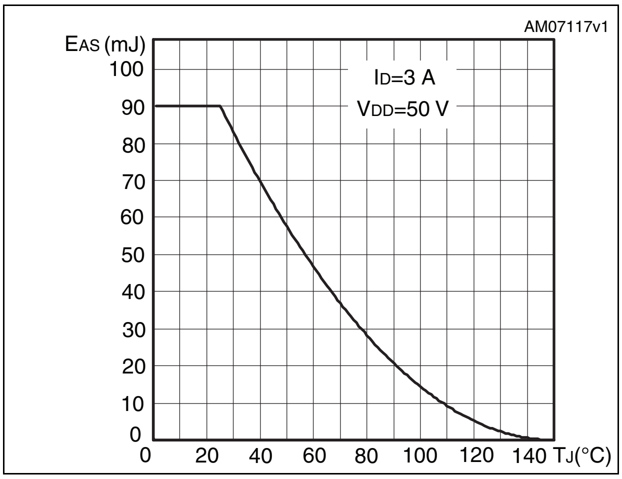


Figure 14. Maximum avalanche energy vs starting Tj



3 Test circuits

Figure 15. Switching times test circuit for resistive load

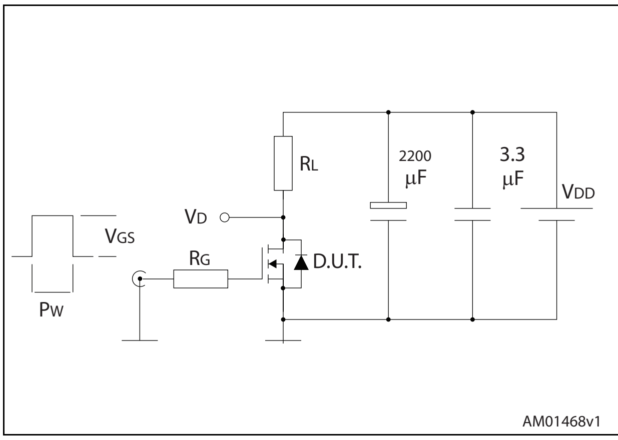


Figure 16. Gate charge test circuit

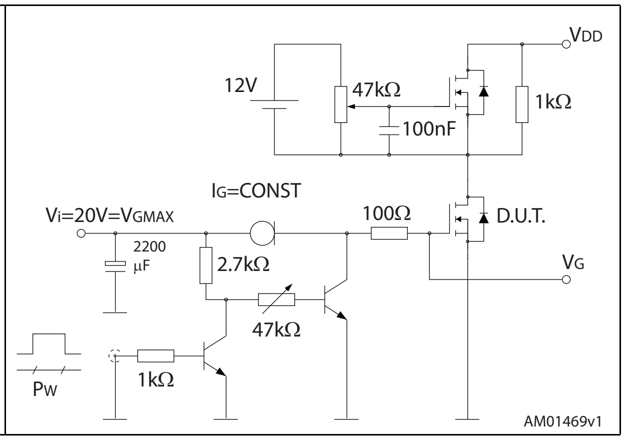


Figure 17. Test circuit for inductive load switching and diode recovery times

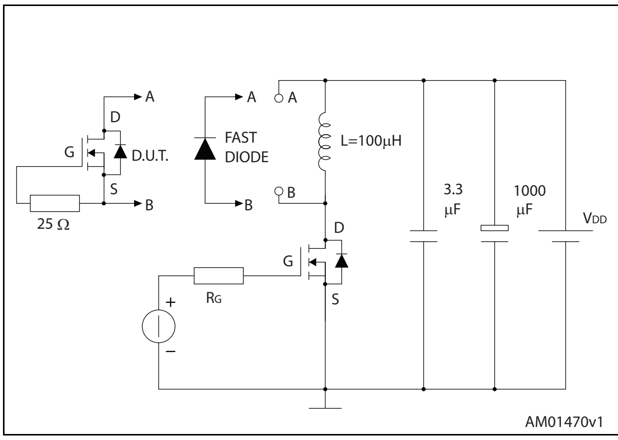


Figure 18. Unclamped inductive load test circuit

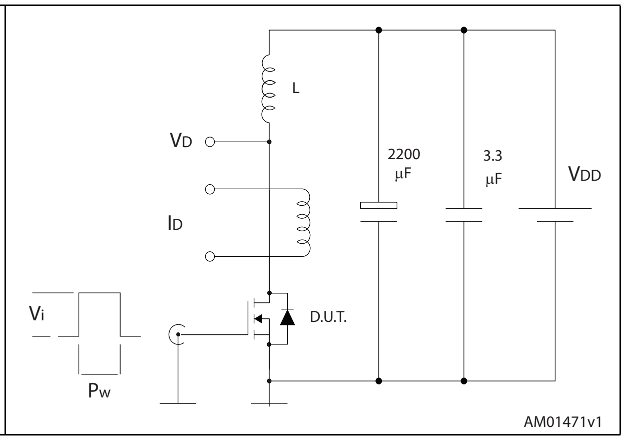


Figure 19. Unclamped inductive waveform

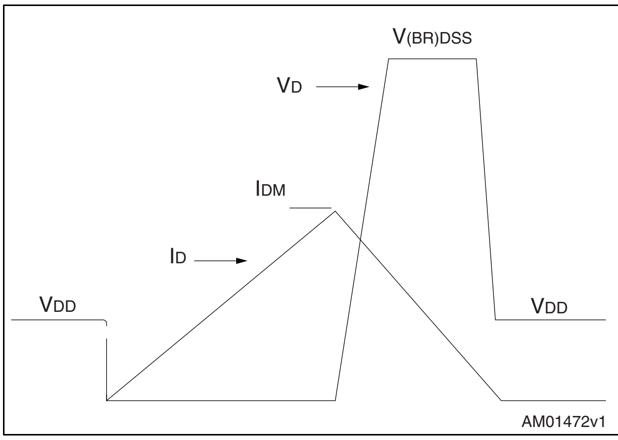
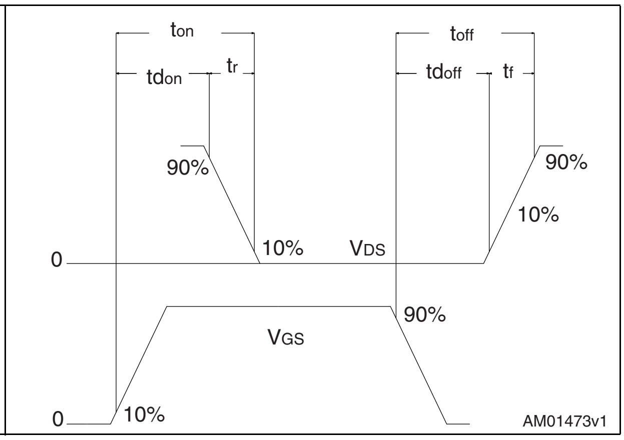


Figure 20. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 21. TO-220FP drawing

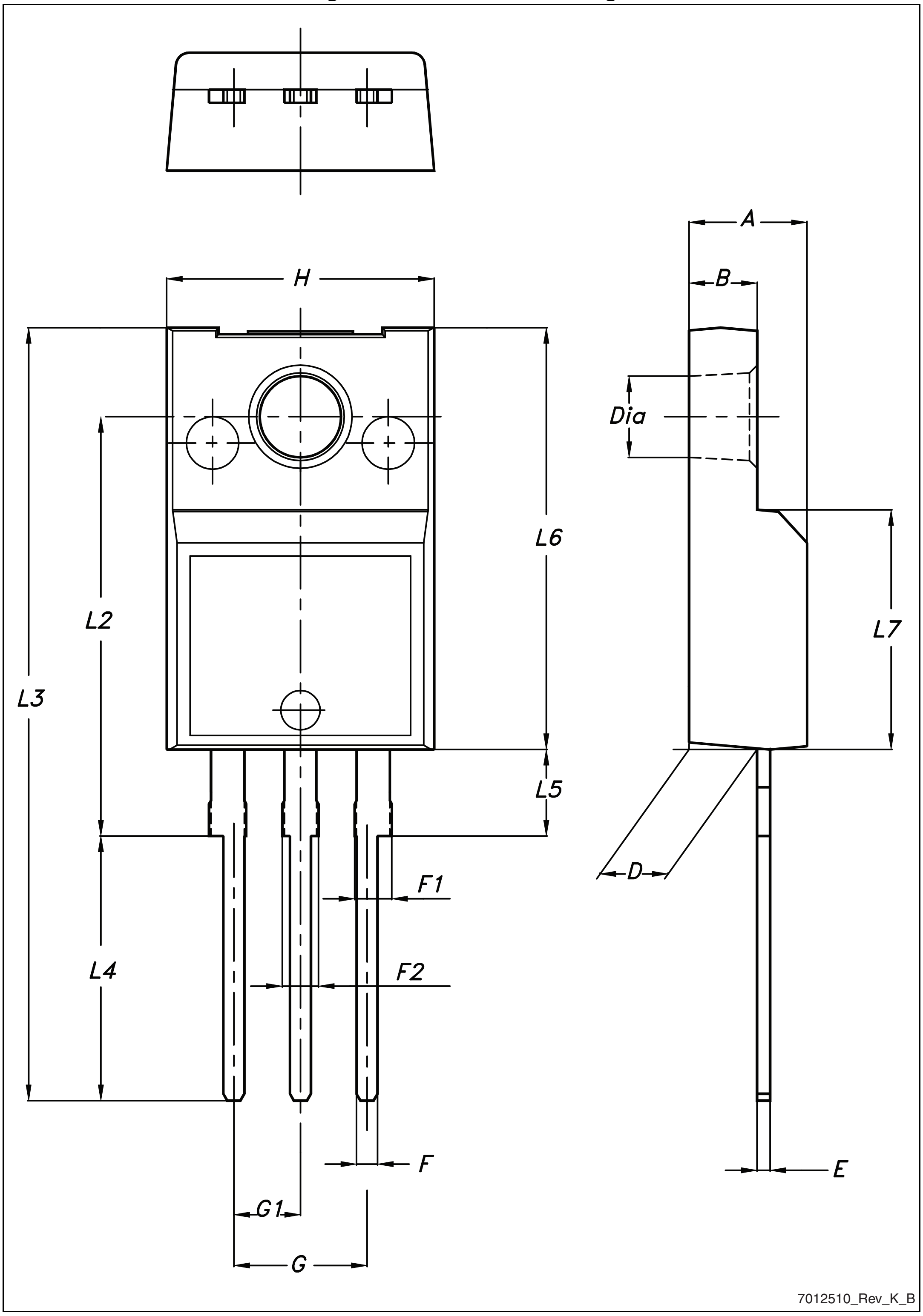


Table 9. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Ø	3		3.2

5 Revision history

Table 10. Document revision history

Date	Revision	Changes
27-May-2014	1	First release. Part number previously included in datasheet DocID16958
03-Sep-2015	2	Updated *Table 2.: Absolute maximum ratings* Minor text changes.