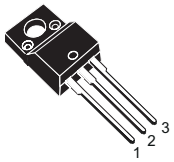
# STF7N60M2

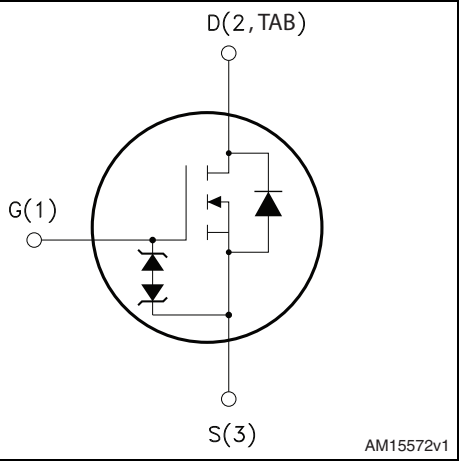
## N-channel 600 V, 0.86 Ω typ., 5 A MDmesh II Plus™ low $Q_g$ Power MOSFET in TO-220FP package

**Datasheet - production data**




**TO-220FP**

**Figure 1. Internal schematic diagram**




## Features

| Order code | $V_{DS}$ @ $T_{Jmax}$ | $R_{DS(on)}$ max | $I_D$ |
|---|---|---|---|
| STF7N60M2 | 650 V | 0.95 Ω | 5 A |

- Extremely low gate charge
- Lower $R_{DS(on)}$ x area vs previous generation
- Low gate input resistance
- 100% avalanche tested
- Zener-protected

## Applications

- Switching applications

## Description

This device is an N-channel Power MOSFET developed using a new generation of MDmesh™ technology: MDmesh II Plus™ low $Q_g$. This revolutionary Power MOSFET associates a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

**Table 1. Device summary**

| Order code | Marking | Package | Packaging |
|---|---|---|---|
| STF7N60M2 | 7N60M2 | TO-220FP | Tube |

# Contents

# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{GS}$ | Gate-source voltage | ± 25 | V |
| $I_D$ | Drain current (continuous) at $T_C$ = 25 °C | 5(1) | A |
| $I_D$ | Drain current (continuous) at $T_C$ = 100 °C | 3.5(1) | A |
| $I_{DM}$ (1) | Drain current (pulsed) | 20(1) | A |
| $P_{TOT}$ | Total dissipation at $T_C$ = 25 °C | 20 | W |
| $V_{ISO}$ | Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s; $T_C$=25 °C) | 2500 | V |
| dv/dt (2) | Peak diode recovery voltage slope | 15 | V/ns |
| dv/dt(3) | MOSFET dv/dt ruggedness | 50 | |
| $T_{stg}$ | Storage temperature | - 55 to 150 | °C |
| $T_j$ | Max. operating junction temperature | | |

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq 5$ A, di/dt $\leq$ 400 A/µs; $V_{DS\ peak} < V_{(BR)DSS}$, $V_{DD}$=400 V
3. $V_{DS} \leq$ 480 V

**Table 3. Thermal data**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{thj\text{-}case}$ | Thermal resistance junction-case max | 6.25 | °C/W |
| $R_{thj\text{-}amb}$ | Thermal resistance junction-ambient max | 62.5 | °C/W |

**Table 4. Avalanche characteristics**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $I_{AR}$ | Avalanche current, repetitive or not repetitive (pulse width limited by $T_{jmax}$ ) | 1.5 | A |
| $E_{AS}$ | Single pulse avalanche energy (starting $T_j$=25°C, $I_D$= $I_{AR}$; $V_{DD}$=50) | 99 | mJ |

# 2 Electrical characteristics

($T_C$ = 25 °C unless otherwise specified)

**Table 5. On /off states**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $I_D$ = 1 mA, $V_{GS}$ = 0 | 600 | | | V |
| $I_{DSS}$ | Zero gate voltage drain current ($V_{GS}$ = 0) | $V_{DS}$ = 600 V<br>$V_{DS}$ = 600 V, $T_C$=125 °C | | | 1<br>100 | µA<br>µA |
| $I_{GSS}$ | Gate-body leakage current ($V_{DS}$ = 0) | $V_{GS}$ = ± 25 V | | | ±10 | µA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | 2 | 3 | 4 | V |
| $R_{DS(on)}$ | Static drain-source on-resistance | $V_{GS}$ = 10 V, $I_D$ = 2.5 A | | 0.86 | 0.95 | Ω |

**Table 6. Dynamic**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $C_{iss}$ | Input capacitance | $V_{DS}$ = 100 V, f = 1 MHz, $V_{GS}$ = 0 | - | 271 | - | pF |
| $C_{oss}$ | Output capacitance | | - | 15.7 | - | pF |
| $C_{rss}$ | Reverse transfer capacitance | | - | 0.68 | - | pF |
| $C_{oss\ eq.}$ (1) | Equivalent output capacitance | $V_{DS}$ = 0 to 480 V, $V_{GS}$ = 0 | - | 75.5 | - | pF |
| $R_G$ | Intrinsic gate resistance | f = 1 MHz open drain | - | 7.2 | - | Ω |
| $Q_g$ | Total gate charge | $V_{DD}$ = 480 V, $I_D$ = 5 A, $V_{GS}$ = 10 V (see *Figure 15*) | - | 8.8 | - | nC |
| $Q_{gs}$ | Gate-source charge | | - | 1.8 | - | nC |
| $Q_{gd}$ | Gate-drain charge | | - | 4.3 | - | nC |

1. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as $C_{oss}$ when $V_{DS}$ increases from 0 to 80% $V_{DSS}$

**Table 7. Switching times**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{d(on)}$ | Turn-on delay time | $V_{DD}$ = 300 V, $I_D$ = 2.5 A, $R_G$ = 4.7 Ω, $V_{GS}$ = 10 V (see *Figure 14* and *19*) | - | 7.6 | - | ns |
| $t_r$ | Rise time | | - | 7.2 | - | ns |
| $t_{d(off)}$ | Turn-off delay time | | - | 19.3 | - | ns |
| $t_f$ | Fall time | | - | 15.9 | - | ns |

**Table 8. Source drain diode**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{SD}$<br>$I_{SDM}$ (1) | Source-drain current<br>Source-drain current (pulsed) | | - | | 5<br>20 | A<br>A |
| $V_{SD}$ (2) | Forward on voltage | $I_{SD}$ = 5 A, $V_{GS}$ = 0 | - | | 1.6 | V |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$ = 5 A, di/dt = 100 A/µs<br>$V_{DD}$ = 60 V (see *Figure 19*) | - | 275 | | ns |
| $Q_{rr}$ | Reverse recovery charge | | - | 1.55 | | nC |
| $I_{RRM}$ | Reverse recovery current | | - | 11 | | A |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$ = 5 A, di/dt = 100 A/µs<br>$V_{DD}$ = 60 V, $T_j$ = 150 °C<br>(see *Figure 19*) | - | 376 | | ns |
| $Q_{rr}$ | Reverse recovery charge | | - | 2.1 | | nC |
| $I_{RRM}$ | Reverse recovery current | | - | 11 | | A |

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

**Figure 2. Safe operating area**

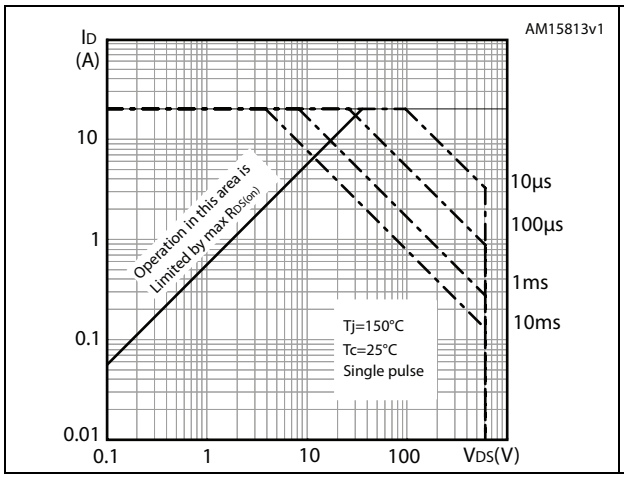



**Figure 3. Thermal impedance**

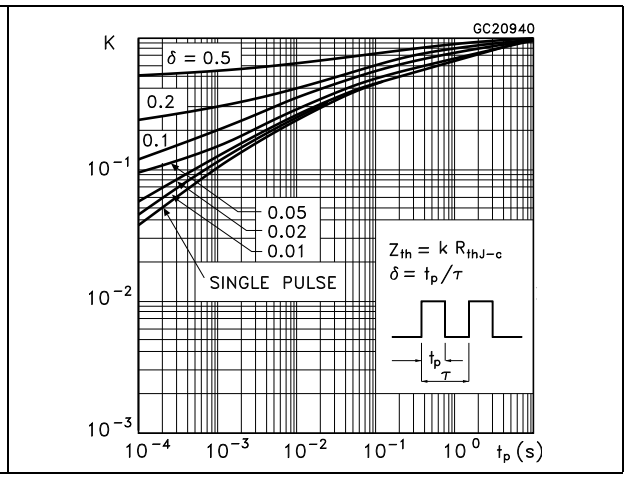



**Figure 4. Output characteristics**

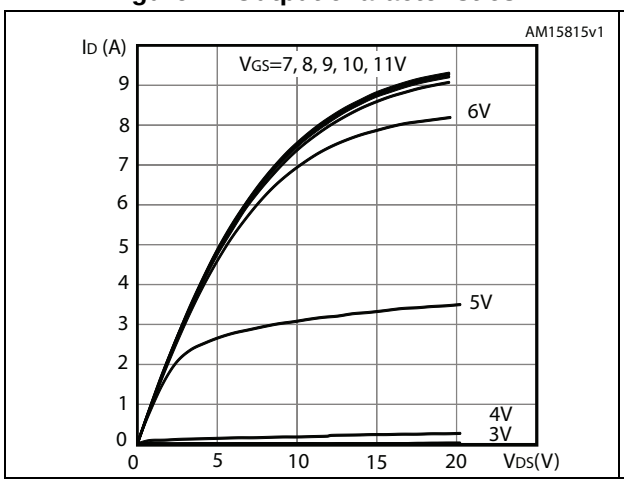



**Figure 5. Transfer characteristics**

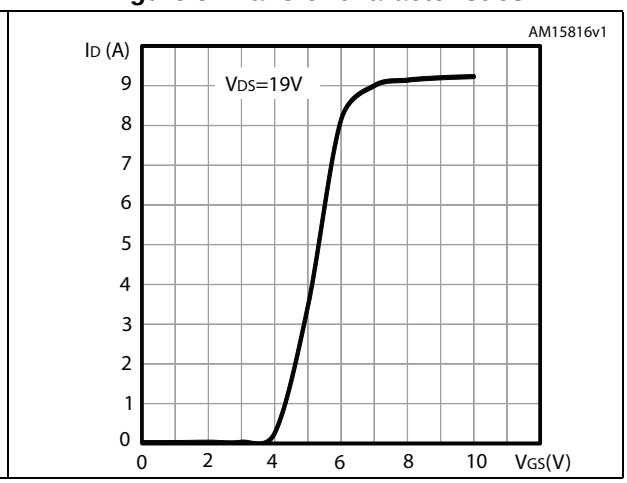



**Figure 6. Gate charge vs gate-source voltage**

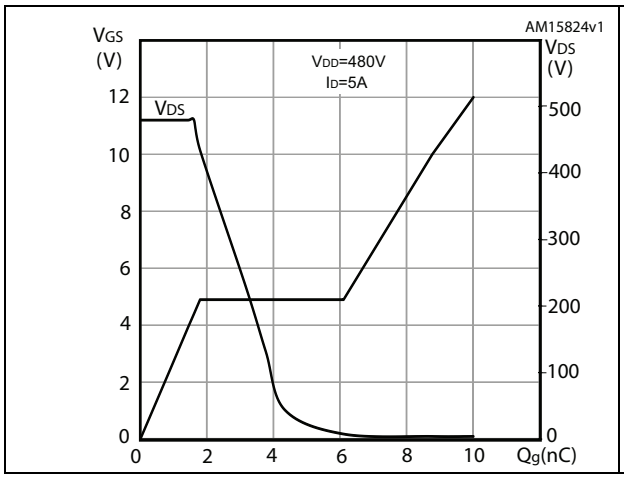



**Figure 7. Static drain-source on-resistance**

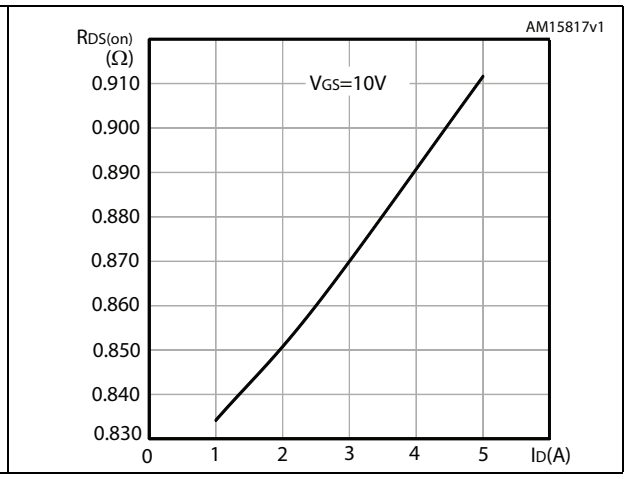


**Figure 8. Capacitance variations**

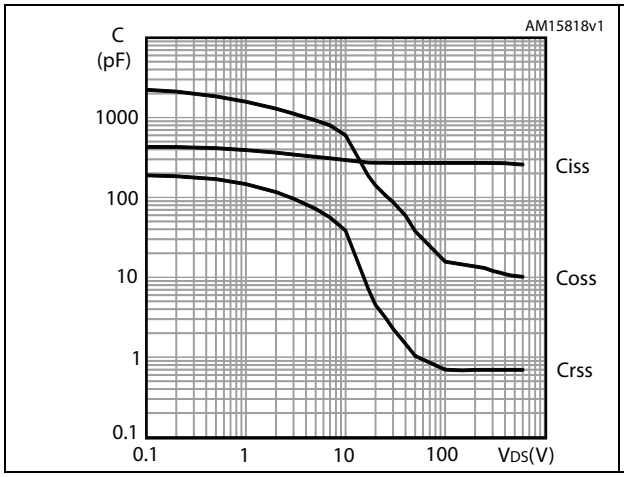



**Figure 9. Output capacitance stored energy**

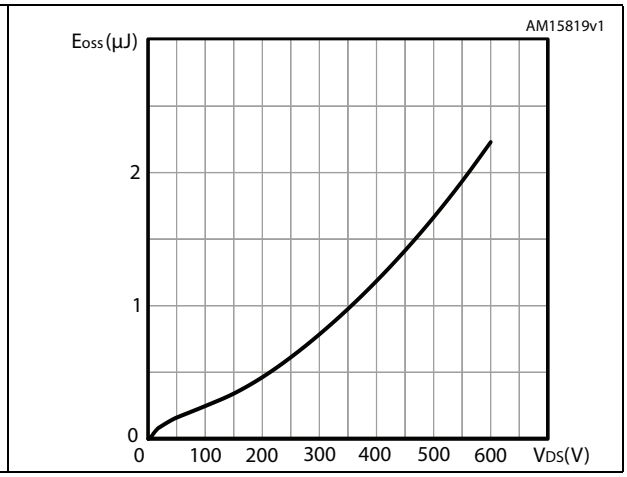



**Figure 10. Normalized gate threshold voltage vs. temperature**

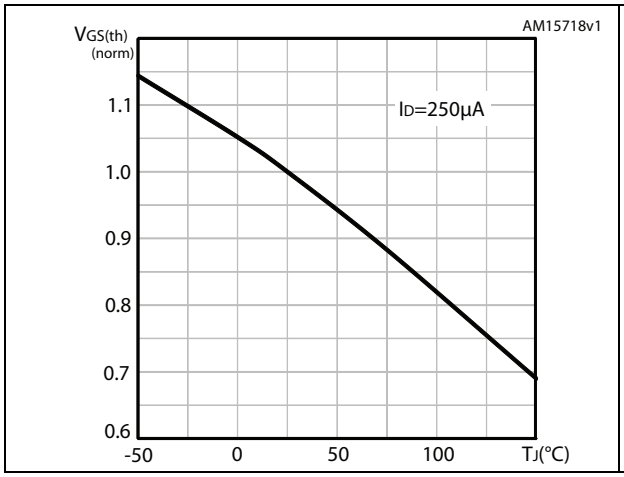



**Figure 11. Normalized on-resistance vs. temperature**

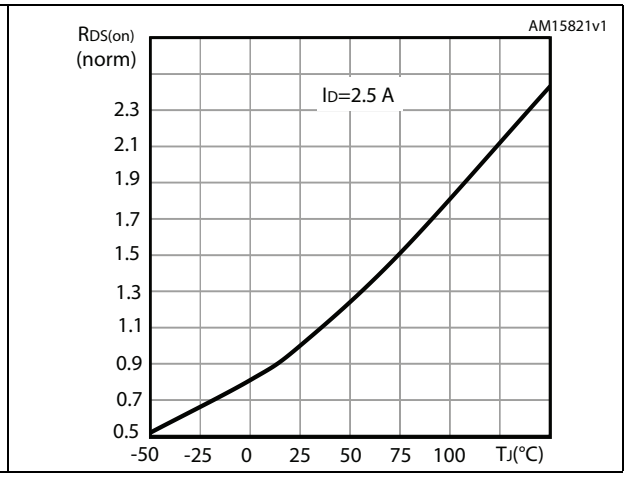



**Figure 12. Drain-source diode forward characteristics**

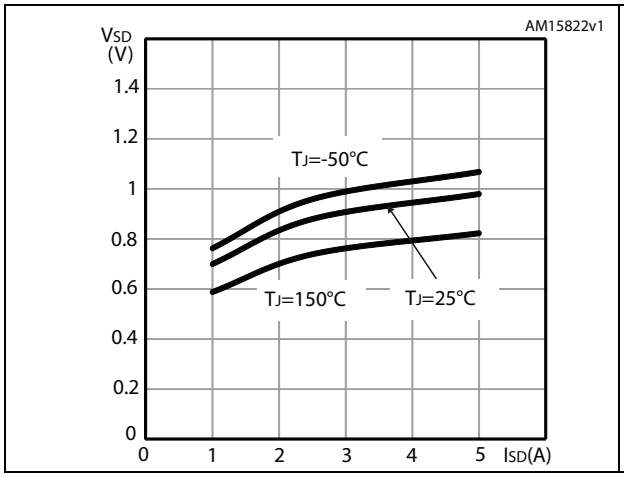
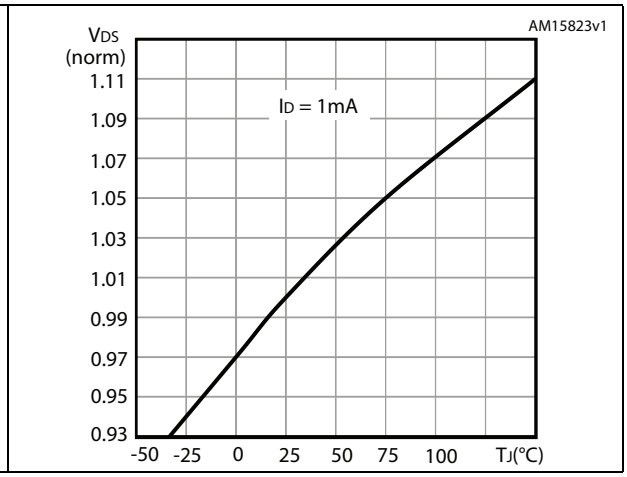



**Figure 13. Normalized $V_{DS}$ vs. temperature**



# 3 Test circuits

**Figure 14. Switching times test circuit for resistive load**

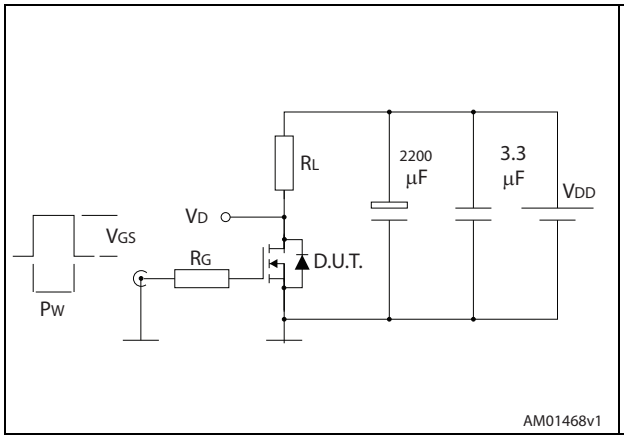



**Figure 15. Gate charge test circuit**

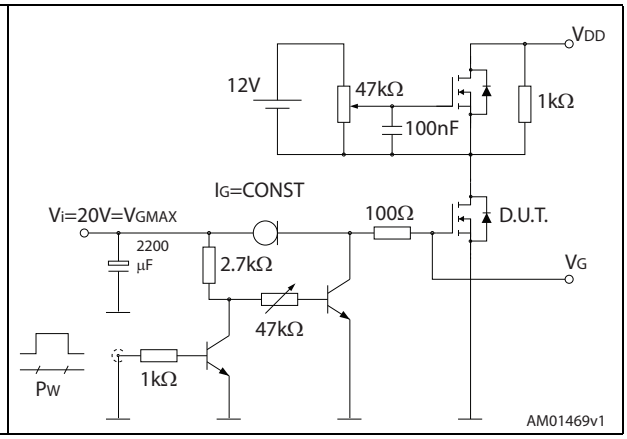



**Figure 16. Test circuit for inductive load switching and diode recovery times**

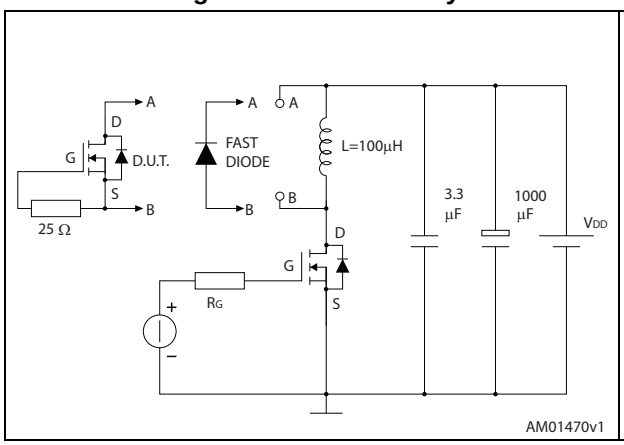



**Figure 17. Unclamped inductive load test circuit**

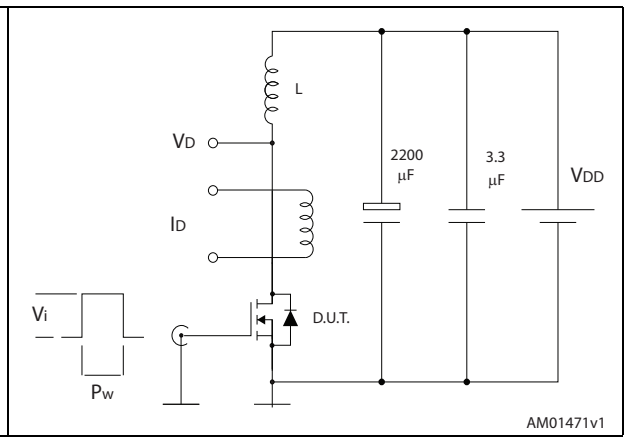



**Figure 18. Unclamped inductive waveform**

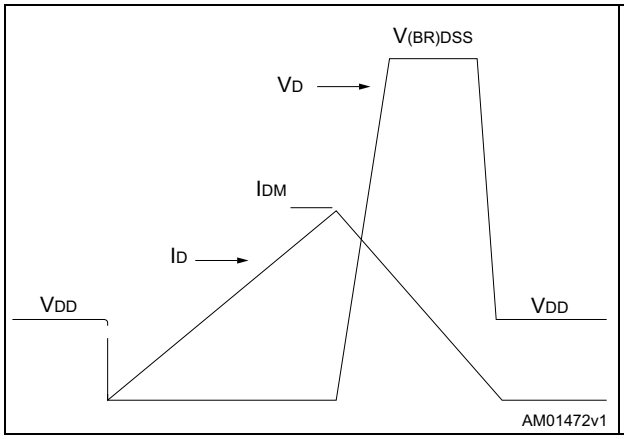
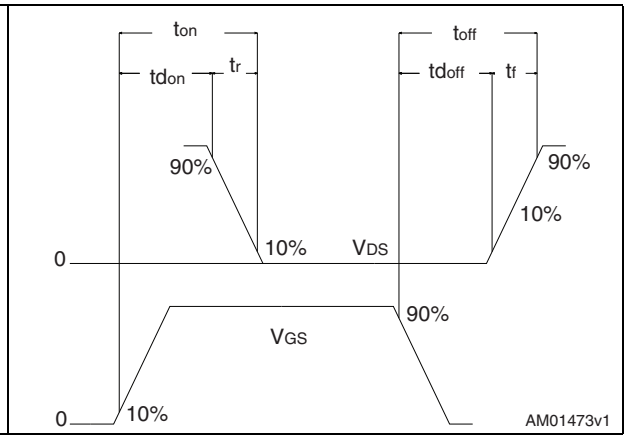



**Figure 19. Switching time waveform**



# 4 Package mechanical data

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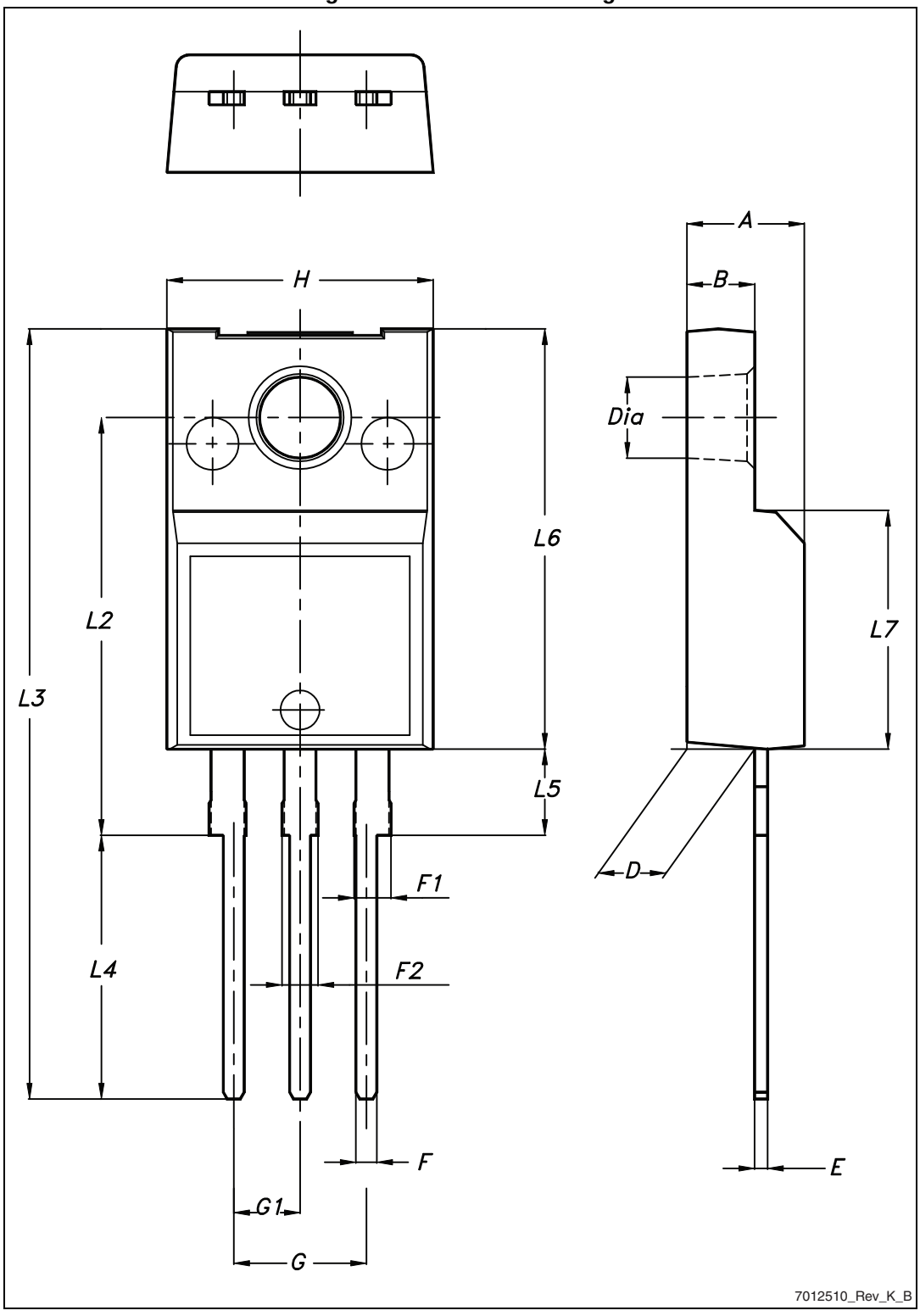
Table 9. TO-220FP mechanical data

| Dim. | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 4.4 | | 4.6 |
| B | 2.5 | | 2.7 |
| D | 2.5 | | 2.75 |
| E | 0.45 | | 0.7 |
| F | 0.75 | | 1 |
| F1 | 1.15 | | 1.70 |
| F2 | 1.15 | | 1.70 |
| G | 4.95 | | 5.2 |
| G1 | 2.4 | | 2.7 |
| H | 10 | | 10.4 |
| L2 | | 16 | |
| L3 | 28.6 | | 30.6 |
| L4 | 9.8 | | 10.6 |
| L5 | 2.9 | | 3.6 |
| L6 | 15.9 | | 16.4 |
| L7 | 9 | | 9.3 |
| Dia | 3 | | 3.2 |

Figure 20. TO-220FP drawing



# 5 Revision history

Table 10. Document revision history

| Date | Revision | Changes |
|---|---|---|
| 26-Jun-2013 | 1 | First release. |

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