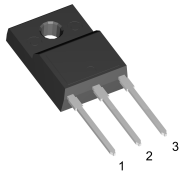
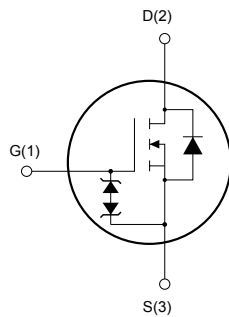


N-channel 600 V, 0.255 Ω typ., 13 A MDmesh M2 Power MOSFET in a TO-220FP wide creepage package



TO-220FP wide creepage



AM15572v1_no_tab



Features

| Order code | $V_{DS} @ T_{Jmax}$ | $R_{DS(on)}$ max. | I_D |
|-------------|---------------------|-------------------|-------|
| STFH18N60M2 | 650 V | 0.280 Ω | 13 A |

- Extremely low gate charge
- Excellent output capacitance (C_{OSS}) profile
- 100% avalanche tested
- Zener-protected
- Wide distance of 4.25 mm between the pins

Applications

- Switching applications
- LCC converters
- Resonant converters

Description

This device is an N-channel Power MOSFET developed using MDmesh M2 technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance and optimized switching characteristics, rendering it suitable for the most demanding high efficiency converters.

The TO-220FP wide creepage package provides increased surface insulation for Power MOSFETs to prevent failure due to arcing, which can occur in polluted environments.

Product status link

[STFH18N60M2](#)

Product summary

| | |
|-------------------|------------------------|
| Order code | STFH18N60M2 |
| Marking | 18N60M2 |
| Package | TO-220FP wide creepage |
| Packing | Tube |

1 Electrical ratings

Table 1. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|----------------|---|------------|------------------|
| V_{GS} | Gate-source voltage | ± 25 | V |
| $I_D^{(1)}$ | Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$ | 13 | A |
| | Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$ | 8 | A |
| $I_{DM}^{(2)}$ | Drain current (pulsed) | 52 | A |
| P_{TOT} | Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$ | 25 | W |
| $dv/dt^{(3)}$ | Peak diode recovery voltage slope | 15 | V/ns |
| $dv/dt^{(4)}$ | MOSFET dv/dt ruggedness | 50 | V/ns |
| V_{ISO} | Insulation withstand voltage (RMS) from all three leads to external heat sink ($t = 1\text{ s}$; $T_C = 25\text{ }^\circ\text{C}$) | 2.5 | kV |
| T_{stg} | Storage temperature range | -55 to 150 | $^\circ\text{C}$ |
| T_j | Operating junction temperature range | | |

- Limited by maximum junction temperature.
- Pulse width limited by safe operating area.
- $I_{SD} \leq 13\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$; $V_{DS(peak)} < V_{(BR)DSS}$, $V_{DD} = 400\text{ V}$
- $V_{DS} \leq 480\text{ V}$

Table 2. Thermal data

| Symbol | Parameter | Value | Unit |
|----------------|-------------------------------------|-------|---------------------------|
| $R_{thj-case}$ | Thermal resistance junction-case | 5 | $^\circ\text{C}/\text{W}$ |
| $R_{thj-amb}$ | Thermal resistance junction-ambient | 62.5 | $^\circ\text{C}/\text{W}$ |

Table 3. Avalanche characteristics

| Symbol | Parameter | Value | Unit |
|----------|--|-------|------|
| I_{AR} | Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax}) | 3 | A |
| E_{AS} | Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$) | 135 | mJ |

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified).

Table 4. On /off states

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------|-----------------------------------|--|------|-------|----------|---------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $I_D = 1\text{ mA}$, $V_{GS} = 0\text{ V}$ | 600 | | | V |
| I_{DSS} | Zero gate voltage drain current | $V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$ | | | 1 | μA |
| | | $V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$, $T_C = 125\text{ °C}$ ⁽¹⁾ | | | 100 | μA |
| I_{GSS} | Gate-body leakage current | $V_{DS} = 0\text{ V}$, $V_{GS} = \pm 25\text{ V}$ | | | ± 10 | μA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$ | 2 | 3 | 4 | V |
| $R_{DS(on)}$ | Static drain-source on-resistance | $V_{GS} = 10\text{ V}$, $I_D = 6.5\text{ A}$ | | 0.255 | 0.280 | Ω |

1. Defined by design, not subject to production test.

Table 5. Dynamic

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-------------------------------|-------------------------------|---|------|-------|------|----------|
| C_{iss} | Input capacitance | $V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$ | - | 791 | - | pF |
| C_{oss} | Output capacitance | | - | 40 | - | pF |
| C_{rSS} | Reverse transfer capacitance | | - | 1.3 | - | pF |
| $C_{oss\ eq.}$ ⁽¹⁾ | Equivalent output capacitance | $V_{DS} = 0$ to 480 V , $V_{GS} = 0\text{ V}$ | - | 164.5 | - | pF |
| R_G | Intrinsic gate resistance | $f = 1\text{ MHz}$, $I_D = 0\text{ A}$ | - | 5.6 | - | Ω |
| Q_g | Total gate charge | $V_{DD} = 480\text{ V}$, $I_D = 13\text{ A}$, $V_{GS} = 0$ to 10 V (see Figure 14. Test circuit for gate charge behavior) | - | 21.5 | - | nC |
| Q_{gs} | Gate-source charge | | - | 3.2 | - | nC |
| Q_{gd} | Gate-drain charge | | - | 11.3 | - | nC |

1. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 6. Switching times

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|--------------|---------------------|--|------|------|------|------|
| $t_{d(on)}$ | Turn-on delay time | $V_{DD} = 300\text{ V}$, $I_D = 6.5\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform) | - | 12 | - | ns |
| t_r | Rise time | | - | 9 | - | ns |
| $t_{d(off)}$ | Turn-off delay time | | - | 47 | - | ns |
| t_f | Fall time | | - | 10.6 | - | ns |

Table 7. Source drain diode

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------------|-------------------------------|--|------|------|------|---------------|
| I_{SD} | Source-drain current | | - | | 13 | A |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) | | - | | 52 | A |
| $V_{SD}^{(2)}$ | Forward on voltage | $I_{SD} = 13\text{ A}$, $V_{GS} = 0\text{ V}$ | - | | 1.6 | V |
| t_{rr} | Reverse recovery time | $I_{SD} = 13\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ | - | 305 | | ns |
| Q_{rr} | Reverse recovery charge | $V_{DD} = 60\text{ V}$ (see Figure 15. Test circuit for inductive load switching and diode recovery times) | - | 3.3 | | μC |
| I_{RRM} | Reverse recovery current | (see Figure 15. Test circuit for inductive load switching and diode recovery times) | - | 22 | | A |
| t_{rr} | Reverse recovery time | $I_{SD} = 13\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ | - | 417 | | ns |
| Q_{rr} | Reverse recovery charge | $V_{DD} = 60\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ | - | 4.6 | | μC |
| I_{RRM} | Reverse recovery current | (see Figure 15. Test circuit for inductive load switching and diode recovery times) | - | 22 | | A |

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

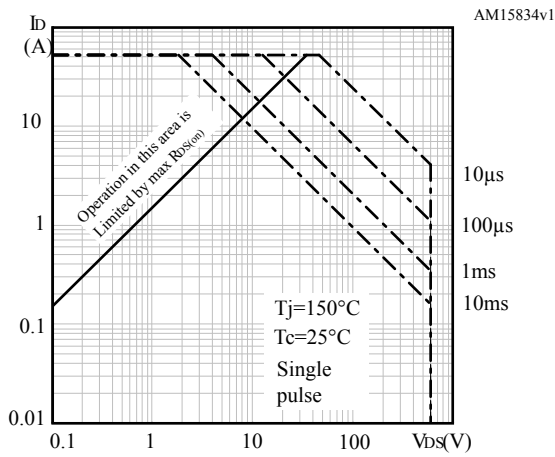


Figure 2. Thermal impedance

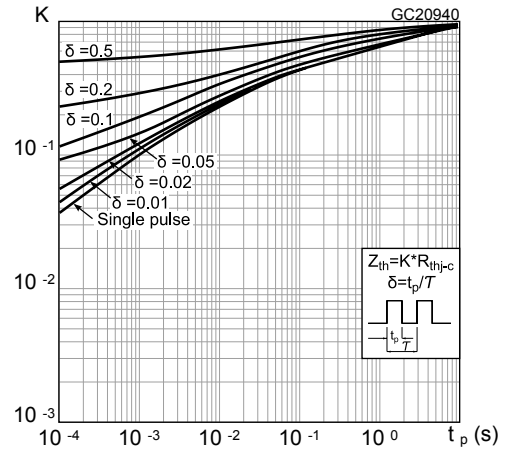


Figure 3. Output characteristics

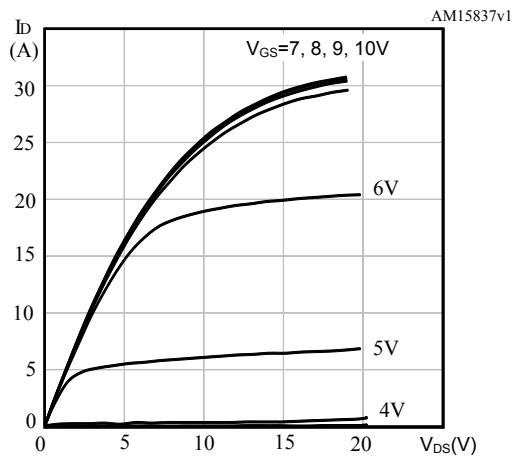


Figure 4. Transfer characteristics

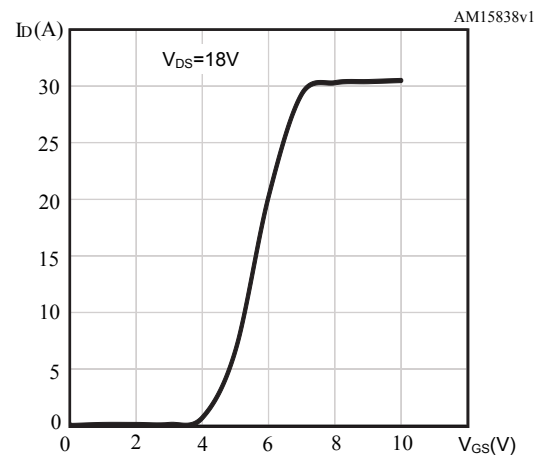


Figure 5. Gate charge vs gate-source voltage

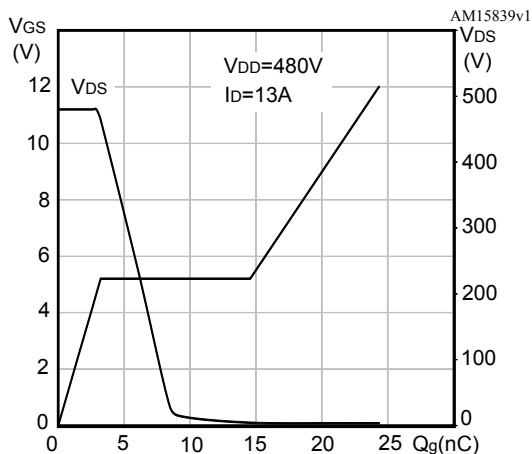


Figure 6. Static drain-source on-resistance

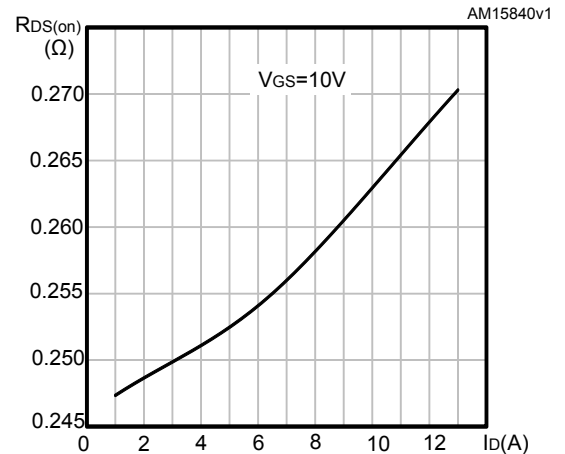


Figure 7. Capacitance variations

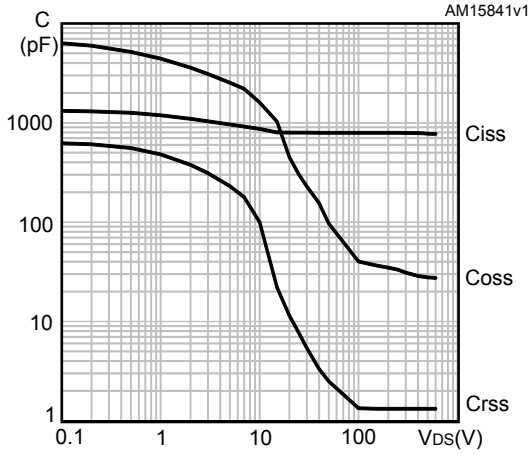


Figure 8. Normalized gate threshold voltage vs. temperature

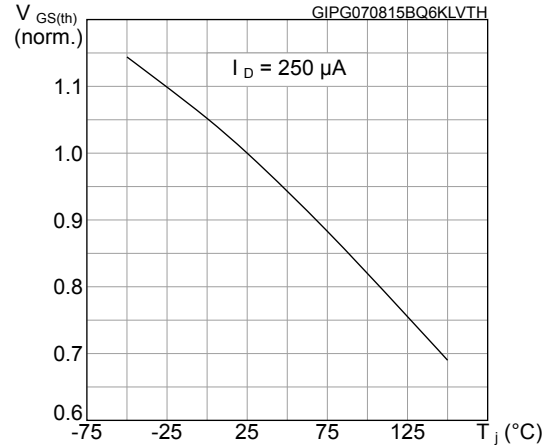


Figure 9. Normalized on-resistance vs temperature

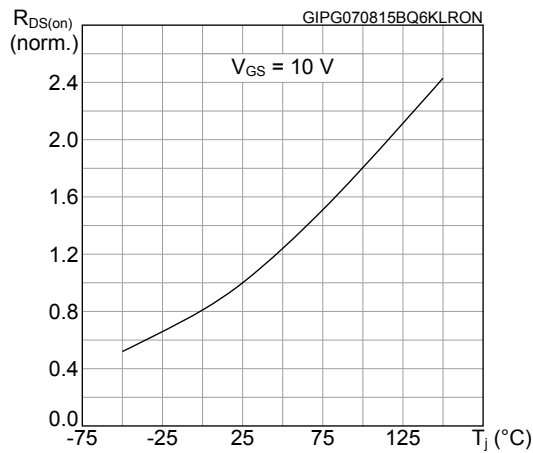


Figure 10. Source-drain diode forward characteristics

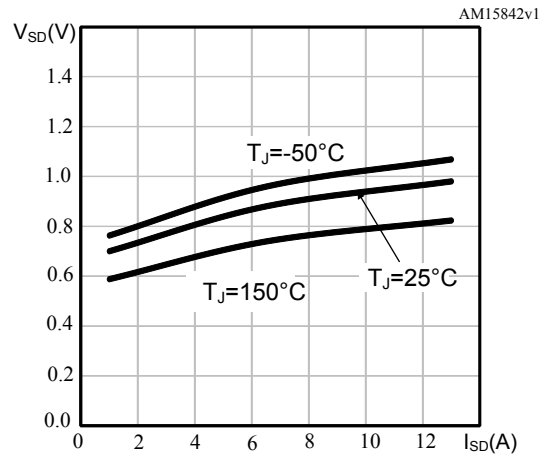


Figure 11. Normalized $V_{(BR)DSS}$ vs temperature

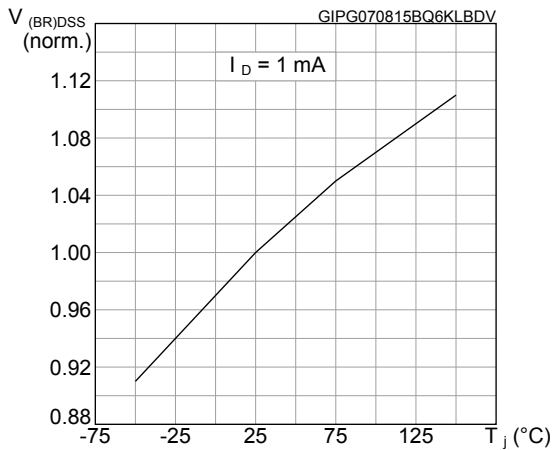
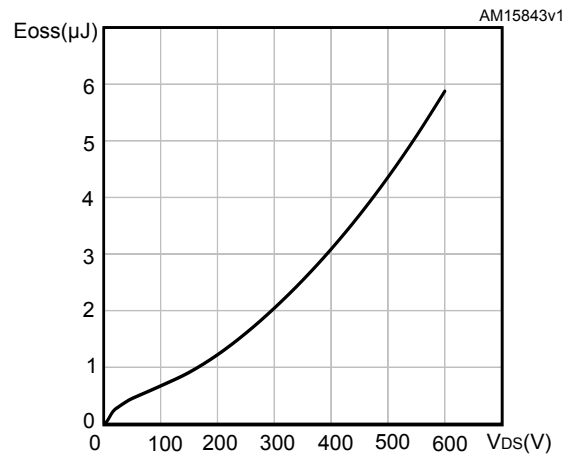
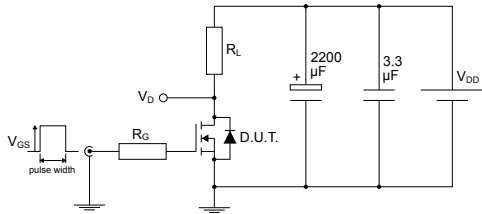


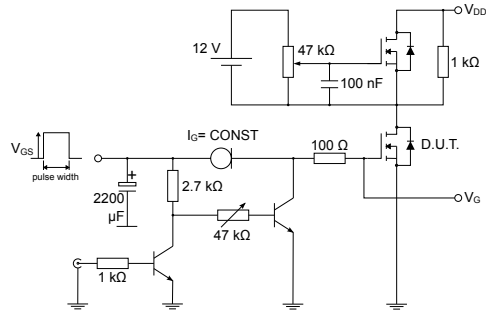
Figure 12. Output capacitance stored energy



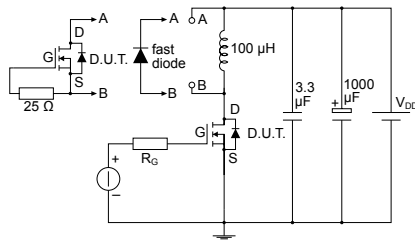
3 Test circuits

Figure 13. Test circuit for resistive load switching times


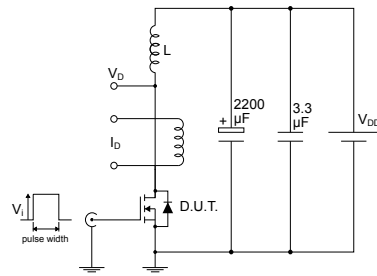
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Figure 14. Test circuit for gate charge behavior


AM01469v1

Figure 15. Test circuit for inductive load switching and diode recovery times


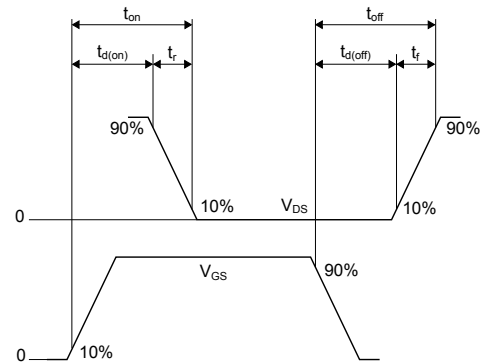
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Figure 16. Unclamped inductive load test circuit


AM01471v1

Figure 17. Unclamped inductive waveform


AM01472v1

Figure 18. Switching time waveform


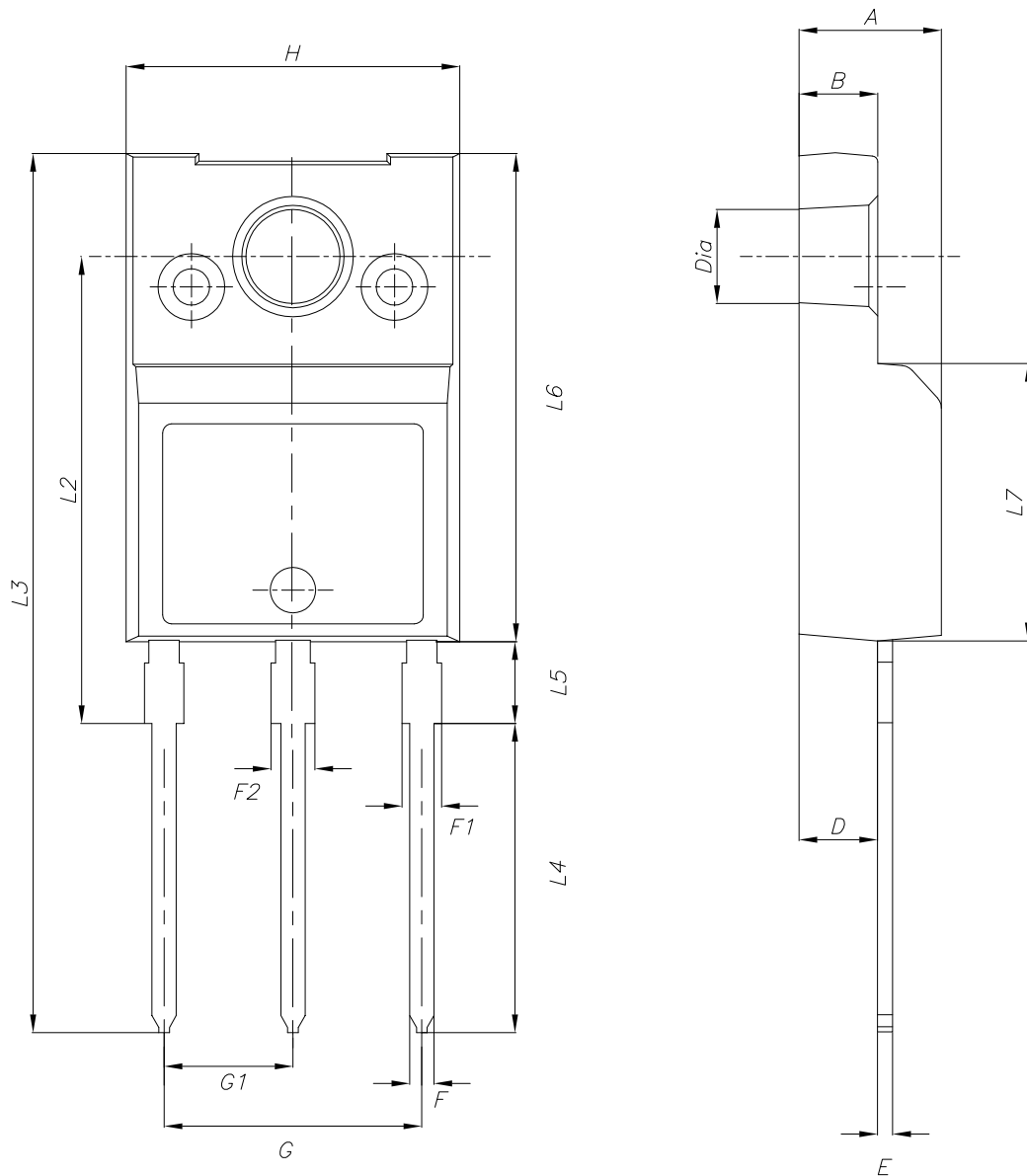
AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-220FP wide creepage package information

Figure 19. TO-220FP wide creepage package outline



DM00260252_1

Table 8. TO-220FP wide creepage package mechanical data

| Dim. | mm | | |
|------|-------|-------|-------|
| | Min. | Typ. | Max. |
| A | 4.60 | 4.70 | 4.80 |
| B | 2.50 | 2.60 | 2.70 |
| D | 2.49 | 2.59 | 2.69 |
| E | 0.46 | | 0.59 |
| F | 0.76 | | 0.89 |
| F1 | 0.96 | | 1.25 |
| F2 | 1.11 | | 1.40 |
| G | 8.40 | 8.50 | 8.60 |
| G1 | 4.15 | 4.25 | 4.35 |
| H | 10.90 | 11.00 | 11.10 |
| L2 | 15.25 | 15.40 | 15.55 |
| L3 | 28.70 | 29.00 | 29.30 |
| L4 | 10.00 | 10.20 | 10.40 |
| L5 | 2.55 | 2.70 | 2.85 |
| L6 | 16.00 | 16.10 | 16.20 |
| L7 | 9.05 | 9.15 | 9.25 |
| Dia | 3.00 | 3.10 | 3.20 |

Revision history

Table 9. Document revision history

| Date | Revision | Changes |
|-------------|----------|--|
| 08-Jun-2016 | 1 | First release. |
| 16-Jun-2016 | 2 | Document status promoted from preliminary data to production data. Minor text changes. |
| 06-Jun-2019 | 3 | Modified Figure 8. Normalized gate threshold voltage vs. temperature, Figure 9. Normalized on-resistance vs temperature and Figure 11. Normalized $V_{(BR)DSS}$ vs temperature. Minor text changes. |

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