

## N-channel 800 V, 0.23 $\Omega$ typ., 16 A MDmesh™ K5 Power MOSFET in a TO-220FP ultra narrow leads package

Datasheet - production data

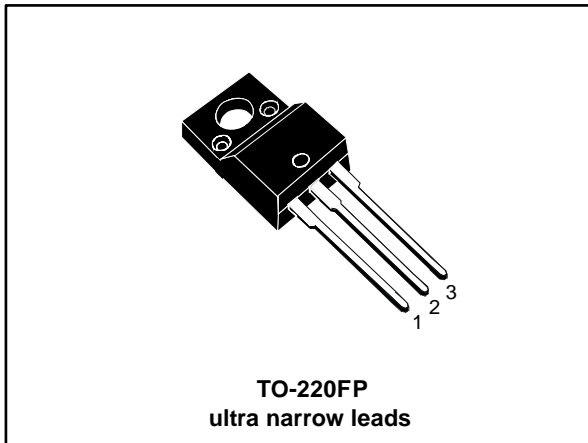
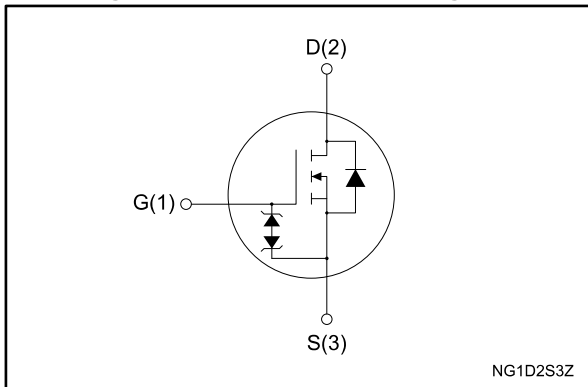


Figure 1: Internal schematic diagram



### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>	P <sub>TOT</sub>
STFU23N80K5	800 V	0.28 $\Omega$	16 A	35 W

- Industry's lowest R<sub>DS(on)</sub> x area
- Industry's best FoM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

### Applications

- Switching applications

### Description

This very high voltage N-channel Power MOSFET is designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Table 1: Device summary

Order code	Marking	Package	Packing
STFU23N80K5	23N80K5	TO-220FP ultra narrow leads	Tube

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## Contents

<b>1</b>	<b>Electrical ratings .....</b>	<b>3</b>
<b>2</b>	<b>Electrical characteristics .....</b>	<b>4</b>
	2.1 Electrical characteristics (curves).....	6
<b>3</b>	<b>Test circuits .....</b>	<b>8</b>
<b>4</b>	<b>Package information .....</b>	<b>9</b>
	4.1 TO-220FP ultra narrow leads package information.....	9
<b>5</b>	<b>Revision history .....</b>	<b>11</b>

# 1 Electrical ratings

**Table 2: Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	$\pm 30$	V
$I_D$	Drain current (continuous) at $T_{case} = 25\text{ }^\circ\text{C}$	16	A
	Drain current (continuous) at $T_{case} = 100\text{ }^\circ\text{C}$	10	
$I_{DM}^{(1)}$	Drain current (pulsed)	64	A
$P_{TOT}$	Total dissipation at $T_{case} = 25\text{ }^\circ\text{C}$	35	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	4.5	V/ns
$dv/dt^{(3)}$	MOSFET $dv/dt$ ruggedness	50	
$V_{ISO}$	Insulation withstand voltage (RMS) from all three leads to external heat sink ( $t = 1\text{ s}$ , $T_C = 25\text{ }^\circ\text{C}$ )	2500	V
$T_{stg}$	Storage temperature range	-55 to 150	$^\circ\text{C}$
$T_j$	Operating junction temperature range		

**Notes:**

(1) Pulse width is limited by safe operating area.

(2)  $I_{SD} \leq 16\text{ A}$ ,  $di/dt = 100\text{ A}/\mu\text{s}$ ,  $V_{DS\text{ peak}} < V_{(BR)DSS}$ ,  $V_{DD} = 80\% V_{(BR)DSS}$

(3)  $V_{DS} \leq 640\text{ V}$

**Table 3: Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	3.6	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient	50	

**Table 4: Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}^{(1)}$	Avalanche current, repetitive or not repetitive	5	A
$E_{AS}^{(2)}$	Single pulse avalanche energy	400	mJ

**Notes:**

(1) Pulse width limited by  $T_{jmax}$ .

(2) Starting  $T_j = 25\text{ }^\circ\text{C}$ ,  $I_D = I_{AR}$ ,  $V_{DD} = 50\text{ V}$ .

## 2 Electrical characteristics

( $T_{\text{case}} = 25\text{ °C}$  unless otherwise specified)

**Table 5: Static**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage	$V_{\text{GS}} = 0\text{ V}$ , $I_{\text{D}} = 1\text{ mA}$	800			V
$I_{\text{DSS}}$	Zero gate voltage drain current	$V_{\text{GS}} = 0\text{ V}$ , $V_{\text{DS}} = 800\text{ V}$			1	$\mu\text{A}$
		$V_{\text{GS}} = 0\text{ V}$ , $V_{\text{DS}} = 800\text{ V}$ , $T_{\text{case}} = 125\text{ °C}^{(1)}$			50	
$I_{\text{GSS}}$	Gate-body leakage current	$V_{\text{DS}} = 0\text{ V}$ , $V_{\text{GS}} = \pm 20\text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{\text{GS(th)}}$	Gate threshold voltage	$V_{\text{DS}} = V_{\text{GS}}$ , $I_{\text{D}} = 100\text{ }\mu\text{A}$	3	4	5	V
$R_{\text{DS(on)}}$	Static drain-source on-resistance	$V_{\text{GS}} = 10\text{ V}$ , $I_{\text{D}} = 8\text{ A}$		0.23	0.28	$\Omega$

**Notes:**

<sup>(1)</sup>Defined by design, not subject to production test.

**Table 6: Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{\text{iss}}$	Input capacitance	$V_{\text{DS}} = 100\text{ V}$ , $f = 1\text{ MHz}$ , $V_{\text{GS}} = 0\text{ V}$	-	1000	-	$\mu\text{F}$
$C_{\text{oss}}$	Output capacitance		-	65	-	
$C_{\text{rss}}$	Reverse transfer capacitance		-	1.5	-	
$C_{\text{O(tr)}}^{(1)}$	Equivalent output capacitance	$V_{\text{DS}} = 0\text{ to }640\text{ V}$ , $V_{\text{GS}} = 0\text{ V}$	-	165	-	$\mu\text{F}$
$C_{\text{O(er)}}^{(2)}$	Equivalent output capacitance	$V_{\text{DS}} = 0\text{ to }640\text{ V}$ , $V_{\text{GS}} = 0\text{ V}$	-	59	-	
$R_{\text{G}}$	Intrinsic gate resistance	$f = 1\text{ MHz}$ , $I_{\text{D}} = 0\text{ A}$	-	4.7	-	$\Omega$
$Q_{\text{g}}$	Total gate charge	$V_{\text{DD}} = 640\text{ V}$ , $I_{\text{D}} = 16\text{ A}$ , $V_{\text{GS}} = 0\text{ to }10\text{ V}$ (see <a href="#">Figure 14: "Test circuit for gate charge behavior"</a> )	-	33	-	nC
$Q_{\text{gs}}$	Gate-source charge		-	6	-	
$Q_{\text{gd}}$	Gate-drain charge		-	25	-	

**Notes:**

<sup>(1)</sup>Time related is defined as a constant equivalent capacitance giving the same charging time as  $C_{\text{oss}}$  when  $V_{\text{DS}}$  increases from 0 to 80%  $V_{\text{DSS}}$ .

<sup>(2)</sup>Energy related is defined as a constant equivalent capacitance giving the same stored energy as  $C_{\text{oss}}$  when  $V_{\text{DS}}$  increases from 0 to 80%  $V_{\text{DSS}}$ .

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 400\text{ V}$ , $I_D = 8\text{ A}$ $R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 13: "Test circuit for resistive load switching times"</a> and <a href="#">Figure 18: "Switching time waveform"</a> )	-	14	-	ns
$t_r$	Rise time		-	9	-	
$t_{d(off)}$	Turn-off delay time		-	48	-	
$t_f$	Fall time		-	9	-	

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		16	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		64	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$ , $I_{SD} = 16\text{ A}$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 16\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 60\text{ V}$ (see <a href="#">Figure 15: "Test circuit for inductive load switching and diode recovery times"</a> )	-	410		ns
$Q_{rr}$	Reverse recovery charge		-	7		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	34		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 16\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 60\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$ (see <a href="#">Figure 15: "Test circuit for inductive load switching and diode recovery times"</a> )	-	650		ns
$Q_{rr}$	Reverse recovery charge		-	10		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	32		A

**Notes:**

(1) Pulse width is limited by safe operating area.

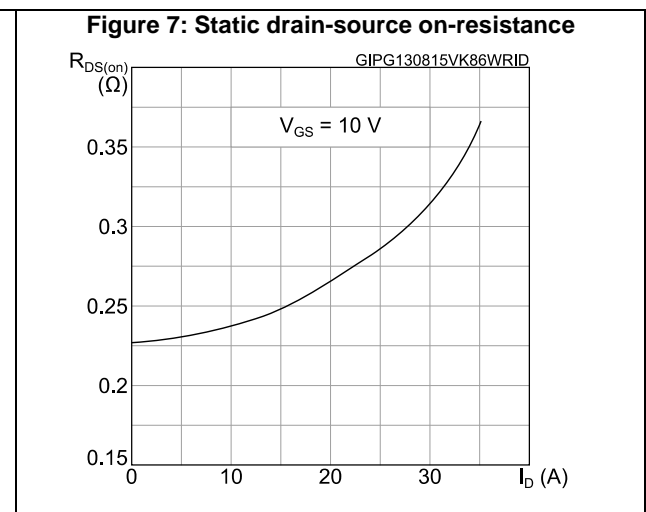
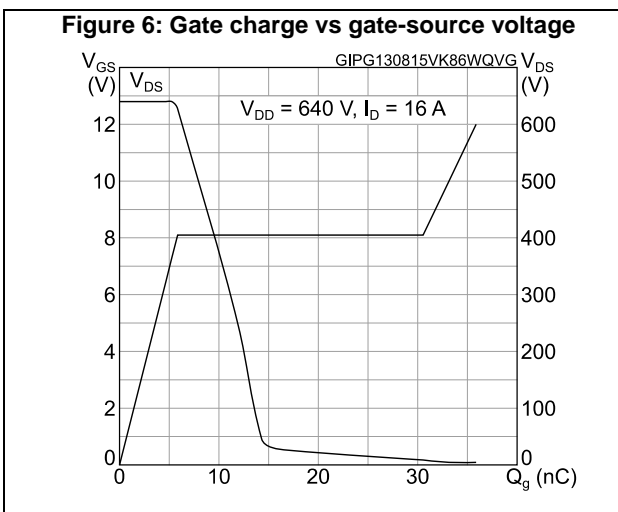
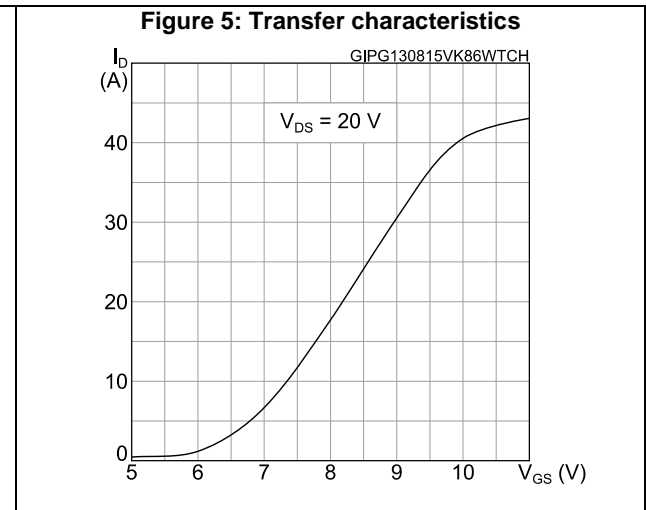
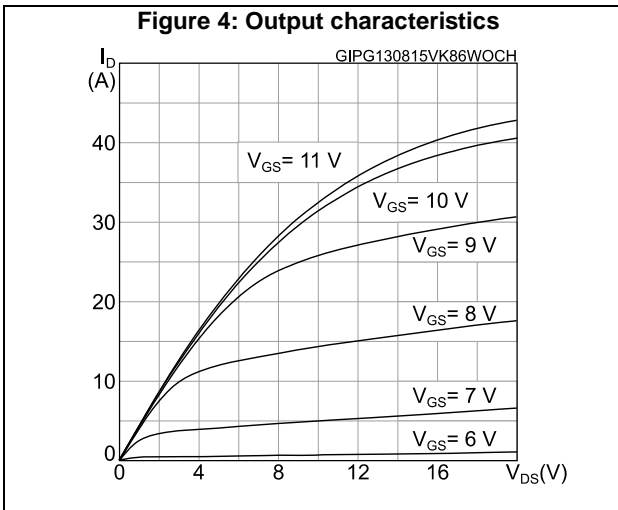
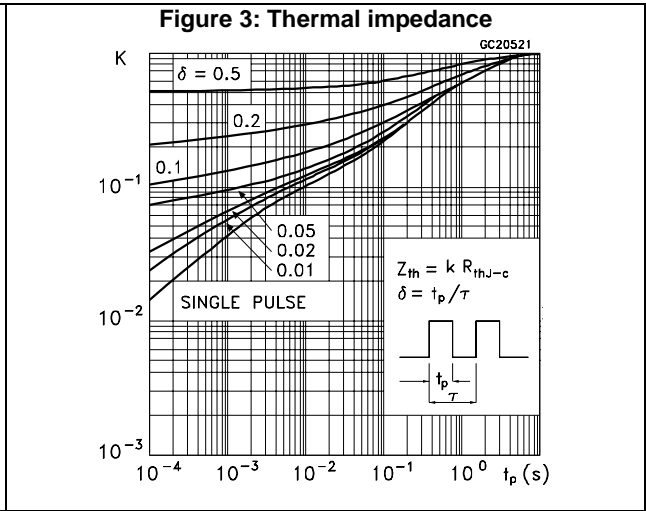
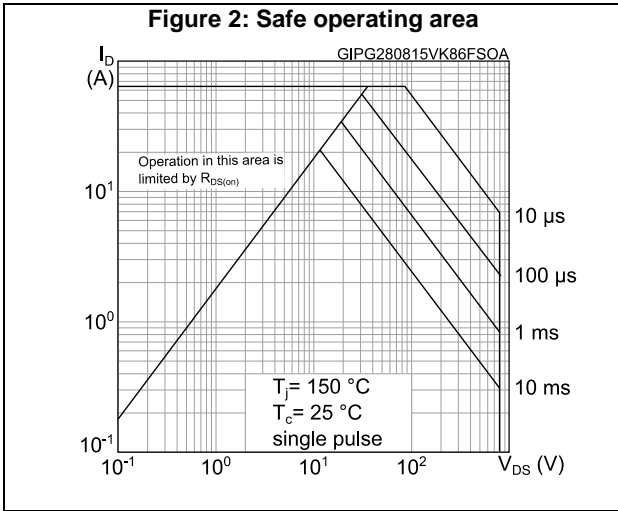
(2) Pulse test: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

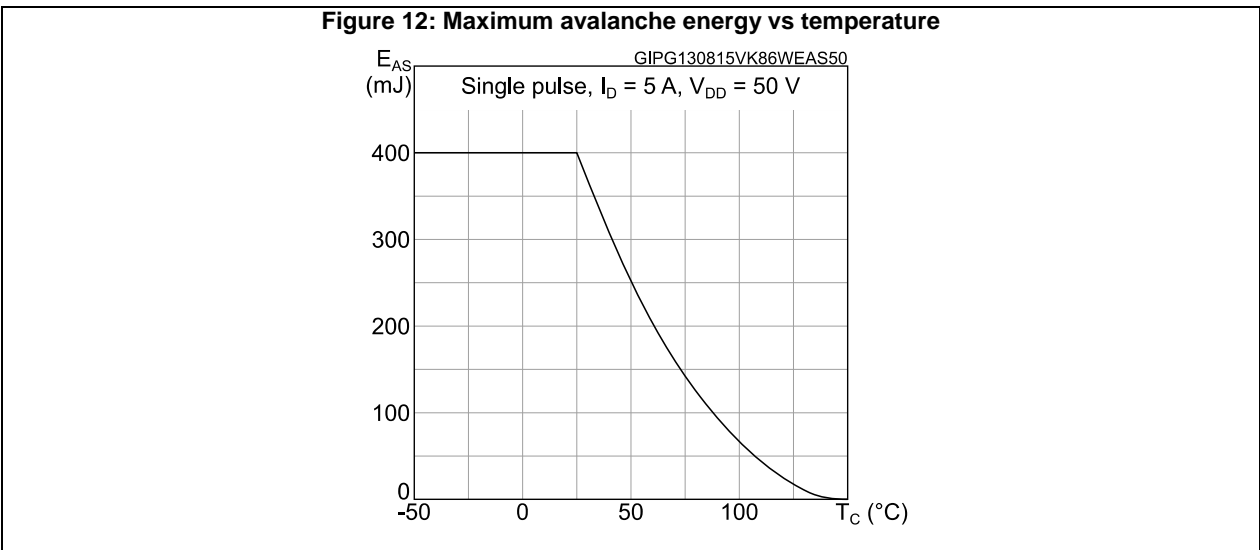
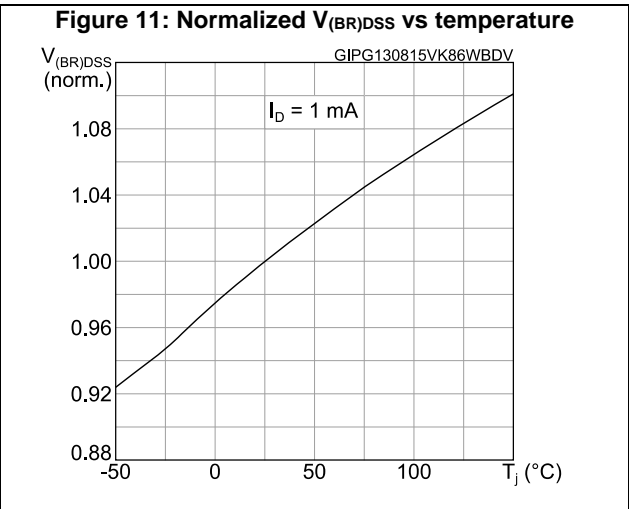
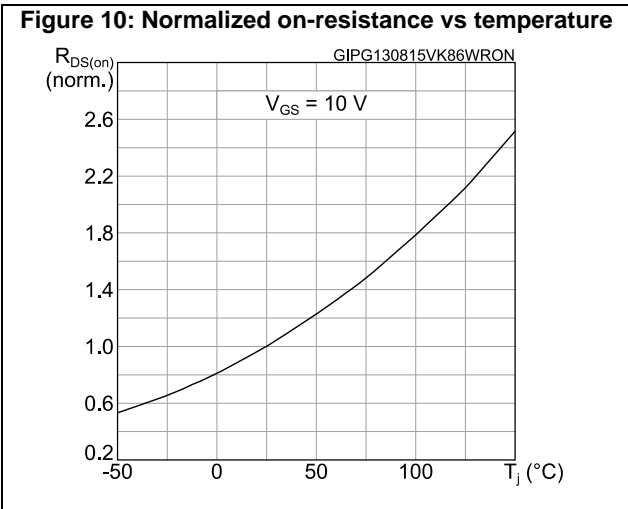
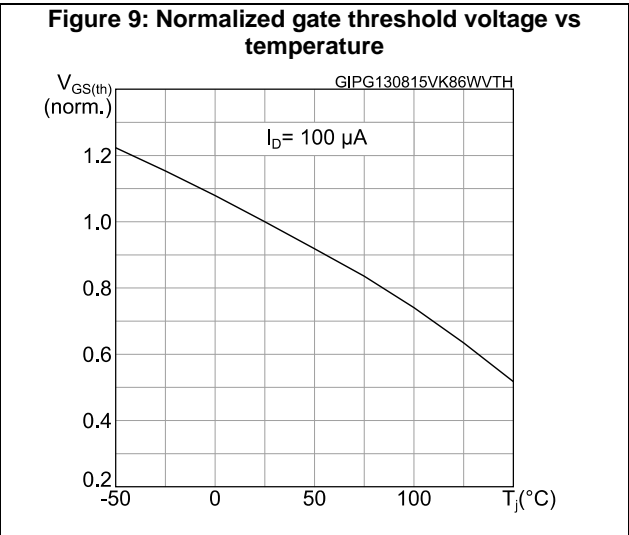
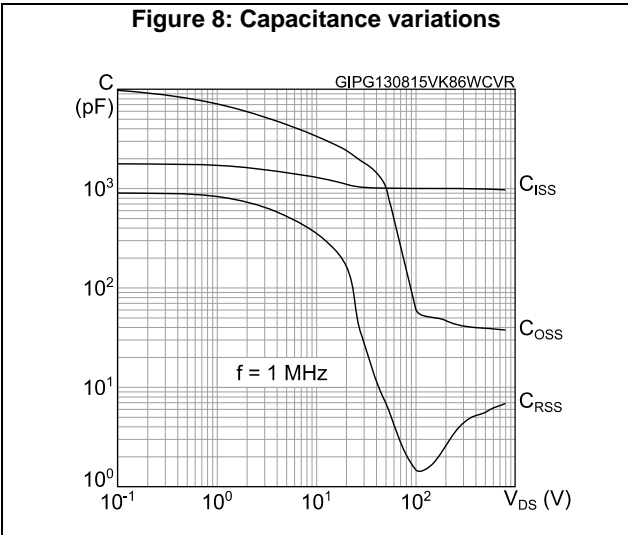
Table 9: Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1\text{ mA}$ , $I_D = 0\text{ A}$	$\pm 30$	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

## 2.1 Electrical characteristics (curves)





### 3 Test circuits

**Figure 13: Test circuit for resistive load switching times**



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**Figure 14: Test circuit for gate charge behavior**



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**Figure 15: Test circuit for inductive load switching and diode recovery times**



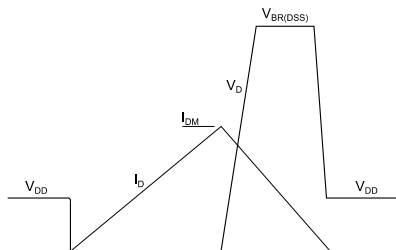
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**Figure 16: Unclamped inductive load test circuit**



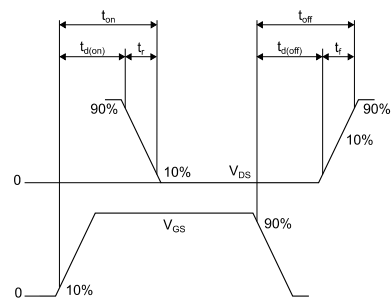
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**Figure 17: Unclamped inductive waveform**



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**Figure 18: Switching time waveform**



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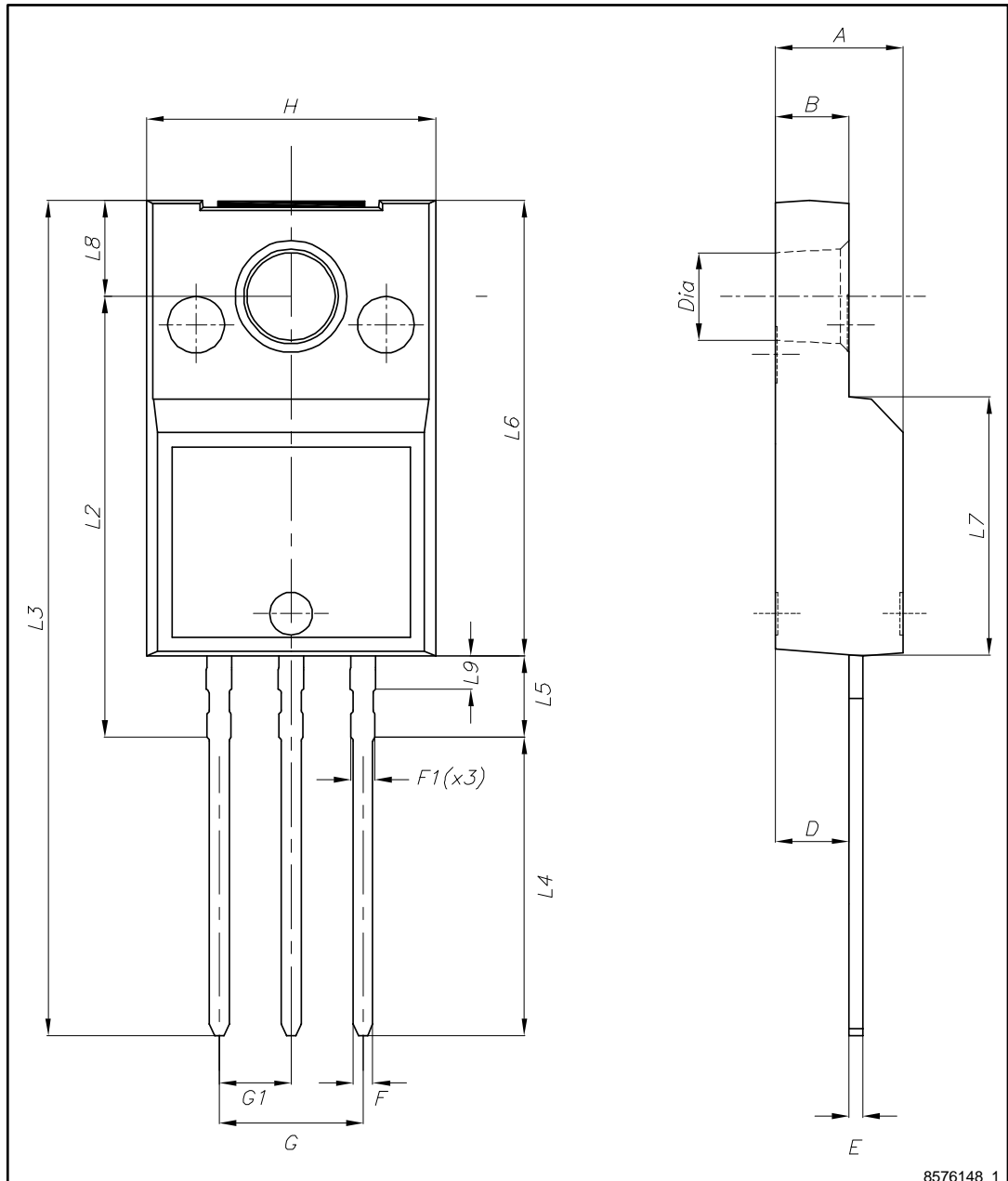


## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 4.1 TO-220FP ultra narrow leads package information

Figure 19: TO-220FP ultra narrow leads package outline



8576148\_1

Table 10: TO-220FP ultra narrow leads mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
E	0.45		0.60
F	0.65		0.75
F1	-		0.90
G	4.95		5.20
G1	2.40	2.54	2.70
H	10.00		10.40
L2	15.10		15.90
L3	28.50		30.50
L4	10.20		11.00
L5	2.50		3.10
L6	15.60		16.40
L7	9.00		9.30
L8	3.20		3.60
L9	-		1.30
Dia.	3.00		3.20

## 5 Revision history

Table 11: Document revision history

Date	Revision	Changes
21-Feb-2017	1	First release

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