

N-channel 600 V, 0.14 Ω typ., 20 A MDmesh™ M2 Power MOSFET in TO-220FP ultra narrow leads package

Datasheet - production data

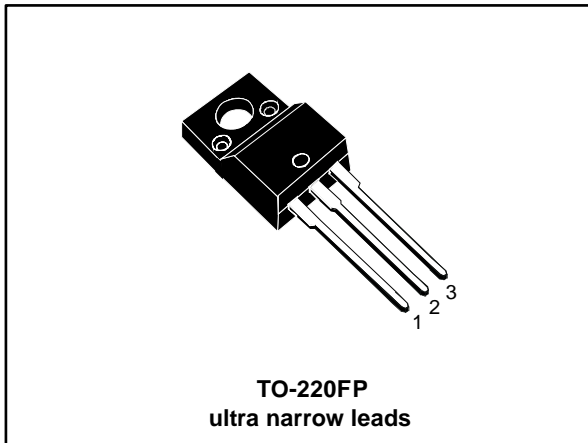
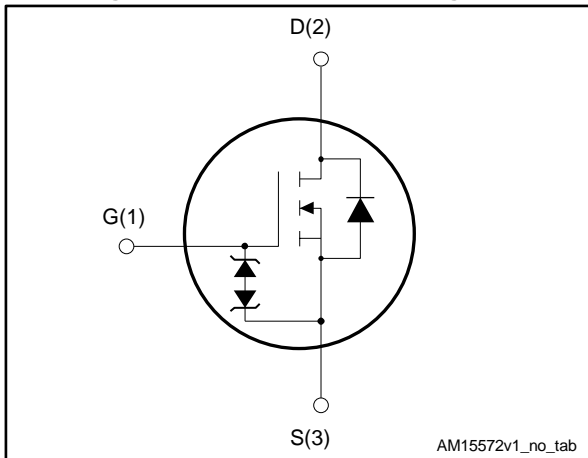


Figure 1: Internal schematic diagram



Features

| Order code | V_{DS} @ T_{Jmax} | $R_{DS(on)}$ max. | I_D | P_{TOT} |
|-------------|-----------------------|-------------------|-------|-----------|
| STFU26N60M2 | 650 V | 0.165 Ω | 20 A | 30 W |

- Extremely low gate charge
- Excellent output capacitance (C_{oss}) profile
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications
- LCC converters, resonant converters

Description

This device is an N-channel Power MOSFET developed using MDmesh™ M2 technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance and optimized switching characteristics, rendering it suitable for the most demanding high efficiency converters.

Table 1: Device summary

| Order code | Marking | Package | Packing |
|-------------|---------|-----------------------------|---------|
| STFU26N60M2 | 26N60M2 | TO-220FP ultra narrow leads | Tube |

Contents

| | | |
|----------|--|-----------|
| 1 | Electrical ratings | 3 |
| 2 | Electrical characteristics | 4 |
| | 2.1 Electrical characteristics (curves)..... | 6 |
| 3 | Test circuits | 8 |
| 4 | Package information | 9 |
| | 4.1 TO-220FP ultra narrow leads package information..... | 9 |
| 5 | Revision history | 11 |

1 Electrical ratings

Table 2: Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|----------------|---|------------|------------------|
| V_{GS} | Gate-source voltage | ± 25 | V |
| $I_D^{(1)}$ | Drain current (continuous) at $T_{case} = 25\text{ }^\circ\text{C}$ | 20 | A |
| | Drain current (continuous) at $T_{case} = 100\text{ }^\circ\text{C}$ | 13 | |
| $I_{DM}^{(2)}$ | Drain current (pulsed) | 80 | A |
| P_{TOT} | Total dissipation at $T_{case} = 25\text{ }^\circ\text{C}$ | 30 | W |
| $dv/dt^{(3)}$ | Peak diode recovery voltage slope | 15 | V/ns |
| $dv/dt^{(4)}$ | MOSFET dv/dt ruggedness | 50 | |
| V_{ISO} | Insulation withstand voltage (RMS) from all three leads to external heat sink ($t = 1\text{ s}$; $T_C = 25\text{ }^\circ\text{C}$) | 2.5 | kV |
| T_{stg} | Storage temperature range | -55 to 150 | $^\circ\text{C}$ |
| T_j | Operating junction temperature range | | |

Notes:

- (1) Limited by maximum junction temperature.
 (2) Pulse width is limited by safe operating area.
 (3) $I_{SD} \leq 20\text{ A}$, $di/dt=400\text{ A}/\mu\text{s}$; $V_{DS(peak)} < V_{(BR)DSS}$, $V_{DD} = 80\% V_{(BR)DSS}$.
 (4) $V_{DS} \leq 480\text{ V}$.

Table 3: Thermal data

| Symbol | Parameter | Value | Unit |
|----------------|-------------------------------------|-------|---------------------------|
| $R_{thj-case}$ | Thermal resistance junction-case | 4.2 | $^\circ\text{C}/\text{W}$ |
| $R_{thj-amb}$ | Thermal resistance junction-ambient | 62.5 | |

Table 4: Avalanche characteristics

| Symbol | Parameter | Value | Unit |
|----------------|---|-------|------|
| $I_{AR}^{(1)}$ | Avalanche current, repetitive or not repetitive | 3.8 | A |
| $E_{AR}^{(2)}$ | Single pulse avalanche energy | 250 | mJ |

Notes:

- (1) Pulse width limited by T_{jmax} .
 (2) starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$.

2 Electrical characteristics

($T_{\text{case}} = 25\text{ °C}$ unless otherwise specified)

Table 5: Static

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------------------------|-----------------------------------|--|------|------|----------|---------------|
| $V_{(\text{BR})\text{DSS}}$ | Drain-source breakdown voltage | $V_{\text{GS}} = 0\text{ V}$, $I_{\text{D}} = 1\text{ mA}$ | 600 | | | V |
| I_{DSS} | Zero gate voltage drain current | $V_{\text{GS}} = 0\text{ V}$, $V_{\text{DS}} = 600\text{ V}$ | | | 1 | μA |
| | | $V_{\text{GS}} = 0\text{ V}$, $V_{\text{DS}} = 600\text{ V}$, $T_{\text{case}} = 125\text{ °C}^{(1)}$ | | | 100 | |
| I_{GSS} | Gate-body leakage current | $V_{\text{DS}} = 0\text{ V}$, $V_{\text{GS}} = \pm 25\text{ V}$ | | | ± 10 | μA |
| $V_{\text{GS(th)}}$ | Gate threshold voltage | $V_{\text{DS}} = V_{\text{GS}}$, $I_{\text{D}} = 250\text{ }\mu\text{A}$ | 2 | 3 | 4 | V |
| $R_{\text{DS(on)}}$ | Static drain-source on-resistance | $V_{\text{GS}} = 10\text{ V}$, $I_{\text{D}} = 10\text{ A}$ | | 0.14 | 0.165 | Ω |

Notes:

⁽¹⁾Defined by design, not subject to production test.

Table 6: Dynamic

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|----------------------------|-------------------------------|--|------|------|------|-------------|
| C_{iss} | Input capacitance | $V_{\text{DS}} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{\text{GS}} = 0\text{ V}$ | - | 1360 | - | pF |
| C_{oss} | Output capacitance | | - | 88 | - | |
| C_{riss} | Reverse transfer capacitance | | - | 2 | - | |
| $C_{\text{oss eq.}}^{(1)}$ | Equivalent output capacitance | $V_{\text{DS}} = 0\text{ to }480\text{ V}$, $V_{\text{GS}} = 0\text{ V}$ | - | 124 | - | pF |
| R_{G} | Intrinsic gate resistance | $f = 1\text{ MHz}$, $I_{\text{D}} = 0\text{ A}$ | - | 4 | - | Ω |
| Q_{g} | Total gate charge | $V_{\text{DD}} = 480\text{ V}$, $I_{\text{D}} = 20\text{ A}$, $V_{\text{GS}} = 0\text{ to }10\text{ V}$ (see Figure 15: "Test circuit for gate charge behavior") | - | 34 | - | nC |
| Q_{gs} | Gate-source charge | | - | 5.6 | - | |
| Q_{gd} | Gate-drain charge | | - | 16.3 | - | |

Notes:

⁽¹⁾ $C_{\text{oss eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 7: Switching times

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------------|---------------------|---|------|------|------|-------------|
| $t_{\text{d(on)}}$ | Turn-on delay time | $V_{\text{DD}} = 300\text{ V}$, $I_{\text{D}} = 10\text{ A}$ $R_{\text{G}} = 4.7\text{ }\Omega$, $V_{\text{GS}} = 10\text{ V}$ (see Figure 14: "Test circuit for resistive load switching times") | - | 20.2 | - | ns |
| t_{r} | Rise time | | - | 8 | - | |
| $t_{\text{d(off)}}$ | Turn-off delay time | | - | 66 | - | |
| t_{f} | Fall time | | - | 10 | - | |

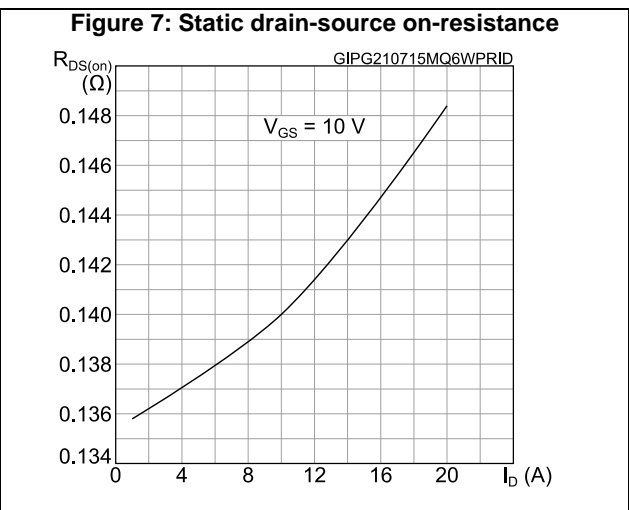
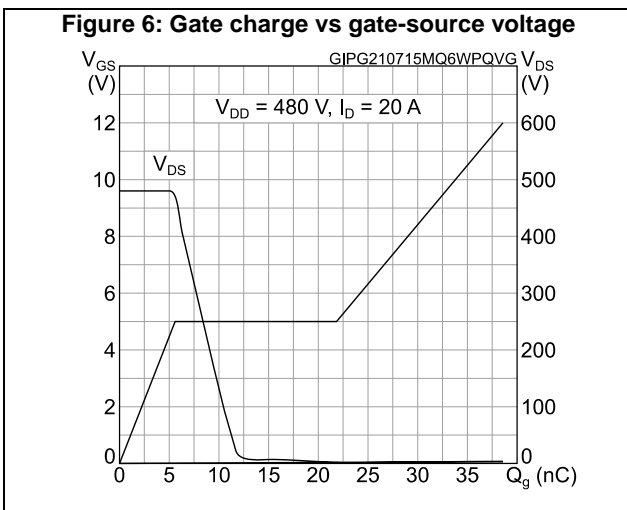
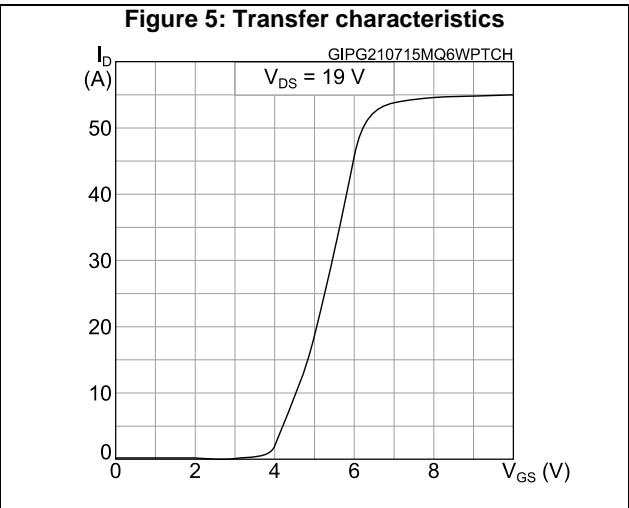
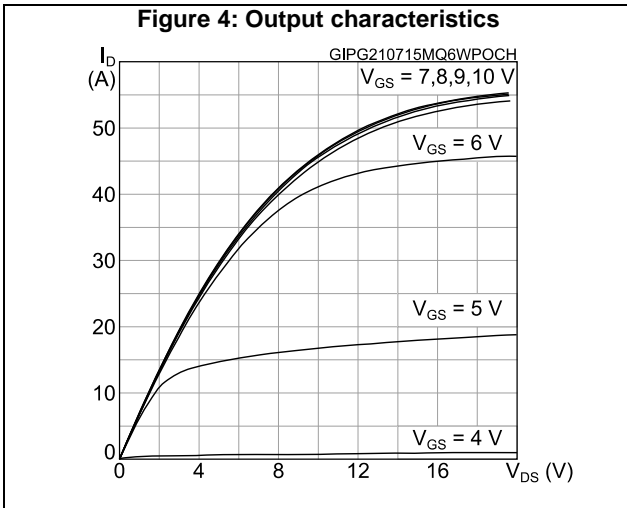
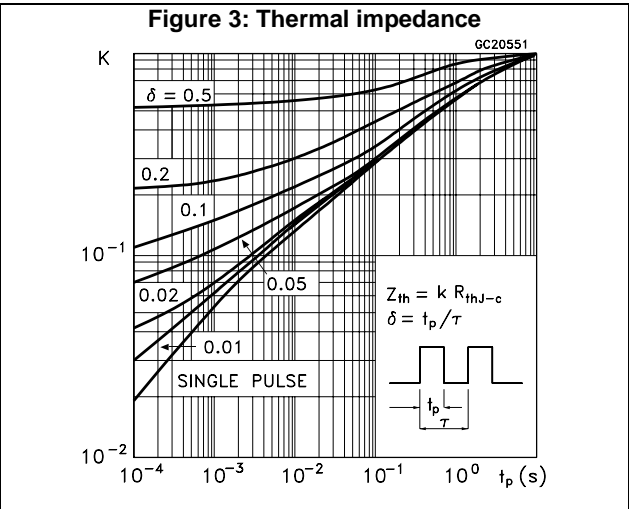
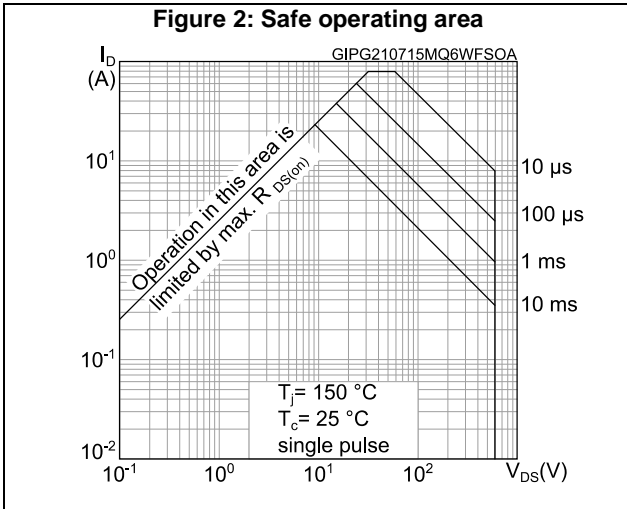
Table 8: Source-drain diode

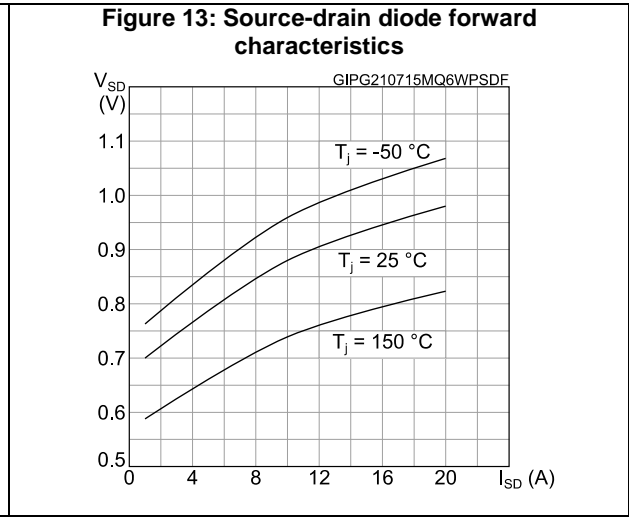
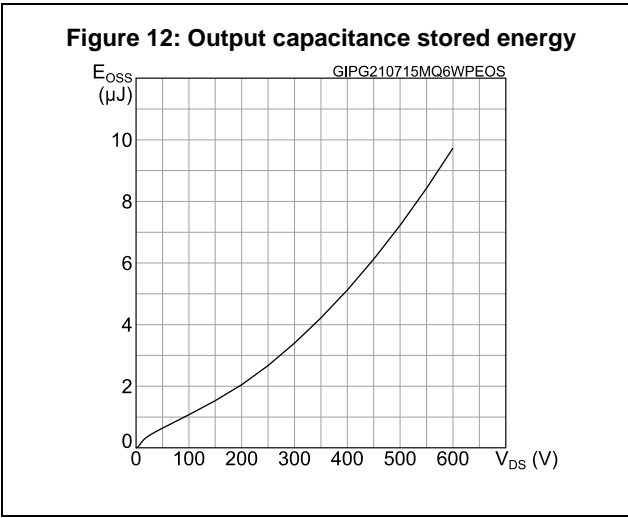
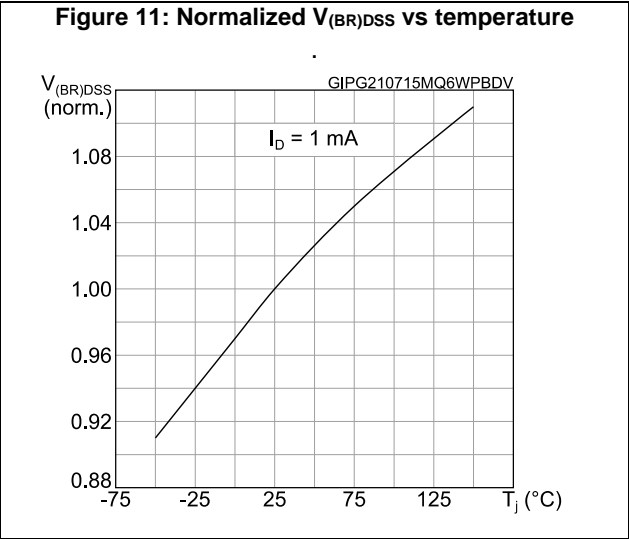
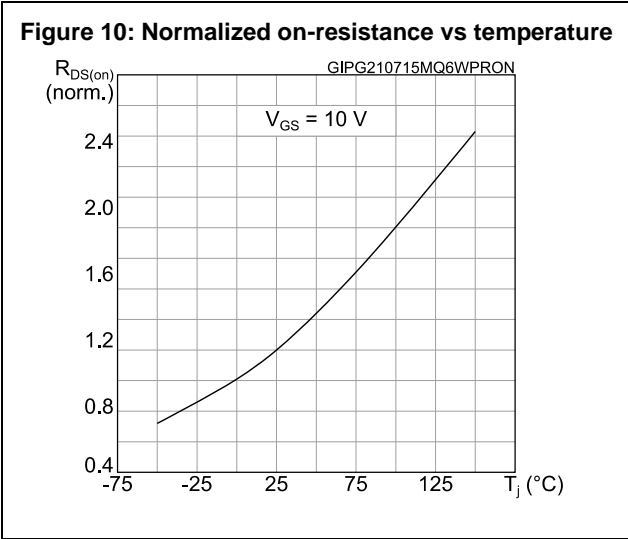
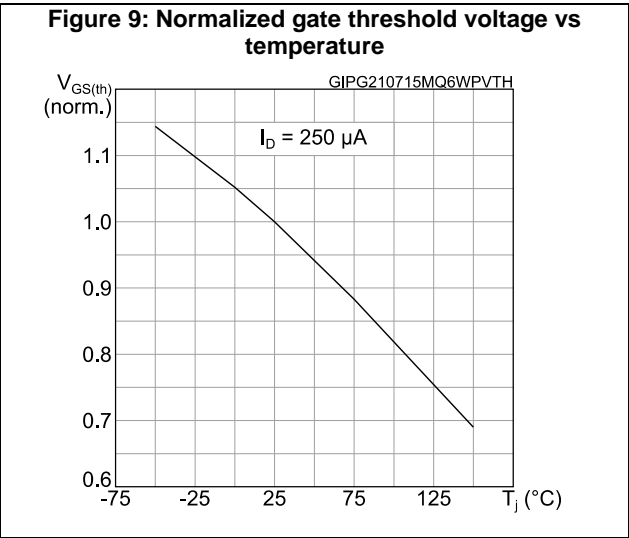
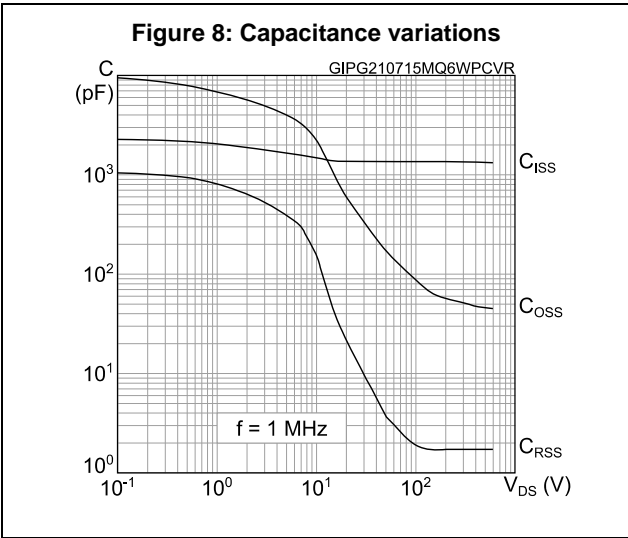
| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------------|-------------------------------|--|------|------|------|---------------|
| I_{SD} | Source-drain current | | - | | 20 | A |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) | | - | | 80 | A |
| $V_{SD}^{(2)}$ | Forward on voltage | $V_{GS} = 0 \text{ V}$, $I_{SD} = 20 \text{ A}$ | - | | 1.6 | V |
| t_{rr} | Reverse recovery time | $I_{SD} = 20 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$, $V_{DD} = 60 \text{ V}$ (see Figure 16: "Test circuit for inductive load switching and diode recovery times") | - | 360 | | ns |
| Q_{rr} | Reverse recovery charge | | - | 5 | | μC |
| I_{RRM} | Reverse recovery current | | - | 27 | | A |
| t_{rr} | Reverse recovery time | $I_{SD} = 20 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$, $V_{DD} = 60 \text{ V}$, $T_j = 150 \text{ }^\circ\text{C}$ (see Figure 16: "Test circuit for inductive load switching and diode recovery times") | - | 556 | | ns |
| Q_{rr} | Reverse recovery charge | | - | 8 | | μC |
| I_{RRM} | Reverse recovery current | | - | 29 | | A |

Notes:

- (1) Pulse width is limited by safe operating area.
(2) Pulse test: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)





3 Test circuits

Figure 14: Test circuit for resistive load switching times



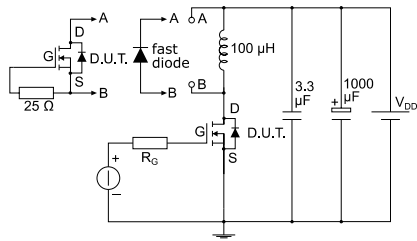
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Figure 15: Test circuit for gate charge behavior



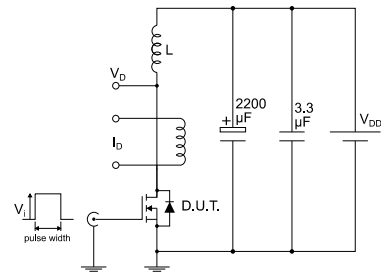
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Figure 16: Test circuit for inductive load switching and diode recovery times



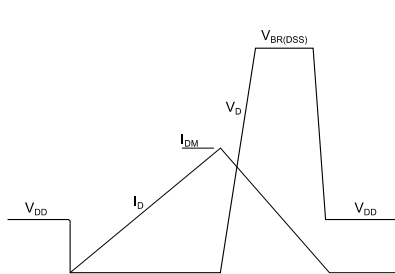
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Figure 17: Unclamped inductive load test circuit



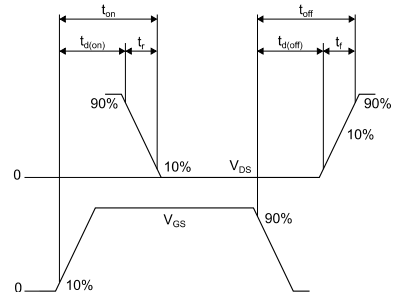
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Figure 18: Unclamped inductive waveform



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Figure 19: Switching time waveform



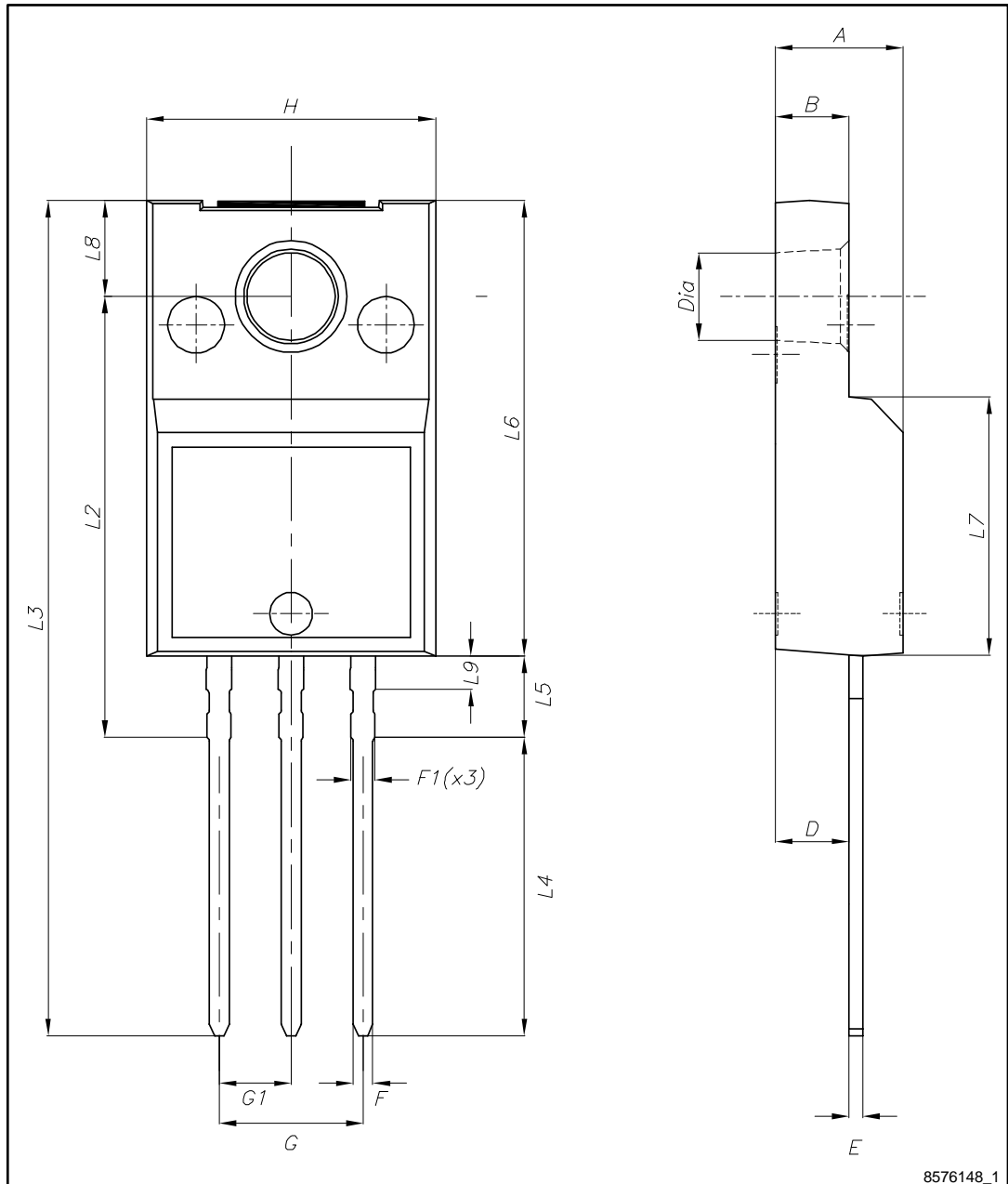
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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 TO-220FP ultra narrow leads package information

Figure 20: TO-220FP ultra narrow leads package outline



8576148_1

Table 9: TO-220FP ultra narrow leads mechanical data

| Dim. | mm | | |
|------|-------|------|-------|
| | Min. | Typ. | Max. |
| A | 4.40 | | 4.60 |
| B | 2.50 | | 2.70 |
| D | 2.50 | | 2.75 |
| E | 0.45 | | 0.60 |
| F | 0.65 | | 0.75 |
| F1 | - | | 0.90 |
| G | 4.95 | | 5.20 |
| G1 | 2.40 | 2.54 | 2.70 |
| H | 10.00 | | 10.40 |
| L2 | 15.10 | | 15.90 |
| L3 | 28.50 | | 30.50 |
| L4 | 10.20 | | 11.00 |
| L5 | 2.50 | | 3.10 |
| L6 | 15.60 | | 16.40 |
| L7 | 9.00 | | 9.30 |
| L8 | 3.20 | | 3.60 |
| L9 | - | | 1.30 |
| Dia. | 3.00 | | 3.20 |

5 Revision history

Table 10: Document revision history

| Date | Revision | Changes |
|-------------|----------|----------------|
| 27-Jul-2017 | 1 | First release. |

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