STF38N65M5, STFW38N65M5

N-channel 650 V, 0.073 Ω typ., 30 A MDmesh™ V Power MOSFETs in TO-220FP and TO-3PF packages

Datasheet - production data

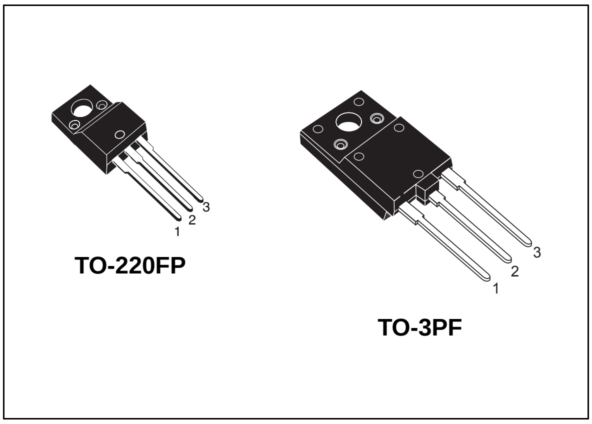
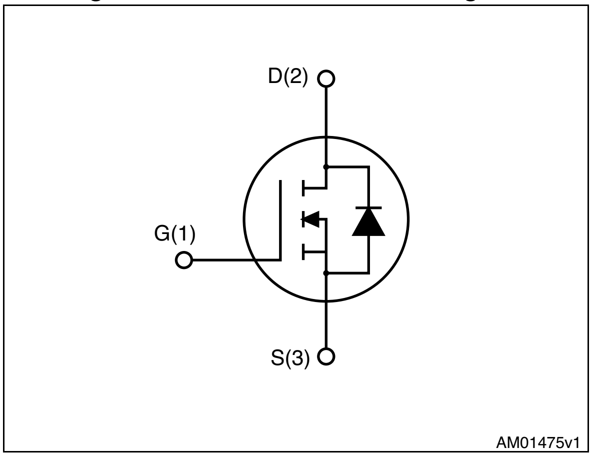


Figure 1. Internal schematic diagram



Features

Order codes	V_{DS}@ T_{Jmax}	$R_{DS(on)}$ max	I_D
STF38N65M5	710 V	0.095 Ω	30 A
STFW38N65M5			

- Higher V_{DSS} rating and high dv/dt capability
- Excellent switching performance
- 100% avalanche tested

Applications

- Switching applications

Description

These devices are N-channel MDmesh™ V Power MOSFETs based on an innovative proprietary vertical process technology, which is combined with STMicroelectronics’ well-known PowerMESH™ horizontal layout structure. The resulting product has extremely low on-resistance, which is unmatched among silicon-based Power MOSFETs, making it especially suitable for applications which require superior power density and outstanding efficiency.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STF38N65M5	38N65M5	TO-220FP	Tube
STFW38N65M5		TO-3PF	

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220FP	TO-3PF	
V_{GS}	Gate-source voltage	± 25		V
I_D (1)	Drain current (continuous) at T_C = 25 °C	30		A
I_D (1)	Drain current (continuous) at T_C = 100 °C	19		A
I_{DM} (1), (2)	Drain current (pulsed)	120		A
P_{TOT}	Total dissipation at T_C = 25 °C	35	57	W
dv/dt (3)	Peak diode recovery voltage slope	15		V/ns
dv/dt (4)	MOSFET dv/dt ruggedness	50		V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; T_C = 25 °C)	2500	3500	V
T_{stg}	Storage temperature	-55 to 150		°C
T_j	Max. operating junction temperature	150		°C

1. Limited by maximum junction temperature
2. Pulse width limited by safe operating area.
3. $I_{SD} \leq$ 30 A, di/dt $\leq$ 400 A/μs; $V_{Peak} < V_{(BR)DSS}$, V_{DD} = 400 V
4. $V_{DS} \leq$ 520 V

Table 3. Thermal data

Symbol	Parameter	Value		Unit
		TO-220FP	TO-3PF	
$R_{thj\text{-}case}$	Thermal resistance junction-case max	3.6	2.2	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient max	62.5	50	°C/W

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	8	A
E_{AS}	Single pulse avalanche energy (starting t_j = 25°C, I_d= I_{AR}; V_{dd}= 50V)	660	mJ

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 5. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	650			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 650 V			1	µA
		V_{DS} = 650 V, T_C=125 °C			100	µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 25 V			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 15 A		0.073	0.095	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0	-	3000	-	pF
C_{oss}	Output capacitance		-	74	-	pF
C_{rss}	Reverse transfer capacitance		-	5.8	-	pF
$C_{o(tr)}$ (1)	Equivalent capacitance time related	V_{DS} = 0 to 520 V, V_{GS} = 0	-	244	-	pF
$C_{o(er)}$ (2)	Equivalent capacitance energy related		-	70	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	2.4	-	Ω
Q_g	Total gate charge	V_{DD} = 520 V, I_D = 15 A, V_{GS} = 10 V (see *Figure 18*)	-	71	-	nC
Q_{gs}	Gate-source charge		-	18	-	nC
Q_{gd}	Gate-drain charge		-	30	-	nC

1. Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}
2. Energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d\ (v)}$	Voltage delay time	V_{DD} = 400 V, I_D = 20 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 19* and *Figure 22*)	-	66	-	ns
$t_{r\ (v)}$	Voltage rise time		-	9	-	ns
$t_{f\ (i)}$	Current fall time		-	9	-	ns
$t_{c(off)}$	Crossing time		-	13	-	ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		30	A
I_{SDM} (1)	Source-drain current (pulsed)		-		120	A
V_{SD} (2)	Forward on voltage	I_{SD} = 30 A, V_{GS} = 0	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 30 A, di/dt = 100 A/µs V_{DD} = 100 V (see *Figure 22*)	-	382		ns
Q_{rr}	Reverse recovery charge		-	6.6		µC
I_{RRM}	Reverse recovery current		-	35		A
t_{rr}	Reverse recovery time	I_{SD} = 30 A, di/dt = 100 A/µs V_{DD} = 100 V, T_j = 150 °C (see *Figure 22*)	-	522		ns
Q_{rr}	Reverse recovery charge		-	10.3		µC
I_{RRM}	Reverse recovery current		-	40		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220FP

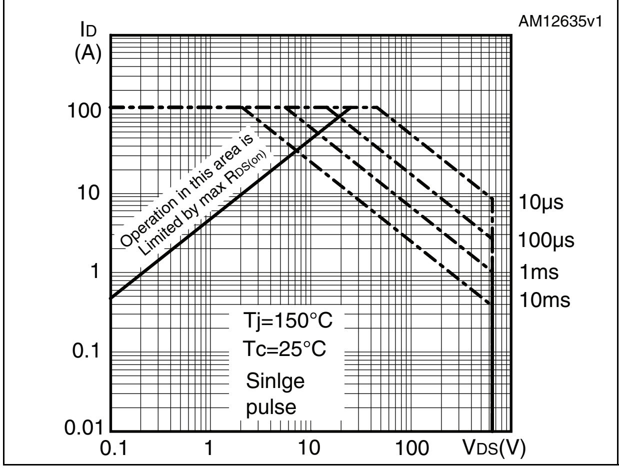


Figure 3. Thermal impedance for TO-220FP

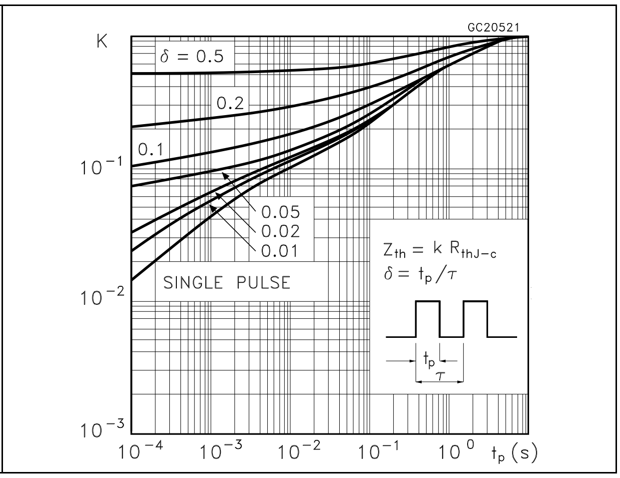


Figure 4. Safe operating area for TO-3PF

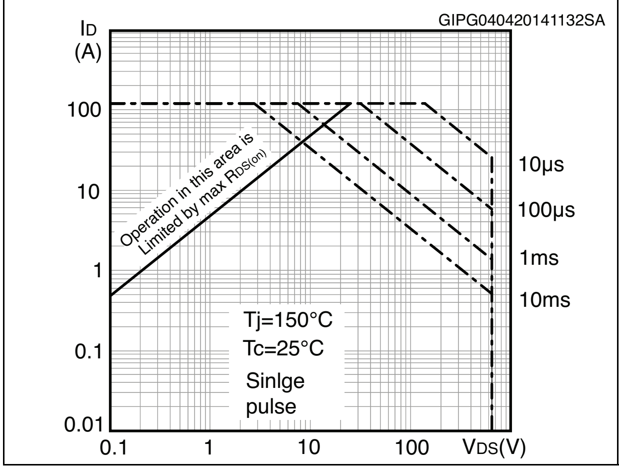


Figure 5. Thermal impedance for TO-3PF

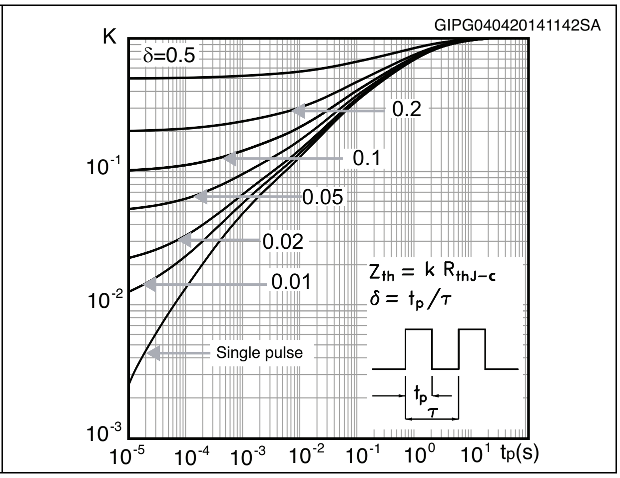


Figure 6. Output characteristics

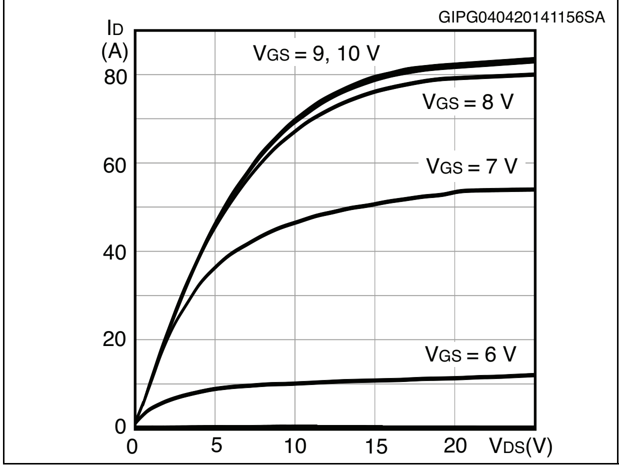


Figure 7. Transfer characteristics

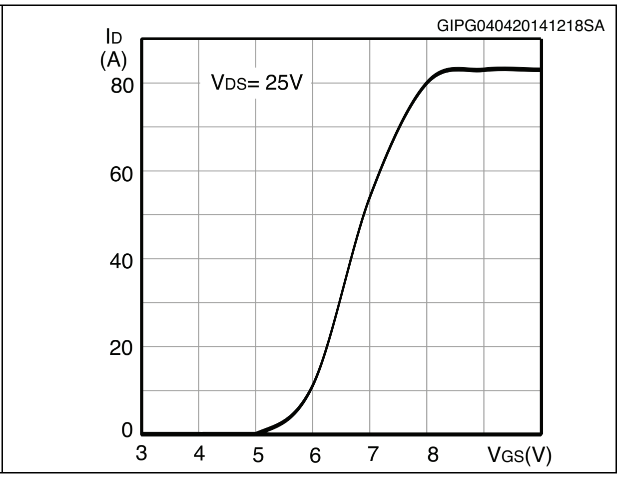


Figure 8. Gate charge vs gate-source voltage

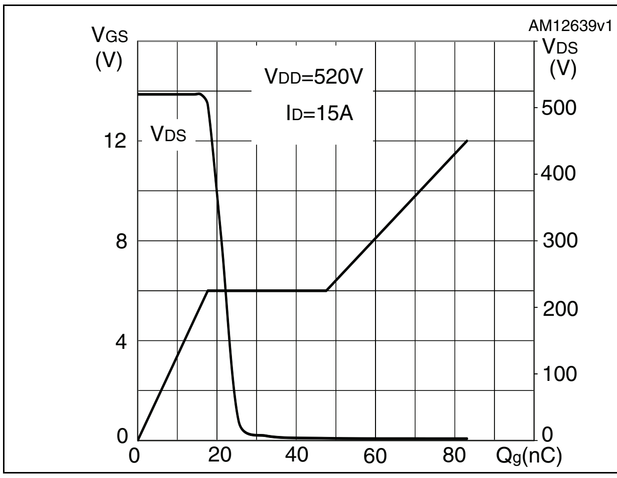


Figure 9. Static drain-source on-resistance

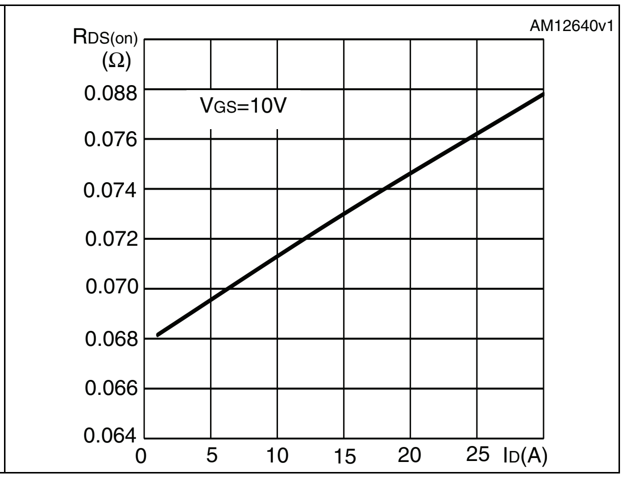


Figure 10. Capacitance variations

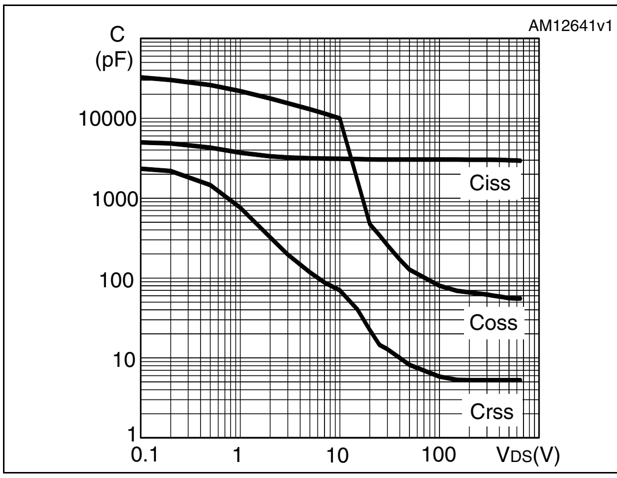


Figure 11. Output capacitance stored energy

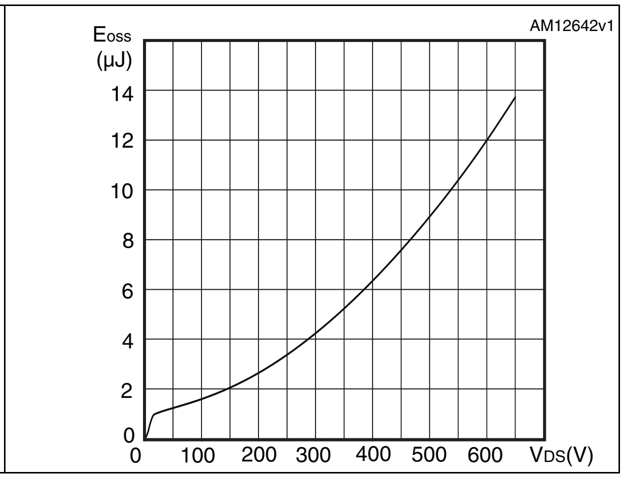


Figure 12. Normalized gate threshold voltage vs temperature

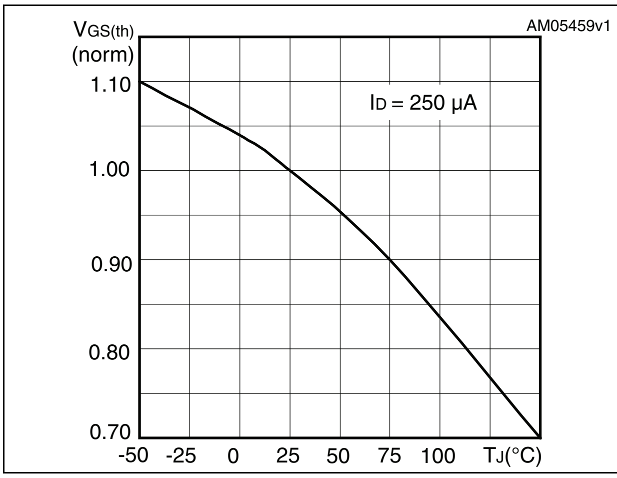


Figure 13. Normalized on-resistance vs temperature

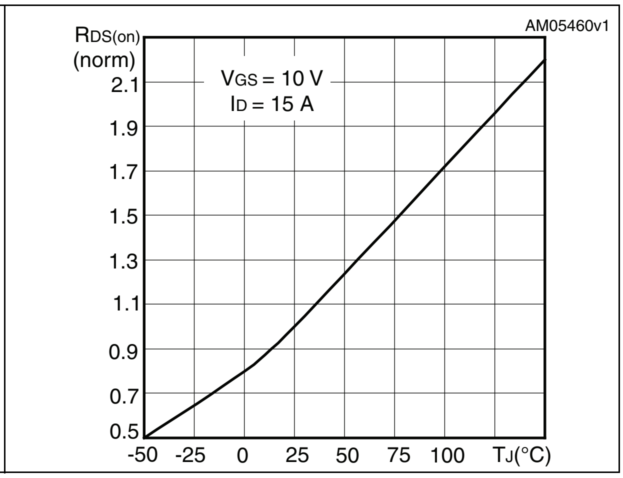


Figure 14. Source-drain diode forward characteristics

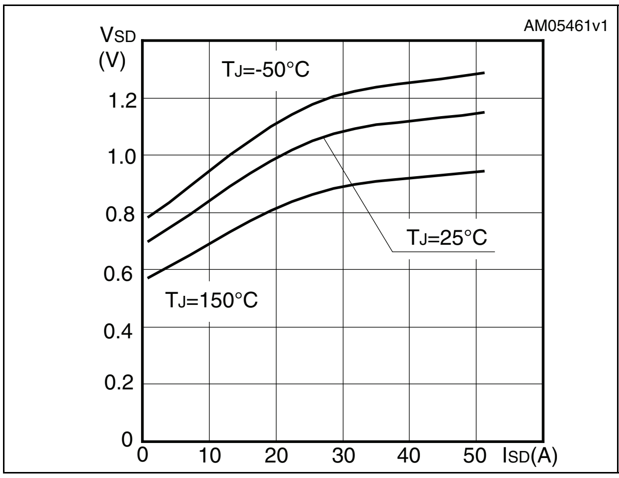


Figure 15. Normalized $V_{(BR)DSS}$ vs temperature

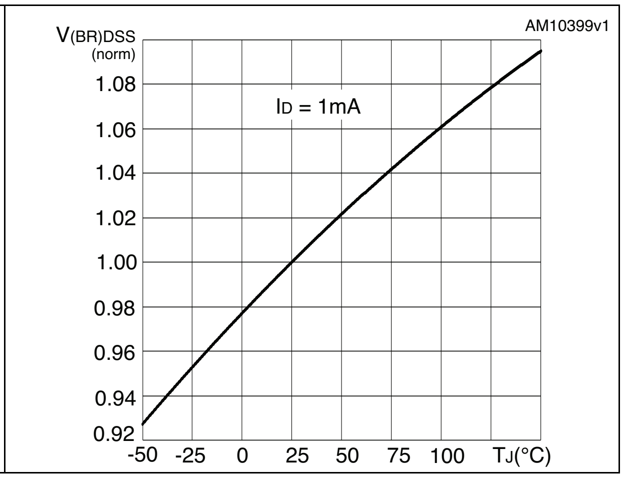
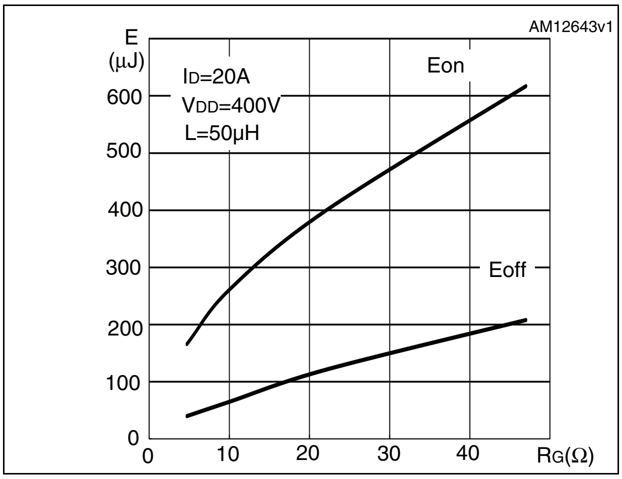


Figure 16. Switching losses vs gate resistance [(1)]



1. Eon including reverse recovery of a SiC diode.

3 Test circuits

Figure 17. Switching times test circuit for resistive load

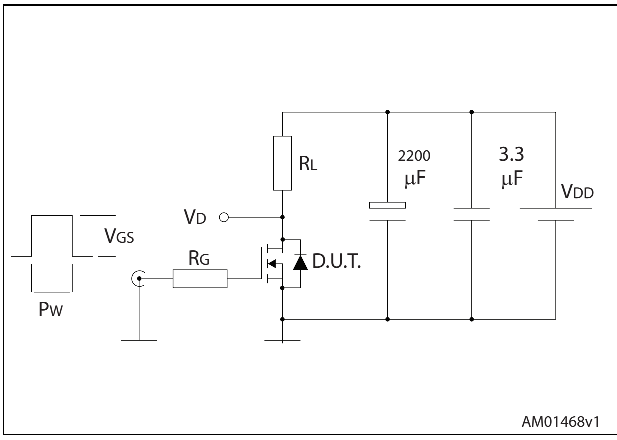


Figure 18. Gate charge test circuit

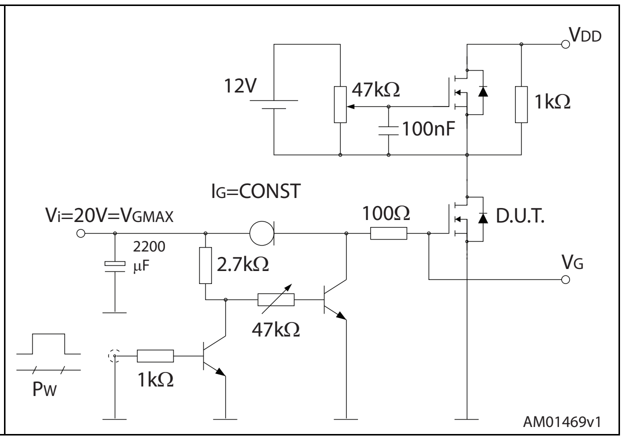


Figure 19. Test circuit for inductive load switching and diode recovery times

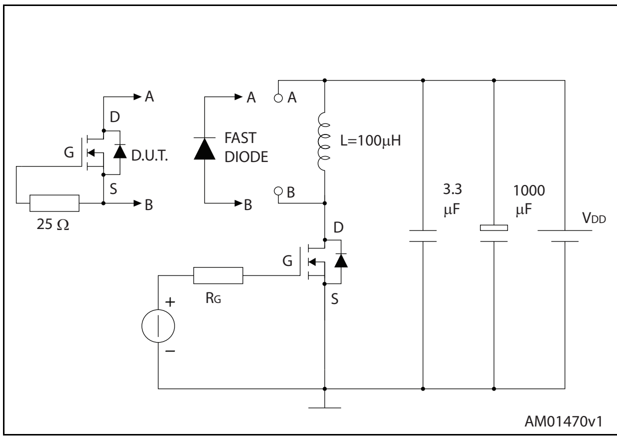


Figure 20. Unclamped inductive load test circuit

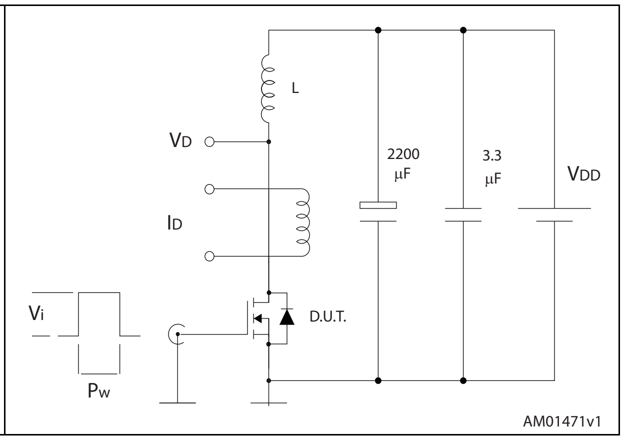


Figure 21. Unclamped inductive waveform

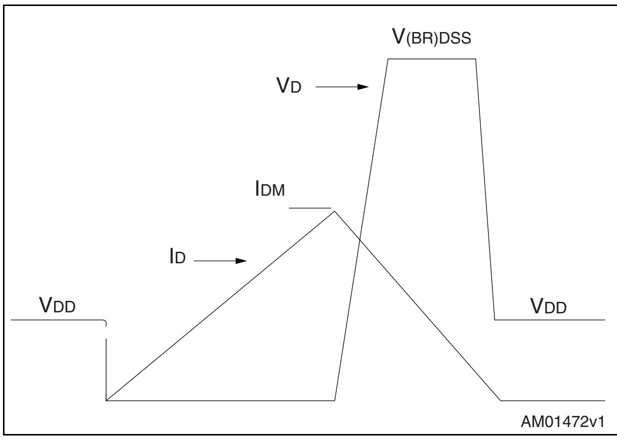
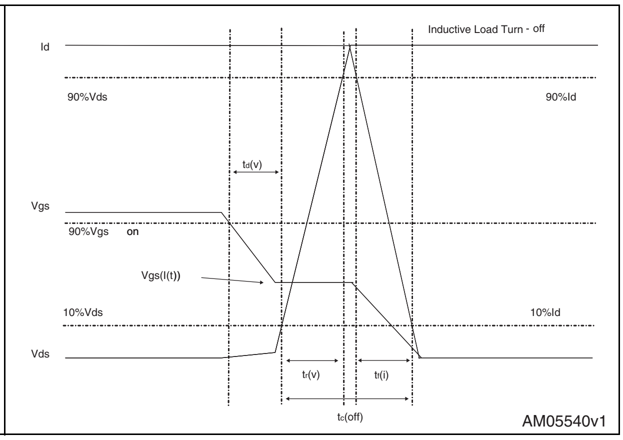


Figure 22. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

4.1 TO-220FP, STF38N65M5

Figure 23. TO-220FP drawing

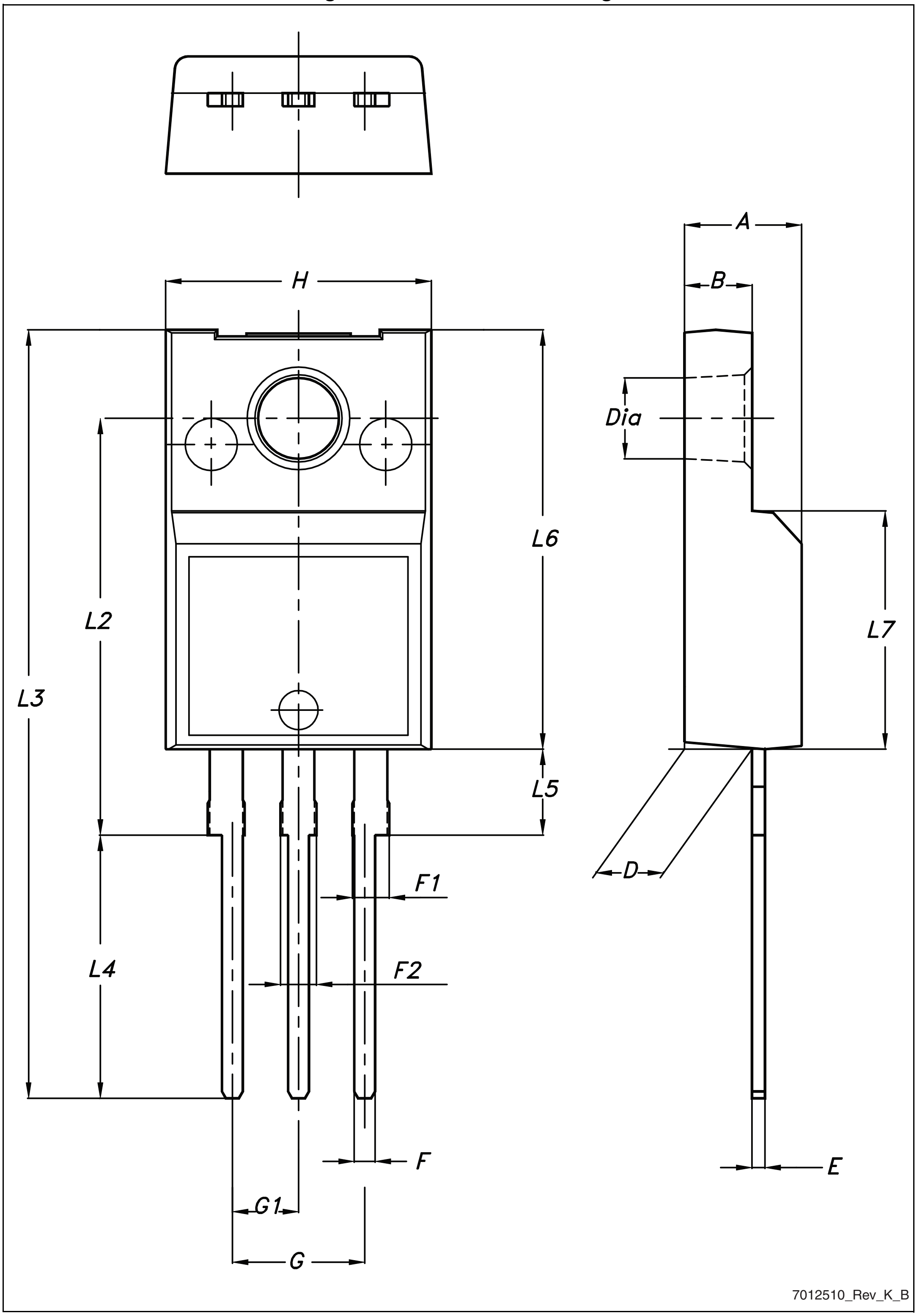


Table 9. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

4.2 TO-3PF, STFW38N65M5

Figure 24. TO-3PF drawing

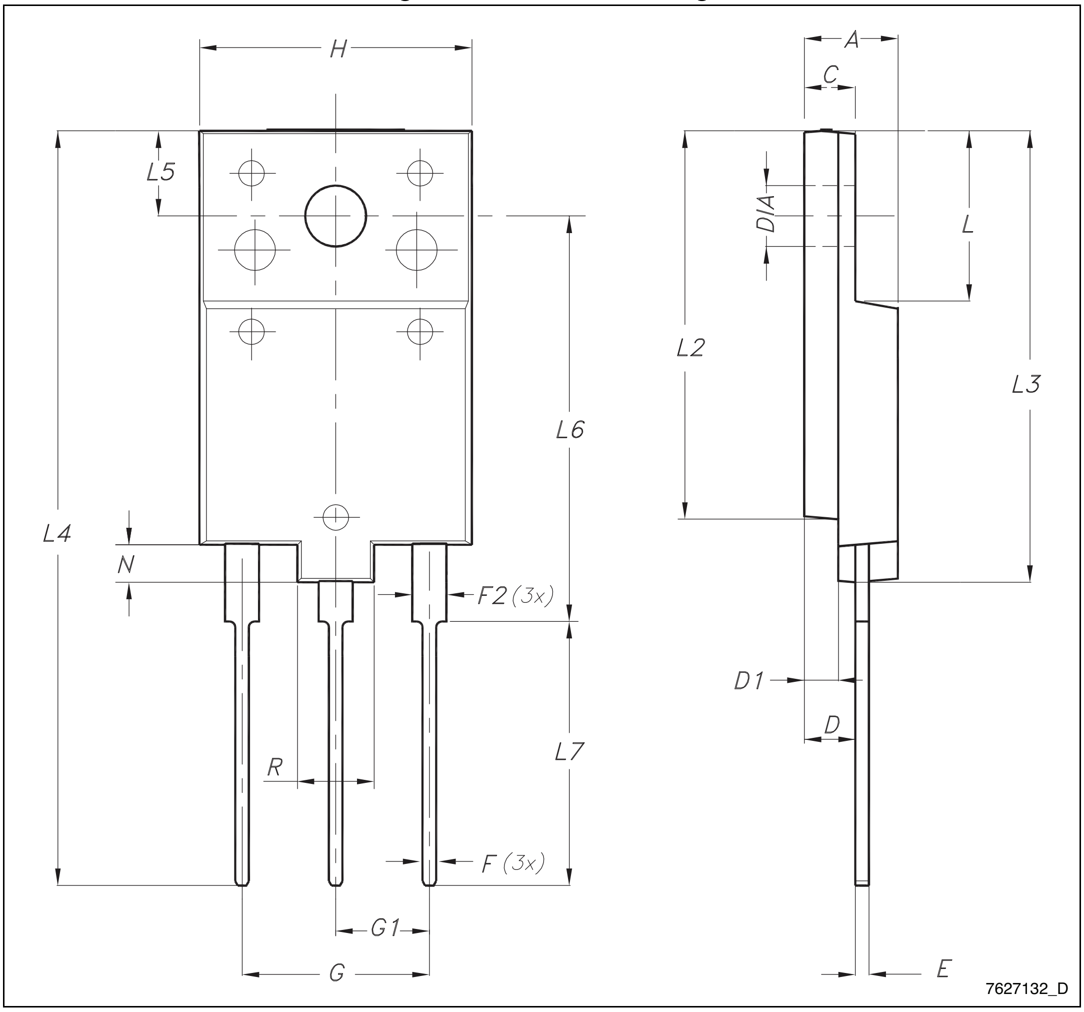


Table 10. TO-3PF mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	5.30		5.70
C	2.80		3.20
D	3.10		3.50
D1	1.80		2.20
E	0.80		1.10
F	0.65		0.95
F2	1.80		2.20
G	10.30		11.50
G1		5.45	
H	15.30		15.70
L	9.80	10	10.20
L2	22.80		23.20
L3	26.30		26.70
L4	43.20		44.40
L5	4.30		4.70
L6	24.30		24.70
L7	14.60		15
N	1.80		2.20
R	3.80		4.20
Dia	3.40		3.80

5 Revision history

Table 11. Document revision history

Date	Revision	Changes
14-Apr-2014	1	First release. Part numbers previously included in datasheet DocID022851