

Demonstration board user guidelines for the low voltage high bandwidth STG3220 dual SPDT switch

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Introduction

This application note concerns the STG3220 demonstration board, designed to show the performance of the low-voltage high bandwidth STG3220 dual SPDT switch.

This document contains:

- a brief description of the STG3220 device
- a description of the demonstration board and all of its components
- the layout of the demonstration board

About the STG3220 device

The STG3220 device is a high-speed CMOS low-voltage dual analog SPDT (single pole dual throw) switch or 2:1 multiplexer/de-multiplexer switch fabricated in silicon gate C²MOS technology. It is designed to operate from 1.65 to 4.3 V, making it ideal for portable applications.

Key features of the STG3220 include


- Ultra low power dissipation: $I_{CC} = 1 \mu\text{A}$ (max.) at $T_A = 85 \text{ }^\circ\text{C}$
- Low on-resistance:
 - $R_{ON} = 4.8 \Omega$ ($T_A = 25 \text{ }^\circ\text{C}$) at $V_{CC} = 4.3 \text{ V}$
 - $R_{ON} = 5.9 \Omega$ ($T_A = 25 \text{ }^\circ\text{C}$) at $V_{CC} = 3.0 \text{ V}$
- Wide operating voltage range: V_{CC} (oper.) = 1.65 V to 4.3 V
- 4.3 V tolerant and 1.8 V compatible threshold on digital control input at $V_{CC} = 2.3$ to 3.0 V
- Typical bandwidth (-3 dB) at 800 MHz on all channels
- USB (2.0) high speed (480 Mbps) signal switching compliance
- Integrated fail safe function
- Interrupt function to indicate to the processor that the device is in dedicated port charging mode
- Latch-up performance exceeds 500 mA per JESD78, Clas3s II
- ESD performance exceeds JESD22:
 - Dn pins: 4000 V human body model (A114-A)
 - All other pins: 2000 V human body model (A114-A)

For further information on the STG3220 device, refer to the datasheet.

1 Description

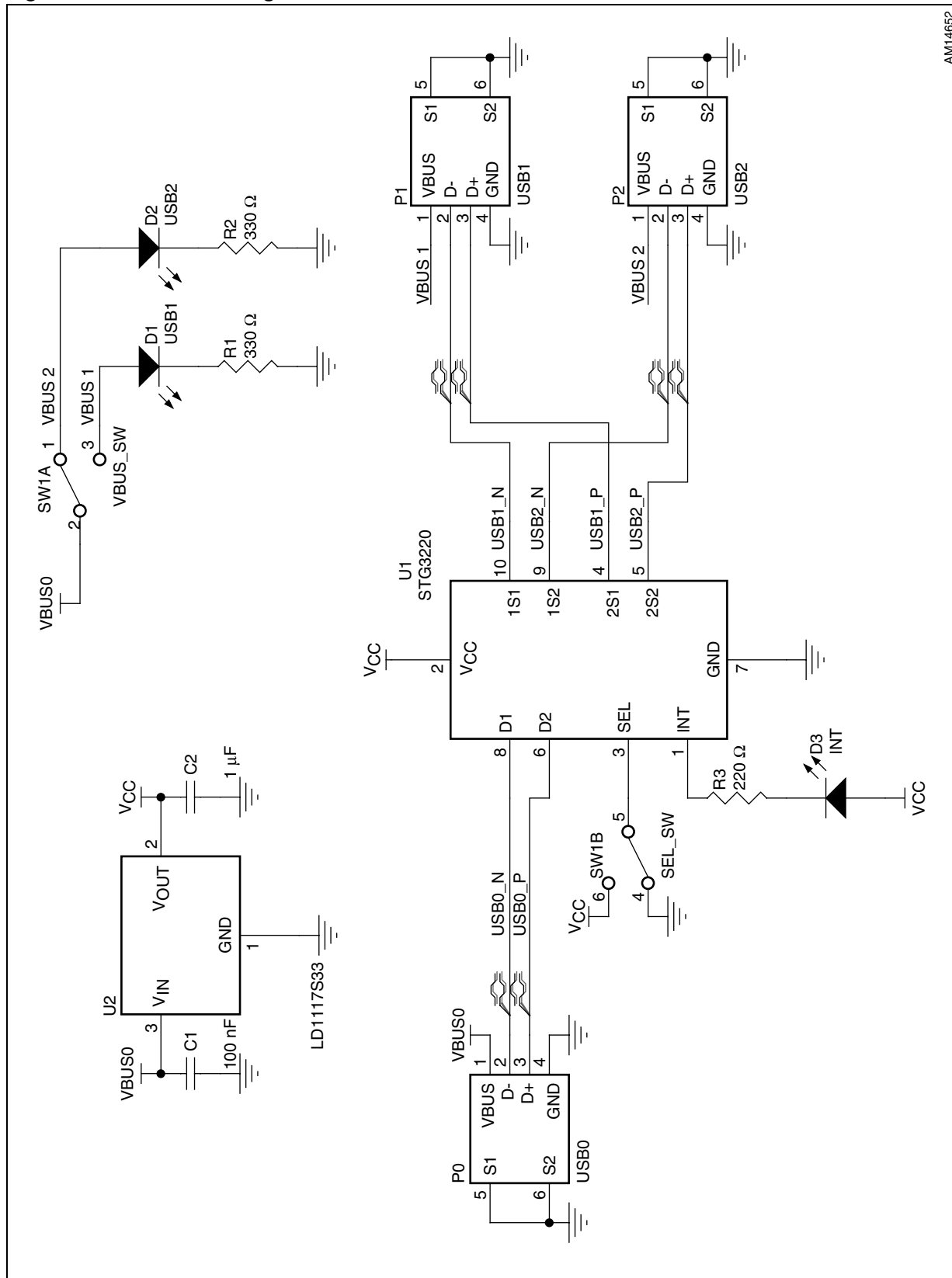
The STG3220 demonstration board is designed for the low-voltage high bandwidth STG3220 dual SPDT switch. The STG3220 device, in a tiny QFN package, is mounted on a 4-layer PCB with impedance matched signal tracks. An easily accessible USB connector on the board allows the board to be used as the USB switch and can be connected to another USB port (PC host, USB hub, etc.). On the other side of the board there are two USB receptacles and thanks to the STG3220 device, one of the USB receptacles is active and connected to the USB port. The active (ON path) is chosen by the manual switch and it is indicated by the luminous LED diode.

Table 1. Main components and connectors

Designator	Description
SW1	USB path selector switch: USB2 position: P0 - P2 USB path selected, D1 green LED diode is luminous USB1 position: P0 - P1 USB path selected, D2 green LED diode is luminous <div style="text-align: center;">  </div>
P0	USB connector. Can be connected to USB port (PC, USB hub, etc.)
P1, P2	USB receptacle. USB port for USB device
D3	The yellow LED diode is luminous if the host is in dedicated port charging mode. The STG3220 device has a built-in dedicated port charging detection circuit to detect the condition when the USB D+/D- lines are both in high state.

The demonstration board is powered through a USB connector P0, so that it is fully functional if the P0 is properly connected to the USB port. For the STG3220 device, the USB VBUS line voltage is decreased to 3.3 V and stabilized by the adjustable and fixed low drop positive voltage regulator LD1117S33 (component U2).

Figure 1. Schematic diagram



AM14652

Table 2. Component list

Designator	Quantity	Description
P0	1	USB connector
P1, P2	2	USB receptacle
SW1	1	Dual SPDT switch
U1	1	STG3220
U2	1	LD1117S33
C1	1	100 nF/50 V, ceramic capacitor, 0603
C2	1	1 μ F/50 V, ceramic capacitor, 0603
D1, D2	2	Green LED, 0805
D3	1	Yellow LED, 0805
R1, R2	2	330 Ω , resistor, 0603
R3	1	220 Ω , resistor, 0603

2 Layout

Figure 2 to Figure 6 show the layers and the top view of the demonstration board.

Figure 2. PCB top layer

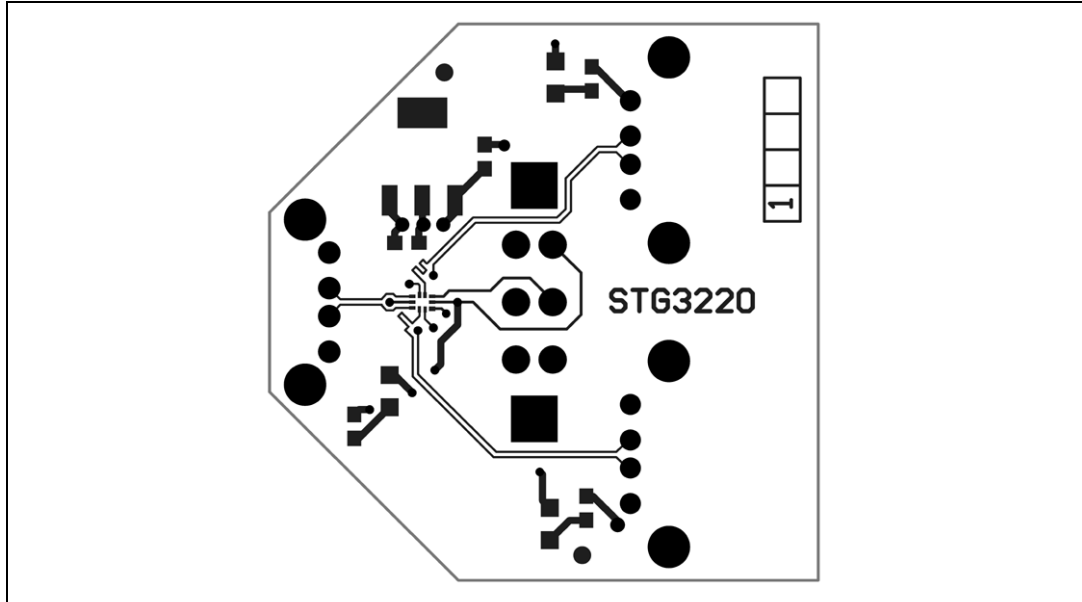


Figure 3. PCB mid1 layer (close to the top)

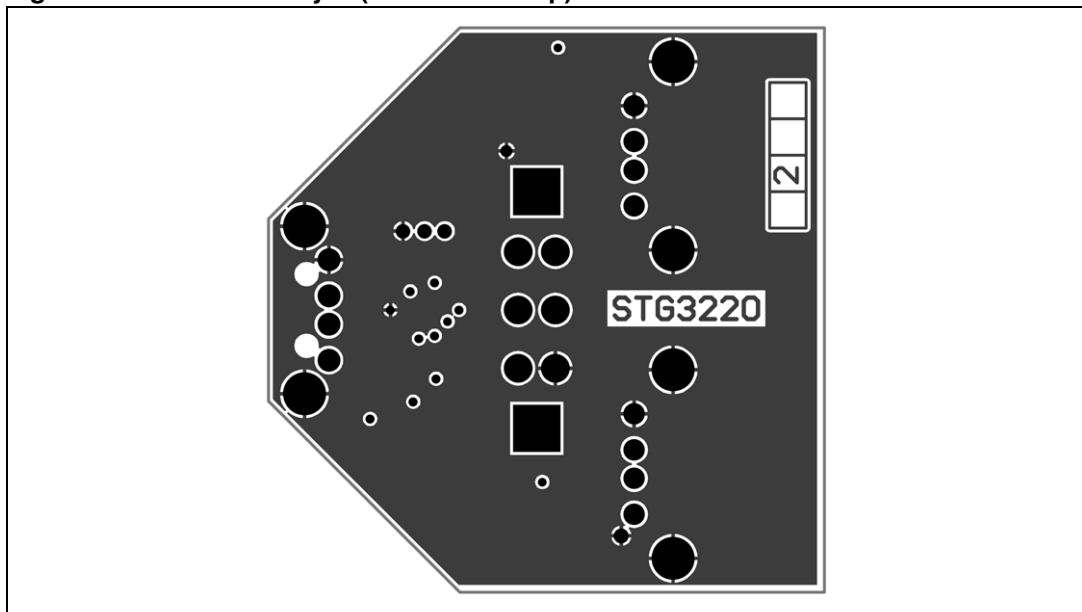


Figure 4. PCB mid2 layer (close to the bottom)

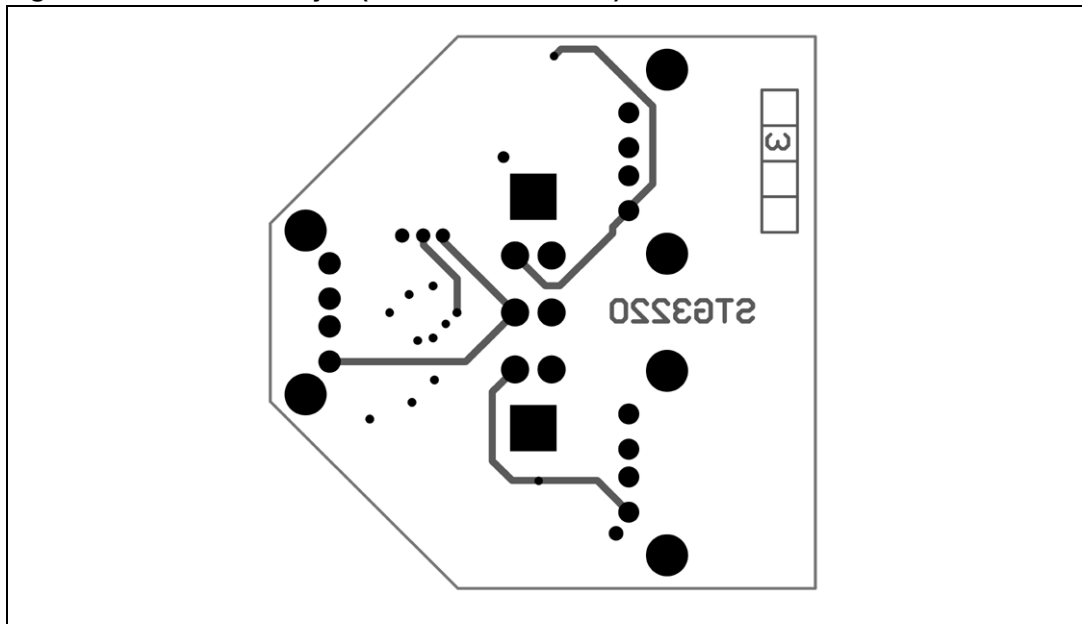


Figure 5. PCB bottom layer

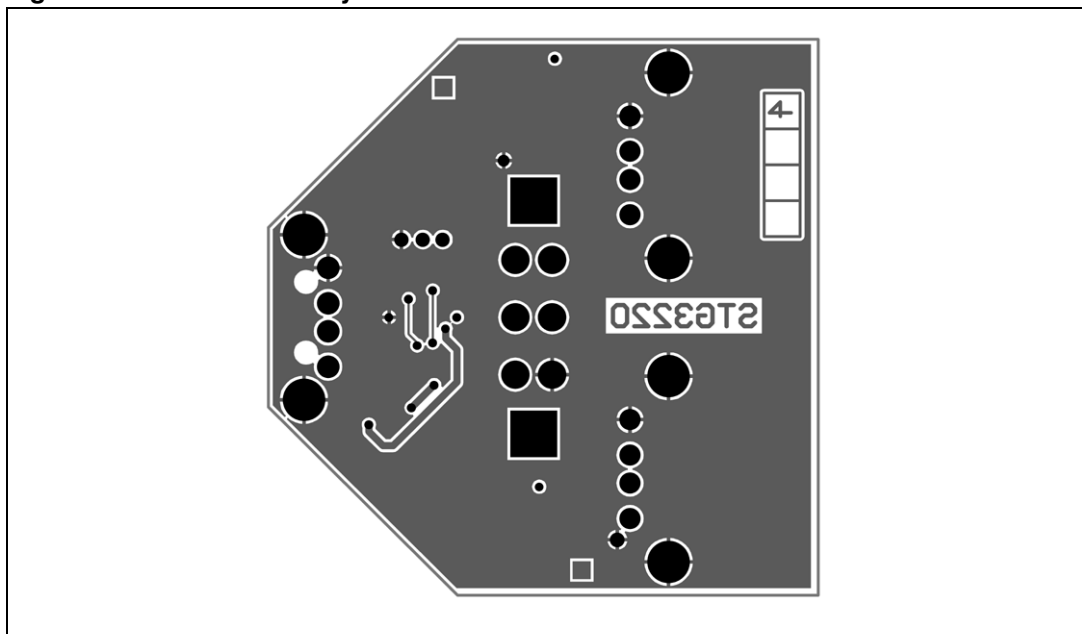
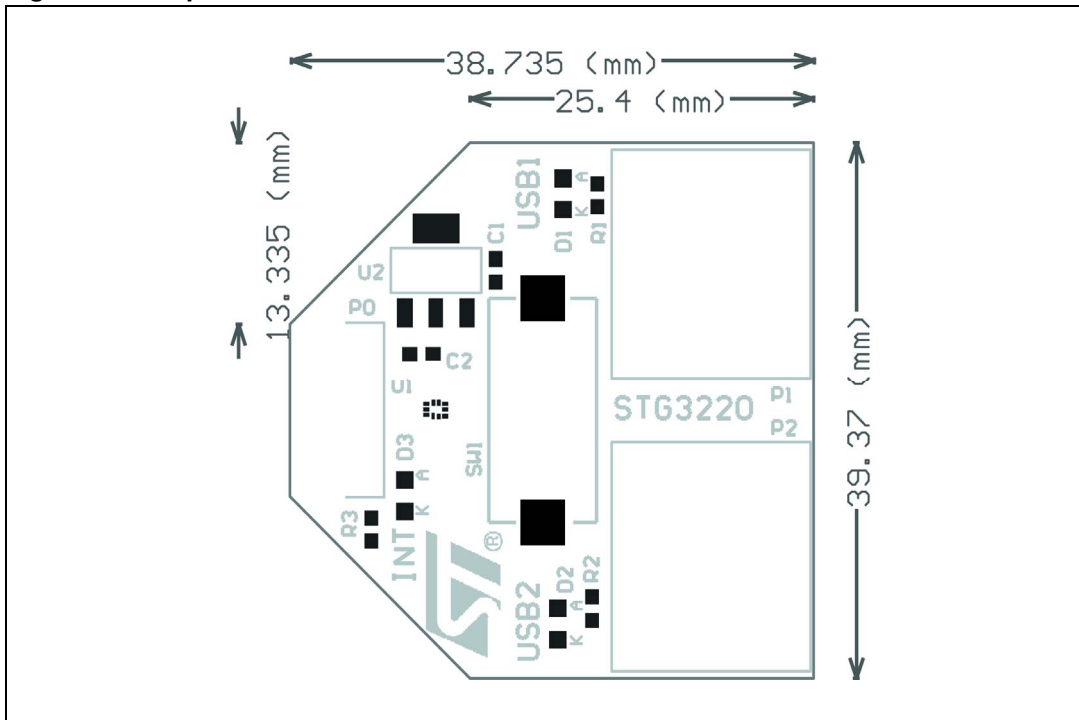


Figure 6. Top view and dimensions



3 Revision history

Table 3. Document revision history

Date	Revision	Changes
28-Aug-2012	1	Initial release.

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