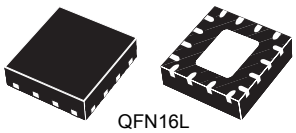
STG3692

Datasheet

Low voltage high bandwidth quad SPDT switch



QFN16L
(2.6x1.8 mm)

Features

- Ultra low power dissipation:
  - I_{CC} = 3 µA at T_A = 85 °C
- Low on-resistance:
  - $R_{DS(on)}$ = 4.6 Ω (T_A = 25 °C) at V_{CC} = 4.3 V
  - $R_{DS(on)}$ = 5.8 Ω (T_A = 25 °C) at V_{CC} = 3.0 V
- Wide operating voltage range:
  - V_{CC} (opr) = 1.65 V to 4.3 V single supply
- 4.3 V tolerant and 1.8 V compatible threshold on digital control input at V_{CC} = 2.3 V to 3.0 V
- Typical bandwidth (-3 dB) at 500 MHz on all channels
- Latch-up performance exceeds 100 mA per JESD 78, Class II
- ESD performance exceeds JESD22
  - 2000-V human body model (A114-A)
- USB (2.0) high speed (480 Mbps) signal switching compliant

Description

The STG3692 is a high-speed CMOS low voltage quad analog SPDT (single pole dual throw) switch or 2:1 multiplexer /demultiplexer switch developed in silicon gate C2MOS technology. It is designed to operate from 1.65 V to 4.3 V, making this device ideal for portable applications.

The nSEL inputs are provided to control the switch. The switch S1 is ON (connected to common ports Dn) when the nSEL input is held high and OFF (high impedance state exists between the two ports) when SEL is held low; the switch S2 is ON (connected to common port D) when the nSEL input is held low and OFF (high impedance state exists between the two ports) when nSEL is held high. Additional key features are fast switching speed, break-before-make delay time and ultra low power consumption. All inputs and outputs are equipped with protection circuits against static discharge, giving them ESD immunity and transient excess voltage.

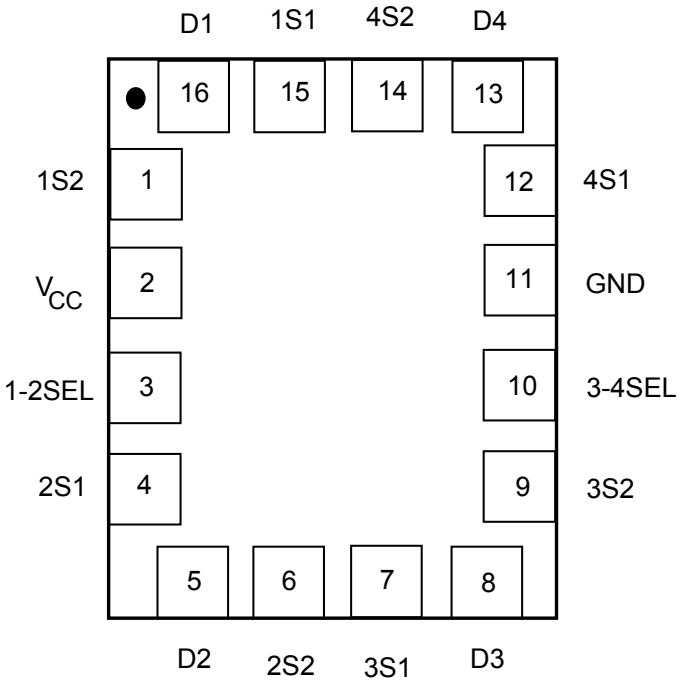
Product status link
STG3692

Product summary	
Order code	STG3692QTR
Package	QFN16L (2.6x1.8 mm)
Packing	Tape and reel

1 Pin settings

1.1 Pin connections

Figure 1. **Pin connection (top through view)**



1.2 Pin description

Table 1. **Pin description**

Pin	Symbol	Name and function
15, 1	1S1, 1S2	Independent channels
4, 6	2S1, 2S2	
7, 9	3S1, 3S2	
12, 14	4S1, 4S2	
16, 5, 8, 13	D1, D2, D3, D4	Common channels
3, 10	1-2SEL, 3-4SEL	Control
2	V_{CC}	Positive supply voltage
11	GND	Ground (0 V)

Note: Exposed pad must be soldered to a floating plane. Do not connect to power or ground.

2 Device summary

Figure 2. **Input equivalent circuit**

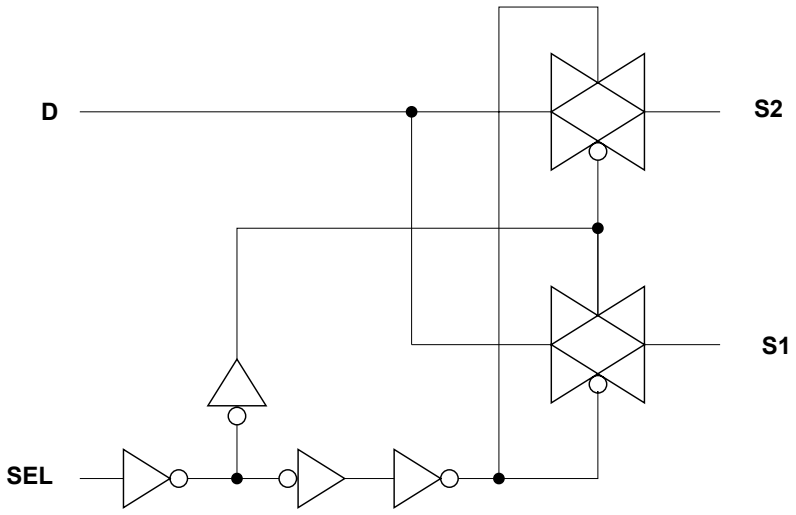


Table 2. **Truth table**

SEL	SWITCH S1	SWITCH S2
H	ON	OFF(1)
L	OFF(1)	ON

1. *High impedance*

3 Maximum ratings

Stressing the device above the rating listed in the absolute maximum ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE program and other relevant quality documents.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	-0.5 to 5.5	V
V_I	DC input voltage	-0.5 to V_{CC} + 0.5	V
V_{IC}	DC control input voltage	-0.5 to 5.5	V
V_O	DC output voltage	-0.5 to V_{CC} + 0.5	V
I_{IKC}	DC input diode current on control pin (V_{SEL}<0 V)	-50	mA
I_{IK}	DC input diode current (V_{SEL}<0 V)	±50	mA
I_{OK}	DC output diode current	±20	mA
I_O	DC output current	±128	mA
I_{OP}	DC output current peak (pulse at 1 ms, 10% duty cycle)	±300	mA
I_{CC} or I_{GND}	DC V_{CC} or ground current	±100	mA
P_D	Power dissipation at T_A = 70 °C[1]	1120	mW
T_{stg}	Storage temperature	-65 to 150	°C
T_L	Lead temperature (10 s)	300	°C

1. *Derate above 70 °C by 18.5 mW/C.*

3.1 Recommended operating conditions

Table 4. Recommended operating conditions

Symbol	Parameters		Value	Unit
V_{CC}	Supply voltage		1.65 to 4.3	V
V_I	Input voltage		0 to V_{CC}	
V_{IC}	Control input voltage		0 to 4.3	
V_O	Output voltage		0 to V_{CC}	
T_{op}	Operating temperature		-40 to 85	°C
dt/dv	Input rise and fall time control input	V_{CC} = 1.65 V to 2.7 V	0 to 20	ns/V
		V_{CC} = 3.0 to 4.3 V	0 to 10	

4 Electrical characteristics

Table 5. DC specifications

Symbol	Parameter	Test conditions		Value					Unit
		V_{CC} (V)		T_A = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
V_{IH}	High level input voltage	1.65 -1.95		0.65 V_{CC}			0.65 V_{CC}		V
		2.3-2.5		1.2			1.2		
		2.7-3.0		1.3			1.3		
		3.3-3.6		1.4			1.4		
		4.3		1.6			1.6		
V_{IL}	Low level input voltage	1.65-1.95				0.25			V
		2.3-2.5				0.25			
		2.7-3.0				0.25			
		3.3-3.6				0.30			
		4.3				0.40			
R_{PEAK}	Switch-on peak resistance	1.8	V_S = 0 V to V_{CC}, I_S = 8 mA		12	16			Ω
		2.7			6.3	8			
		3			5.8	7.5			
		3.7			5	6.5			
		4.3			4.6	6.0			
R_{ON}	Switch-on resistance	3	V_S = 3 V, I_S = 8 mA		4	5.2			Ω
		3	V_S = 0.8 V, I_S = 8 mA		5	6.5			
ΔR_{ON}	ON-resistance match between channels (1)	1.8	V_S @ R_{ON} max., I_S = 8 mA						Ω
		2.7							
		3			0.3				
		3.7							
		4.3							
R_{FLAT}	ON-resistance flatness (2)	1.8	V_S = 0 V to V_{CC}, I_S = 8 mA		6.6				Ω
		2.7			2				
		3			1.7				
		3.7			1.5				
		4.3			1.6				
I_{OFF}	OFF-state leakage current (SN)	4.3	V_S = 0.3 V and V_D = 4 V or V_S = 4 V and V_D = 0.3 V			±20		±100	nA
I_{ON}	ON-state leakage current (D)	4.3	V_S = 0.3 V and V_D = 4 V or V_S = 4 V and V_D = 0.3 V			±20		±100	nA

Symbol	Parameter	Test conditions		Value					Unit
		V_{CC} (V)		T_A = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
I_{SEL}	SEL input leakage current	0 to 4.3	V_{SEL} = 0 to 4.3 V			±0.1		2	µA
I_{CC}	Quiescent supply current	1.65 to 4.3	V_{SEL} = V_{CC} or GND			0.1		3	µA
I_{CCLV}	Quiescent supply current low voltage driving	4.3	V_{1-2SEL}, V_{3-4SEL} = 1.65 V		20	25		35	µA
			V_{1-2SEL}, V_{3-4SEL} = 1.80 V		17	22		30	
			V_{1-2SEL}, V_{3-4SEL} = 2.60 V		6	11		20	

1. *ΔRon = max. |mSN-nSN|, where m = 1..4 and n = 1..4, N = 1..2*
2. *Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.*

Table 6. Analog switch characteristics (C_L = 35 pF, R_L = 50 Ω, t_r = t_f ≤ 5 ns)

Symbol	Parameter	Test conditions		Value					Unit
		V_{CC} (V)		T_A = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
t_{PLH}, t_{PHL}	Propagation delay	1.65 -1.95			0.3				ns
		2.3-2.7			0.3				
		3.0-3.3			0.25				
		3.6-4.3			0.25				
t_{ON}	Turn-on time	1.65 -1.95	V_S = 0.8 V		31				ns
		2.3-2.7	V_S = 1.5 V		20	26		34	
		3.0-3.3			15	20		26	
		3.6-4.3			12	15		20	
t_{OFF}	Turn-off time	1.65 -1.95	V_S = 0.8 V		22				ns
		2.3-2.7	V_S = 1.5 V		14	18		23	
		3.0-3.3			11	14		18	
		3.6-4.3			10	13		17	
t_D	Break- before-make time delay	1.65-1.95	C_L = 35 pF, R_L = 50 Ω, V_S = 1.5 V	1	7				ns
		2.3-2.7		1	5				
		3.0-3.3		1	4				
		3.6-4.3		1	3				
Q	Charge injection	1.65	C_L = 100 pF, V_{GEN} = 0 V, R_{GEN} = 0 Ω		2.8				pC
		2.3			3.5				
		3			3.8				
		4.3			5				

Table 7. Analog switch characteristics (C_L = 5 pF, R_L = 50 Ω, T_A = 25 °C)

Symbol	Parameter	Test conditions		Value					Unit
		V_{CC} (V)		T_A = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
OIRR	Off isolation(1)	1.65 - 4.3	DC bias = V_{CC}/2, f = 1 MHz, signal = 0 dBm		-79				dB
			DC bias = V_{CC}/2, f = 10 MHz, signal = 0 dBm		-60				
X_{talk}	Crosstalk	1.65 - 4.3	DC bias = V_{CC}/2, f = 1 MHz, signal = 0 dBm		-78				dB
			DC bias = V_{CC}/2, f = 10 MHz, signal = 0 dBm		-61				
B_W	-3 dB bandwidth	3.0 - 4.3	R_L = 50 Ω, DC bias = V_{CC}/2, signal = 0 dBm		500				MHz
D_G	Differential gain	3.0 - 4.3	R_L = 150 Ω		0.64				%
D_P	Differential phase	3.0 - 4.3	R_L = 150 Ω		0.1				deg
C_{IN}	Control pin input capacitance	3.3	f = 1 MHz, V_S= 0.1 Vpp		6.2				pF
C_{ON}	Sn port capacitance when switch is enabled	3.3	f = 1 MHz, V_S= 0.1 Vpp		12				pF
C_{OFF}	Sn port capacitance when switch is disabled	3.3	f = 1 MHz, V_S= 0.1 Vpp		5				pF

1. *Off isolation = 20 Log10 (V_D/V_S), V_D = output. V_S = input to off switch.*

Table 8. USB related AC electrical characteristics

Symbol	Parameter	Test conditions		Value					Unit
		V_{CC} (V)		T_A = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
$t_{SK(0)}$	Channel-to-channel skew	3.0 to 3.6	C_L = 10 pF		26				ps
$t_{SK(P)}$	Skew of opposite transition of the same output	3.0 to 3.6	C_L = 10 pF		60				ps
T_J	Total jitter	3.0 to 3.6	R_L = 50 Ω, C_L = 10 pF, t_R = t_F = 750 ps at 480 Mbps		130				ps

5 Test circuits

Figure 3. **On-resistance**

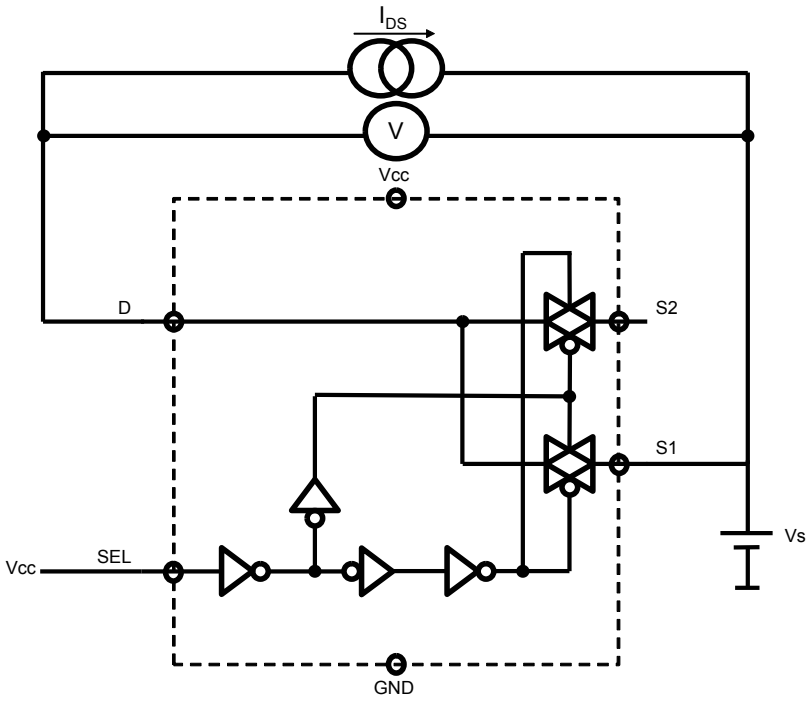


Figure 4. **Bandwidth**

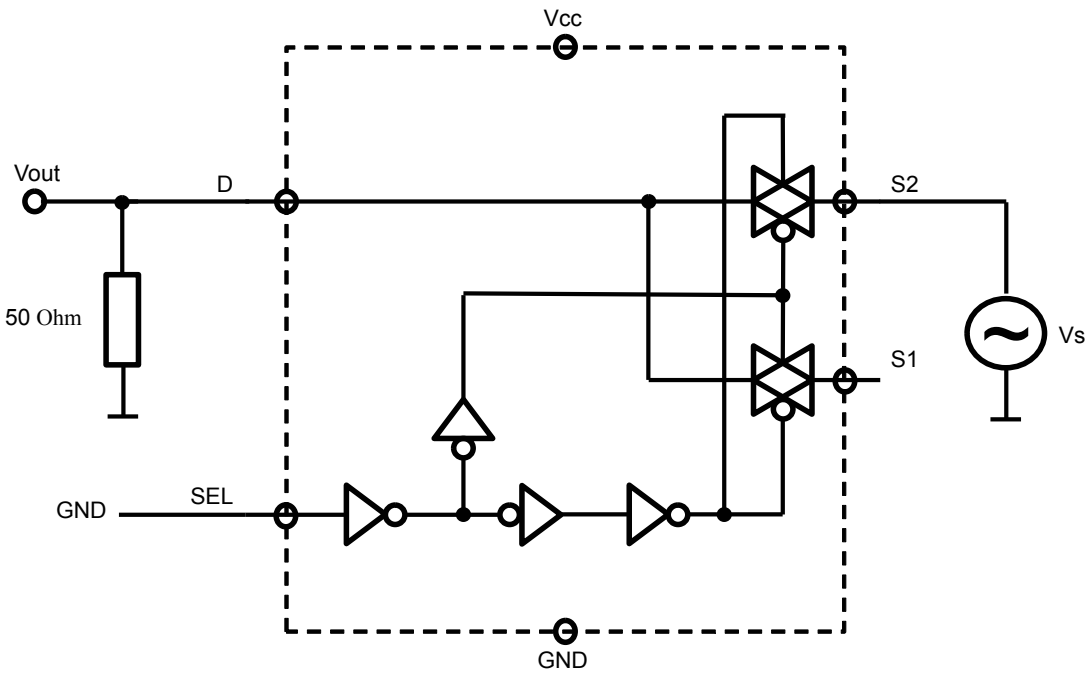


Figure 5. **Off leakage**

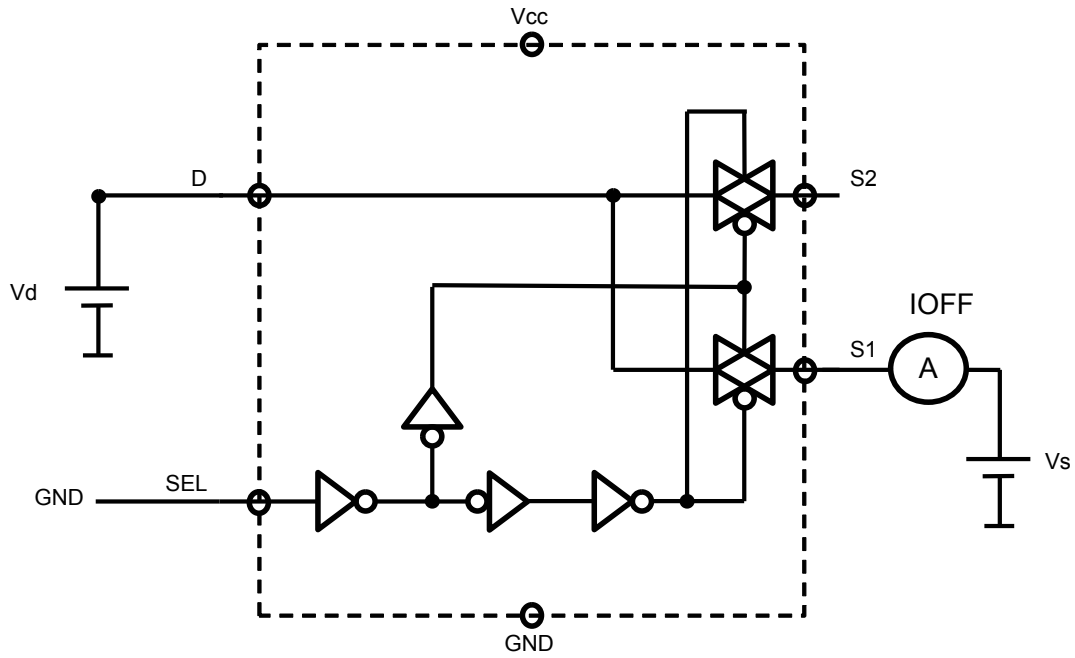


Figure 6. **On leakage**

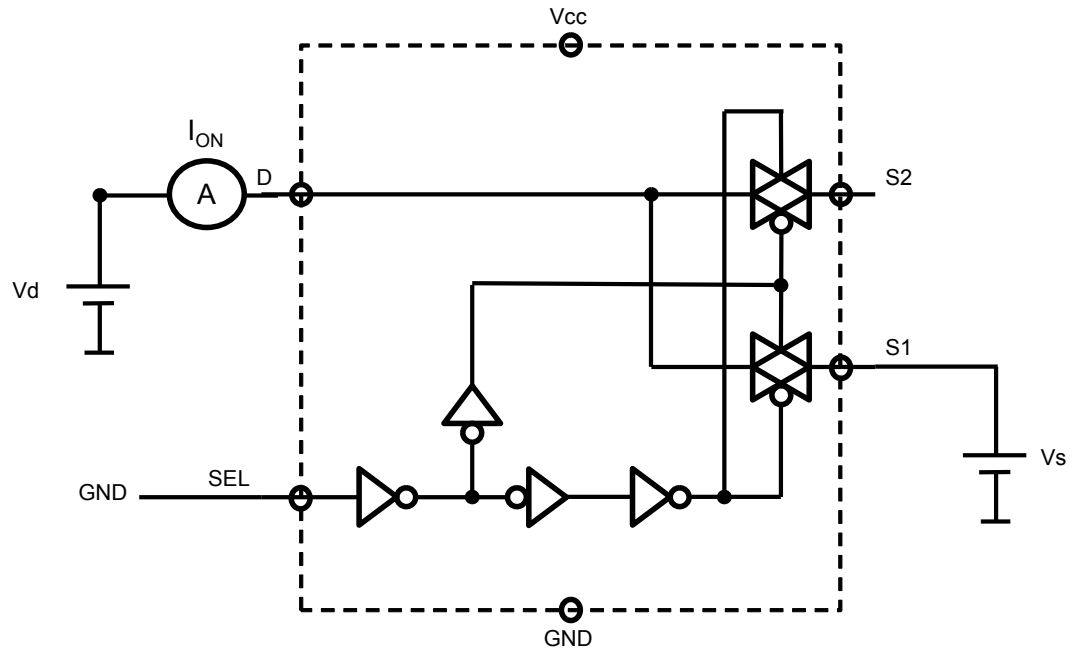


Figure 7. **Channel-to-channel crosstalk**

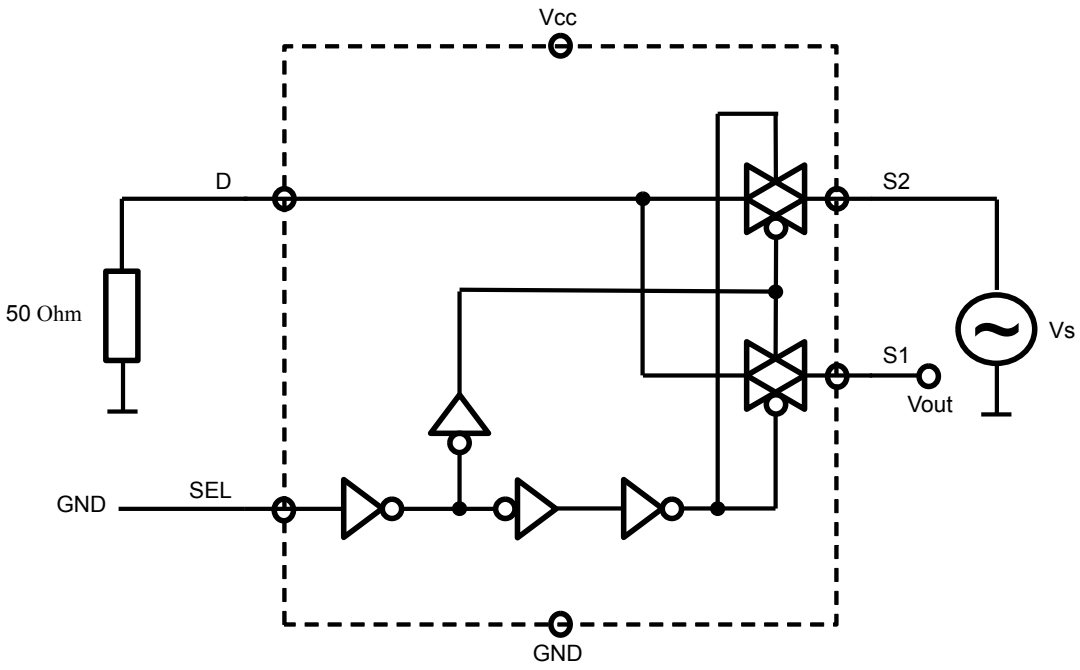


Figure 8. **OFF isolation**

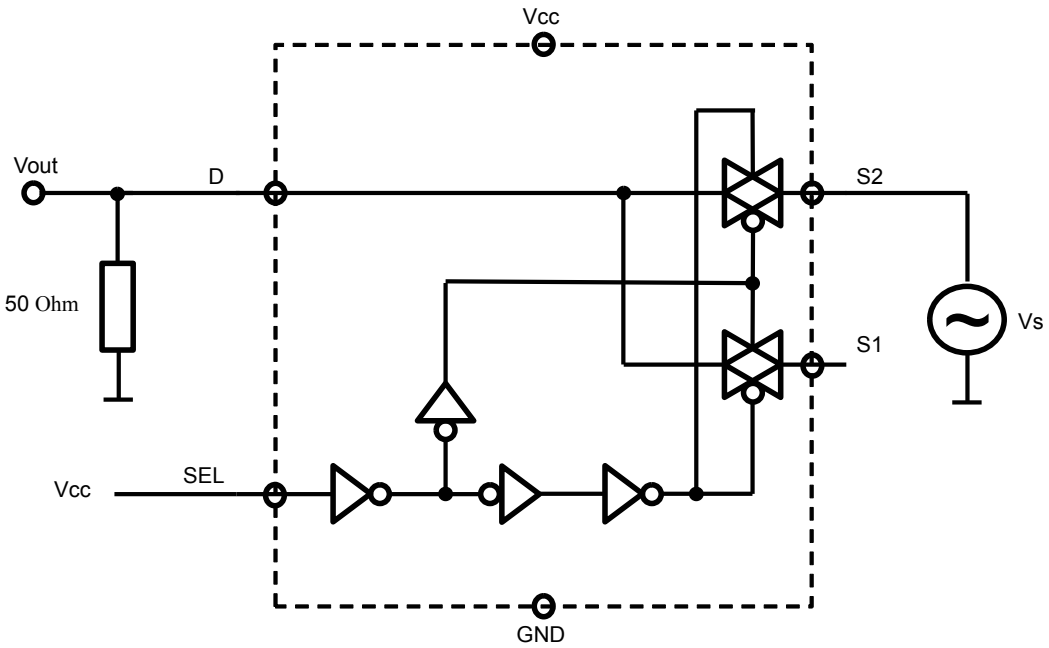
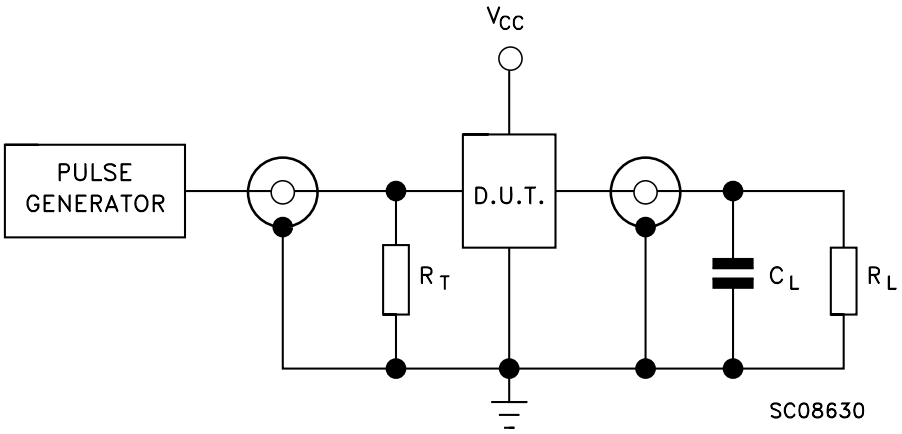


Figure 9. **Test circuits**



Note:
1. *C_L = 5/35 pF or equivalent: (includes jig capacitance)*
2. *R_L = 50 Ω or equivalent*
3. *R_T = Z_{OUT} of pulse generator (typically 50 Ω)*

Figure 10. **Break-before-make time delay**

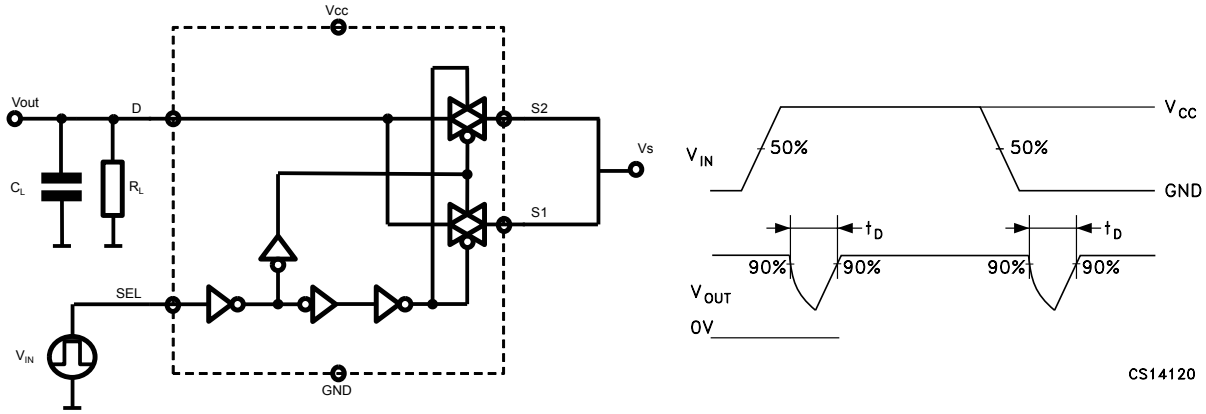


Figure 11. **Switching time and charge injection (V_{GEN} = 0 V, R_{GEN} = 0 Ω, RL = 1 MΩ, CL= 100 pF)**

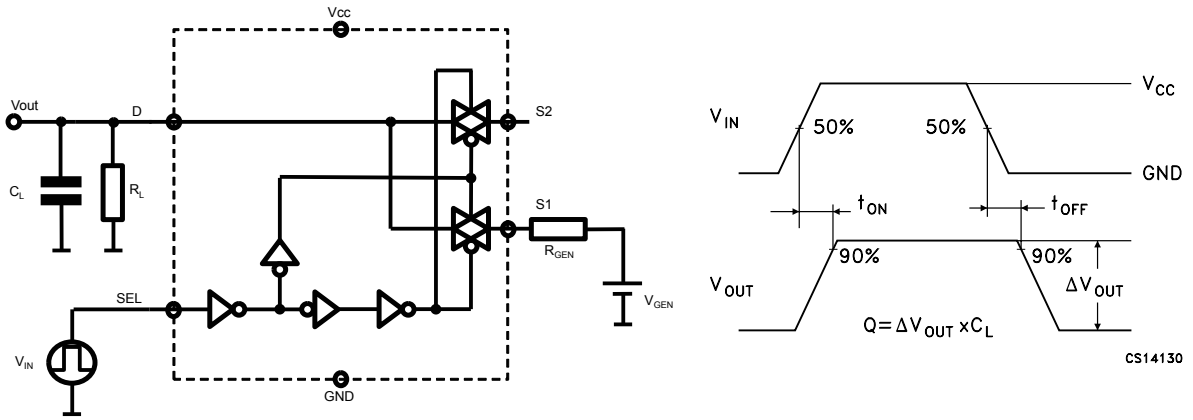
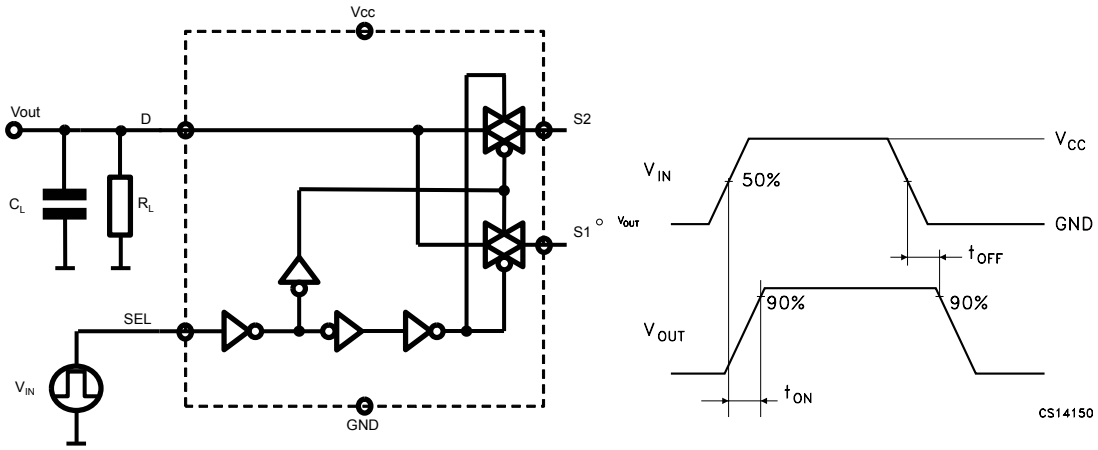


Figure 12. **Turn-on, turn-off delay time**



6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

6.1 QFN16 (2.6x1.8 mm) package information

Figure 13. QFN16L (2.6x1.8 mm) package outline

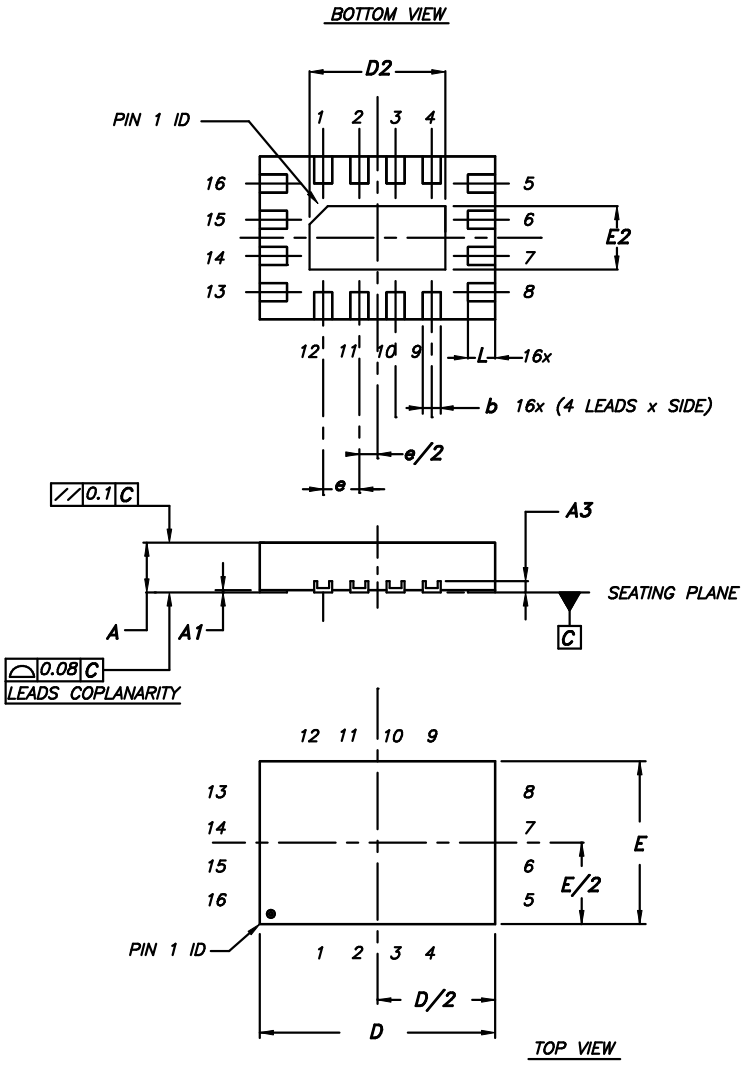
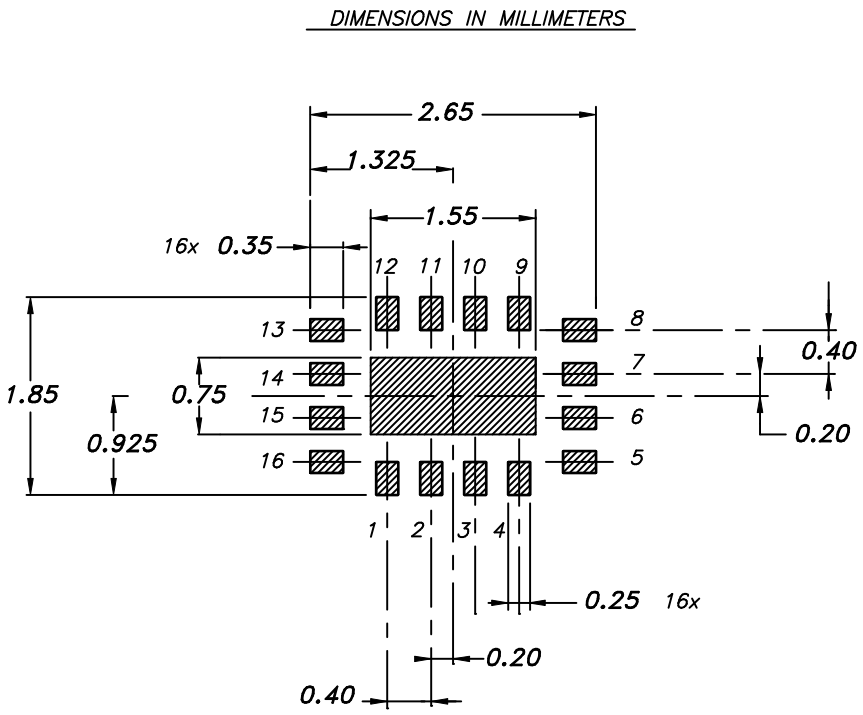


Table 9. **QFN16L (2.6x1.8 mm) package mechanical data**

Symbol	mm		
	Min.	Typ.	Max.
A	0.45	0.5	0.55
A1	0	0.02	0.05
A3		0.127	
b	0.15	0.2	0.25
D	2.55	2.6	2.65
D2	1.45	1.5	1.55
E	1.75	1.8	1.85
E2	0.65	0.7	0.75
e		0.4	
L	0.25	0.3	0.35

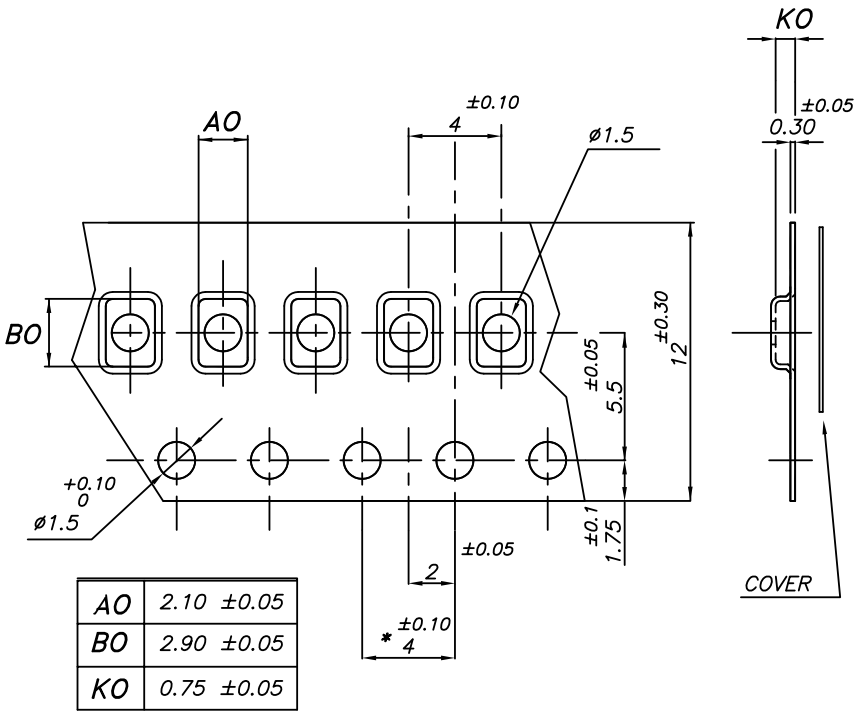
Note: VFQFPN - Standard for thermally enhanced vey fine pitch quad flat package no leads. The leads size is comprehensive of the thickness of the leads finishing material. Dimensions do not include mold protusion. Package outline exclusive of metal burrs dimensions. Shipping media tape and reel units: 3000.

Figure 14. **QFN16L (2.6x1.8 mm) recommended footprint**



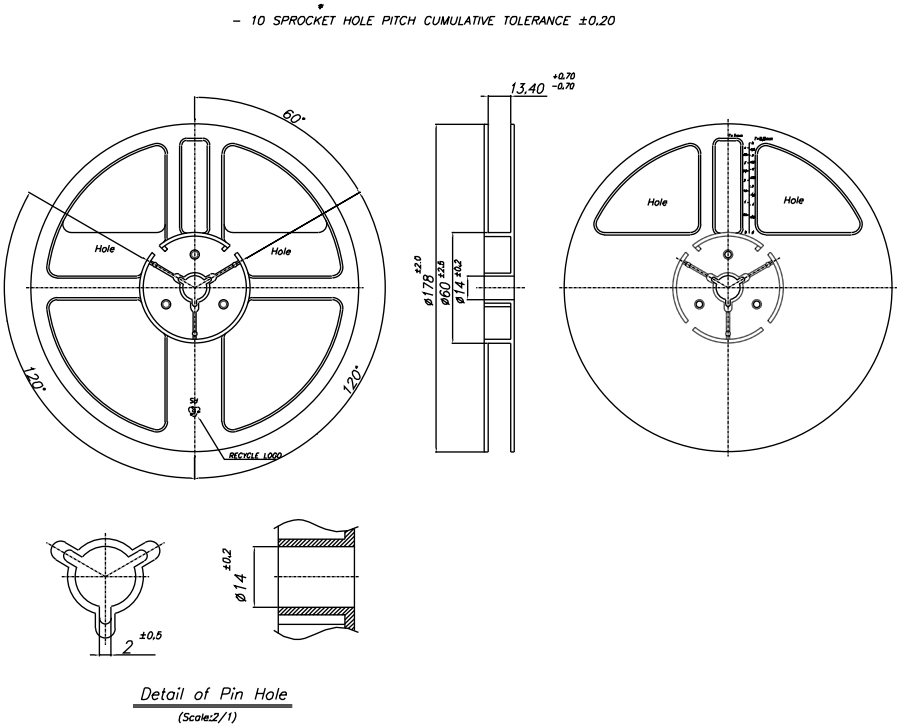
6.2 QFN16L (2.6x1.8 mm) packing information

Figure 15. **QFN16L (2.6x1.8 mm) carrier tape**



AO	2.10 ±0.05
BO	2.90 ±0.05
KO	0.75 ±0.05

Figure 16. **QFN16L (2.6x1.8 mm) reel**



Revision history

Table 10. **Document revision history**

Date	Version	Changes
11-Oct-2006	1	Initial release.
08-Nov-2006	2	Added feature in cover page.
08-Jan-2007	3	Mechanical data updated.
03-Jul-2007	4	C_{ON} and C_{OFF} values updated on Table 8 on page 8.
05-May-2010	5	Document reformatted no content change.
30-Jun-2010	6	Update of product maturity.
14-Oct-2019	7	Updated Section 5 Test circuits.
04-Aug-2021	8	Updated ISEL, ICC max. value in Table 5, BW typ. value, OIRR and Xtalk test conditions in Table 7.
07-Dec-2021	9	Updated Table 5. DC specifications.

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