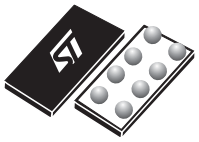
# STG4160

# Low voltage 0.5 Ω single SPDT switch with break-before-make feature and 15 kV contact ESD protection

**Datasheet - production data**



**Flip Chip 8**

## Features

- Wide operating voltage range:
  $V_{CC}$ (opr.) = 1.65 to 4.8 V
- Low power dissipation:
  $I_{CC}$ = 0.2 µA (max.) at $T_A$ = 85 °C
- Low on-resistance:
  - $R_{ON}$ = 0.75 Ω ($T_A$ = 25 °C) at $V_{CC}$ = 2.25 V
  - $R_{ON}$ = 0.50 Ω ($T_A$ = 25 °C) at $V_{CC}$ = 3.0 V
  - $R_{ON}$ = 0.40 Ω ($T_A$ = 25 °C) at $V_{CC}$ = 4.3 V
- Separate supply voltage for switch and control pins
- Latch-up performance exceeds 100 mA per JESD 78, Class II
- ESD performance tested on common pin (D pin):
  - 15 kV IEC 61000-4-2 ESD, contact discharge
  - 8 kV HBM JESD22 A114-B Class II
- ESD performance tested on S1 and S2 pin:
  8 kV IEC 61000-4-2 ESD, contact discharge
- ESD performance test on all other pins:
  - 4 kV HBM (JESD22 A114-B Class II)
  - 400 V machine model (JESD22 A115-A)
  - 1500 V charged-device model (JESD22 C101)

## Applications

- Mobile phones

## Description

The STG4160 device is a high-speed CMOS low voltage single analog SPDT (single pole dual throw) switch or 2:1 multiplexer/demultiplexer switch fabricated in silicon gate $C^2MOS$ technology. It is designed to operate from 1.65 to 4.8 V, making this device ideal for portable applications. It offers low on-resistance (0.40 Ω typ.) at $V_{CC}$ = 4.3 V. The SEL inputs are provided to control the switches.

The switch S1 is ON (connected to the common port D) when the SEL input is held high and OFF (high impedance state exists between the two ports) when the SEL is held low. The switch S2 is ON (connected to the common port D) when the SEL input is held low and OFF (high impedance state exist between the two ports) when the SEL is held high.

Additional key features are fast switching speed, break-before-make delay time and ultra power consumption. All inputs and outputs are equipped with protection circuits against static discharge, giving them ESD immunity and transient excess voltage.

**Table 1. Device summary**

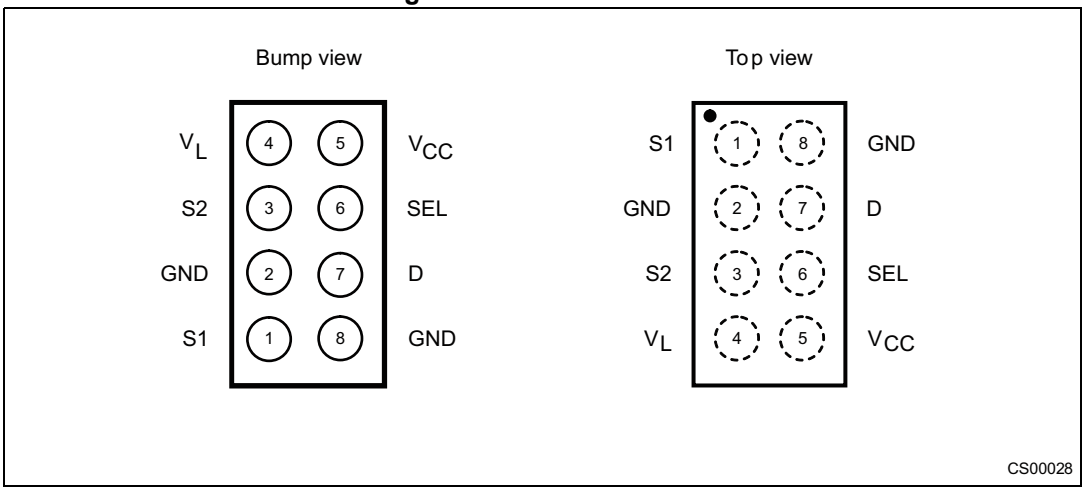
| Order code | Package | Packing |
|---|---|---|
| STG4160BJR | Flip Chip 8 | Tape and reel |

# Contents

# 1 Pin settings

## 1.1 Pin connections

**Figure 1. Pin connections**




## 1.2 Pin description

**Table 2. Pin assignment**

| Pin number | Symbol | Name and function |
|---|---|---|
| 1 | S1 | Independent channel |
| 2 | GND | Ground (0 V) |
| 3 | S2 | Independent channel |
| 4 | $V_L$ | Logic supply voltage |
| 5 | $V_{CC}$ | Positive supply voltage |
| 6 | SEL | Control |
| 7 | D | Common channel |
| 8 | GND | Ground (0 V) |

# 2 Logic diagram

**Figure 2. Functional diagram**

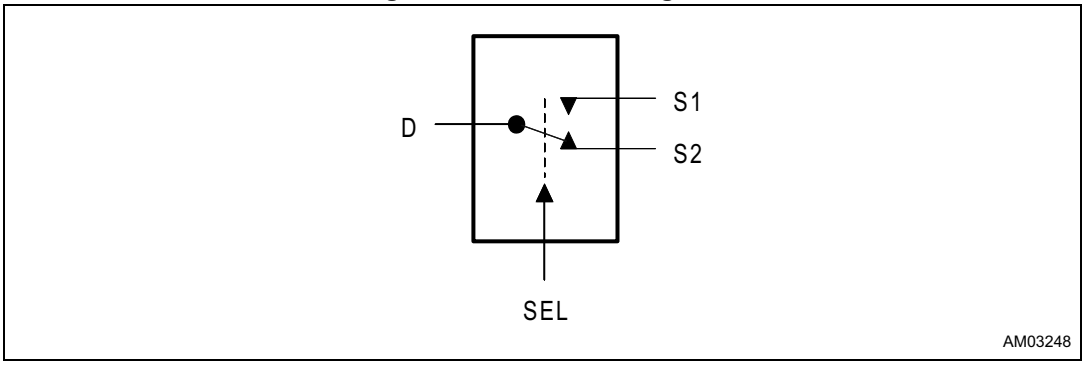



**Figure 3. Circuit equivalent logic**

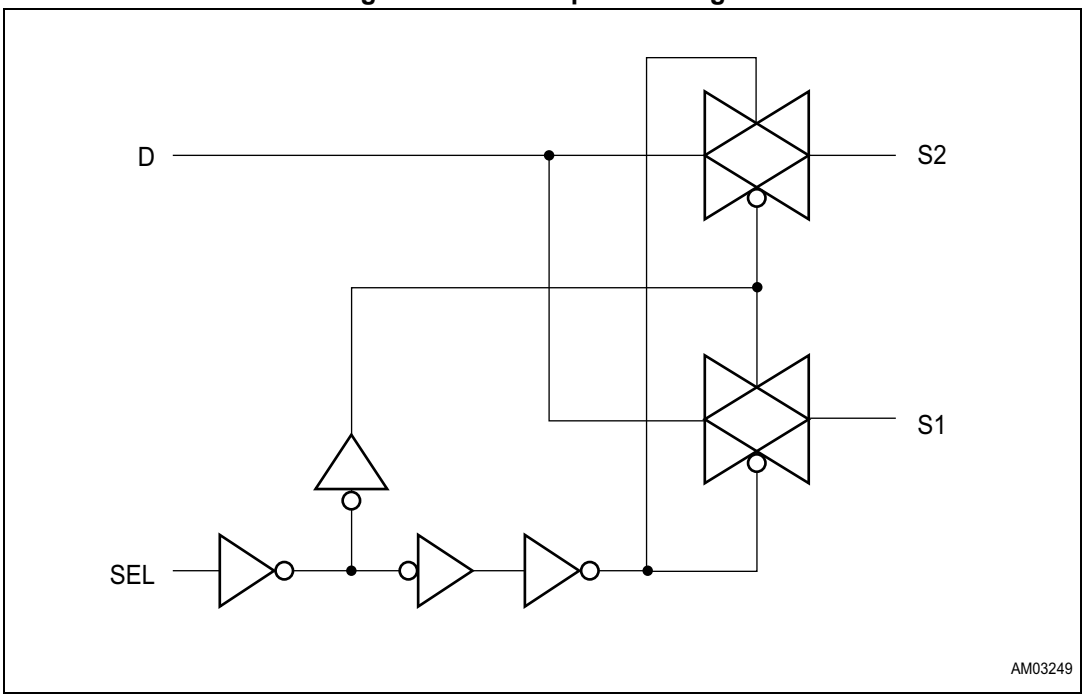



**Table 3. Truth table**

| SEL | Switch S1 | Switch S2 |
|---|---|---|
| H | ON | OFF(1) |
| L | OFF(1) | ON |

1. High impedance.

# 3 Maximum ratings

Stressing the device above the rating listed in *Table 4* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in *Table 5* of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics® SURE program and other relevant quality documents.

**Table 4. Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | Supply voltage | -0.5 to 5.5 | V |
| $V_L$ | Logic supply voltage | -0.5 to 5.5 | V |
| $V_I$ | DC input voltage | -0.5 to $V_{CC}$ + 0.5 | V |
| $V_{IC}$ | DC control input voltage | -0.5 to $V_L$ + 5.5 | V |
| $V_O$ | DC output voltage | -0.5 to $V_{CC}$ + 0.5 | V |
| $I_{IKC}$ | DC input diode current on control pin ($V_{SEL}$ < 0 V) | - 50 | mA |
| $I_{IK}$ | DC input diode current ($V_{SEL}$ < 0 V) | ± 50 | mA |
| $I_{OK}$ | DC output diode current | ± 20 | mA |
| $I_O$ | DC output current | ± 300 | mA |
| $I_{OP}$ | DC output current peak (pulse at 1 ms, 10% duty cycle) | ± 500 | mA |
| $I_{CC}$ or $I_{GND}$ | DC $V_{CC}$ or ground current | ± 100 | mA |
| $P_D$ | Power dissipation at $T_A$ = 70 °C(1) | 500 | mW |
| $T_{stg}$ | Storage temperature | -65 to 150 | °C |
| $T_L$ | Lead temperature (10 sec.) | 260 | °C |

1. Derate above 70 °C by 18.5 mW/C.

**Table 5. Recommended operating conditions**

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 1.65 to 4.8 | V |
| $V_L$ | Logic supply voltage(1) | | 1.65 to $V_{CC}$ | V |
| $V_I$ | Input voltage | | 0 to $V_{CC}$ | V |
| $V_{IC}$ | Control input voltage | | 0 to $V_L$ | V |
| $V_O$ | Output voltage | | 0 to $V_{CC}$ | V |
| $T_{op}$ | Operating temperature | | -40 to 85 | °C |
| dt/dv | Input rise and fall time control input | $V_L$ = 1.65 to 2.7 V | 0 to 20 | ns/V |
| | | $V_L$= 3.0 to 4.8 V | 0 to 10 | |

1. $V_L$ pin should not be left floating.

# 4 Electrical characteristics

**Table 6. DC specifications**

| Symbol | Parameter | $V_{CC}$ (V) | $V_L$ (V) | Test conditions | Value | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | $T_A$ = 25 °C | | | -40 to 85 °C | | |
| | | | | | Min. | Typ. | Max. | Min. | Max. | |
| $V_{IH}$ | High level input voltage | 1.65 – 4.3 | 1.65 – 1.95 | | 1.25 | | | 1.25 | | V |
| | | | 2.3 – 2.7 | | 1.75 | | | 1.75 | | |
| | | | 3.0 – 3.6 | | 2.34 | | | 2.34 | | |
| | | | 4.3 | | 2.80 | | | 2.80 | | |
| $V_{IL}$ | Low level input voltage | 1.65 – 4.3 | 1.65 – 1.95 | | | | 0.6 | | 0.6 | V |
| | | | 2.3 – 2.7 | | | | 0.8 | | 0.8 | |
| | | | 3.0 – 3.6 | | | | 1.05 | | 1.05 | |
| | | | 4.3 | | | | 1.5 | | 1.5 | |
| $R_{ON}$ | On-resistance | 1.8 | 1.65 – 4.3 | $V_S$ = 0 V to $V_{CC}$<br>$I_S$ = 100 mA | | 1.5 | 2.5 | | 3.7 | Ω |
| | | 2.25 | | | | 0.75 | 1.0 | | 1.3 | |
| | | 3 | | | | 0.50 | 0.65 | | 0.8 | |
| | | 3.7 | | | | 0.45 | 0.55 | | 0.7 | |
| | | 4.3 | | | | 0.40 | 0.5 | | 0.65 | |
| $\Delta R_{ON}$ | On-resistance match between channels(1) | 1.8 | 1.65 – 4.3 | $V_S$ = 0 V to $V_{CC}$<br>$I_S$ = 100 mA | | 40 | | | | mΩ |
| | | 2.25 | | | | 20 | | | | |
| | | 3 | | | | 10 | | | | |
| | | 3.7 | | | | 10 | | | | |
| | | 4.3 | | | | 10 | | | | |
| $R_{FLAT}$ | On-resistance flatness(2) | 1.8 | 1.65 – 4.3 | $V_S$ = 0 V to $V_{CC}$<br>$I_S$ = 100 mA | | 1.0 | 1.7 | | 2.0 | mΩ |
| | | 2.25 | | | | 300 | 430 | | 550 | |
| | | 3 | | | | 150 | 190 | | 270 | |
| | | 3.7 | | | | 140 | 180 | | 230 | |
| | | 4.3 | | | | 140 | 180 | | 220 | |
| $I_{OFF}$ | Sn OFF state leakage current | 4.3 | 4.3 | $V_S$ = 0.3 to 4.0<br>$V_D$ = 0.3 to 4.0 | -30 | | 30 | -300 | 300 | nA |
| $I_{ON}$ | Sn ON state leakage current | 4.3 | 4.3 | $V_S$ = 0.3 to 4.0<br>$V_D$ = open | -30 | | 30 | -300 | 300 | nA |
| $I_D$ | D ON state leakage current | 4.3 | 4.3 | $V_S$ = open<br>$V_D$ = 0 to 4.0 | -30 | | 30 | -300 | 300 | nA |

**Table 6. DC specifications (continued)**

| Symbol | Parameter | $V_{CC}$ (V) | $V_L$ (V) | Test conditions | Value | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | $T_A$ = 25 °C | | | -40 to 85 °C | | |
| | | | | | Min. | Typ. | Max. | Min. | Max. | |
| $I_{CC}$ | Quiescent supply current | 1.65 – 4.3 | 1.65 – 4.3 | $V_{SEL}$ = $V_{CC}$ or GND | -0.05 | | 0.05 | -0.2 | 0.2 | µA |
| $I_{SEL}$ | SEL leakage current | 1.65 – 4.3 | 1.65 – 4.3 | $V_{SEL}$= 4.3V or GND | -0.2 | | 0.2 | -2 | 2 | µA |

1. $\Delta R_{ON} = R_{ON(Max)} - R_{ON(Min)}$.
2. Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.

**Table 7. AC electrical characteristics ($C_L$ = 35 pF, $R_L$ = 50 Ω, $t_r = t_f \leq$ 5 ns)**

| Symbol | Parameter | Test conditions | | | Value | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | $V_{CC}$ (V) | $V_L$ (V) | | $T_A$ = 25 °C | | | -40 to 85 °C | | |
| | | | | | Min. | Typ. | Max. | Min. | Max. | |
| $t_{PLH}$, $t_{PHL}$ | Propagation delay | 1.65 – 1.95 | 1.65 – 4.3 | | | 0.18 | | | | ns |
| | | 2.3 – 2.7 | | | | 0.14 | | | | |
| | | 3.0 – 3.3 | | | | 0.12 | | | | |
| | | 3.6 – 4.3 | | | | 0.12 | | | | |
| $t_{ON}$ | Turn-on time | 1.65 – 1.95 | 1.65 – 4.3 | $V_S$ = $V_{CC}$ $R_L$ = 50 Ω $C_L$ = 30 pF | | 70 | 123 | | 160 | ns |
| | | 2.3 – 2.7 | | | | 48 | 62 | | 80 | |
| | | 3 – 3.6 | | | | 33 | 43 | | 56 | |
| | | 4.3 | | | | 29 | 38 | | 49 | |
| $t_{OFF}$ | Turn-off time | 1.65 – 1.95 | 1.65 – 4.3 | $V_S$ = $V_{CC}$ $R_L$ = 50 Ω $C_L$ = 30 pF | | 36 | 45 | | 60 | ns |
| | | 2.3 – 2.7 | | | | 35 | 47 | | 62 | |
| | | 3 – 3.6 | | | | 30 | 40 | | 51 | |
| | | 4.3 | | | | 29 | 38 | | 50 | |
| $t_D$ | Break-before-make time delay | 1.65 – 1.95 | 1.65 – 4.3 | $C_L$ = 35 pF $R_L$ = 50 Ω $V_S$ = $V_{CC}$/2 | 10 | 42 | | | | ns |
| | | 2.3 – 2.7 | | | 10 | 22 | | | | |
| | | 3 – 3.6 | | | 5 | 15 | | | | |
| | | 4.3 | | | 5 | 12 | | | | |
| Q | Charge injection | 1.65 – 1.95 | 1.65 – 4.3 | $C_L$ = 1 nF $V_{GEN}$ = 0 V | | 75 | | | | pC |
| | | 2.3 – 2.7 | | | | 98 | | | | |
| | | 3.0 – 3.3 | | | | 133 | | | | |
| | | 3.6 – 4.3 | | | | 162 | | | | |

**Table 7. AC electrical characteristics ($C_L$ = 35 pF, $R_L$ = 50 Ω, $t_r = t_f \leq$ 5 ns) (continued)**

| Symbol | Parameter | Test conditions | | | Value | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | $V_{CC}$ (V) | $V_L$ (V) | | $T_A$ = 25 °C | | | -40 to 85 °C | | |
| | | | | | Min. | Typ. | Max. | Min. | Max. | |
| OIRR | OFF-isolation(1) | 1.65 – 4.3 | 4.3 | $V_S$ = 1 $V_{RMS}$ f = 100 kHz | | 77 | | | | dB |
| | | | | $V_S$ = 1 $V_{RMS}$ f = 1 MHz | | 67 | | | | |
| | | | | $V_S$ = 1 $V_{RMS}$ f = 5 MHz | | 50 | | | | |
| Xtalk | Crosstalk | 1.65 – 4.3 | 4.3 | $V_S$ = 1 $V_{RMS}$ f = 100 kHz | | 80 | | | | dB |
| | | | | $V_S$ = 1 $V_{RMS}$ f = 1 MHz | | 67 | | | | |
| | | | | $V_S$ = 1 $V_{RMS}$ f = 5 MHz | | 50 | | | | |
| THD | Total harmonic distortion | 2.3 – 4.3 | 4.3 | $R_L$ = 600 Ω $C_L$ = 50 pF $V_S = V_{CC}$ f = 600 Hz to 20 kHz | | 0.01 | | | | % |
| BW | -3 dB Bandwidth (switch ON) | 1.65 – 4.3 | 4.3 | $R_L$ = 50 Ω | | 50 | | | | MHz |

1. OFF-isolation = 20 $\log_{10}$ ($V_D/V_S$), $V_D$ = output, $V_S$ = input to off switch.

**Table 8. Capacitive characteristics**

| Symbol | Parameter | Test conditions | | | Value | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | $V_{CC}$ (V) | $V_L$ (V) | | $T_A$ = 25 °C | | | -40 to 85 °C | | |
| | | | | | Min. | Typ. | Max. | Min. | Max. | |
| $C_{SEL}$ | Control pin input capacitance | 1.8 – 4.3 | 1.8 – 4.3 | $V_L = V_{CC}$ | | 30 | | | | pF |
| $C_{SN}$ | Sn port capacitance | 1.8 – 4.3 | 1.8 – 4.3 | $V_L = V_{CC}$ | | 94 | | | | pF |
| $C_D$ | D port capacitance when the switch is enabled | 1.8 – 4.3 | 1.8 – 4.3 | $V_L = V_{CC}$ | | 227 | | | | pF |

# 5 Test circuits

**Figure 4. On-resistance**

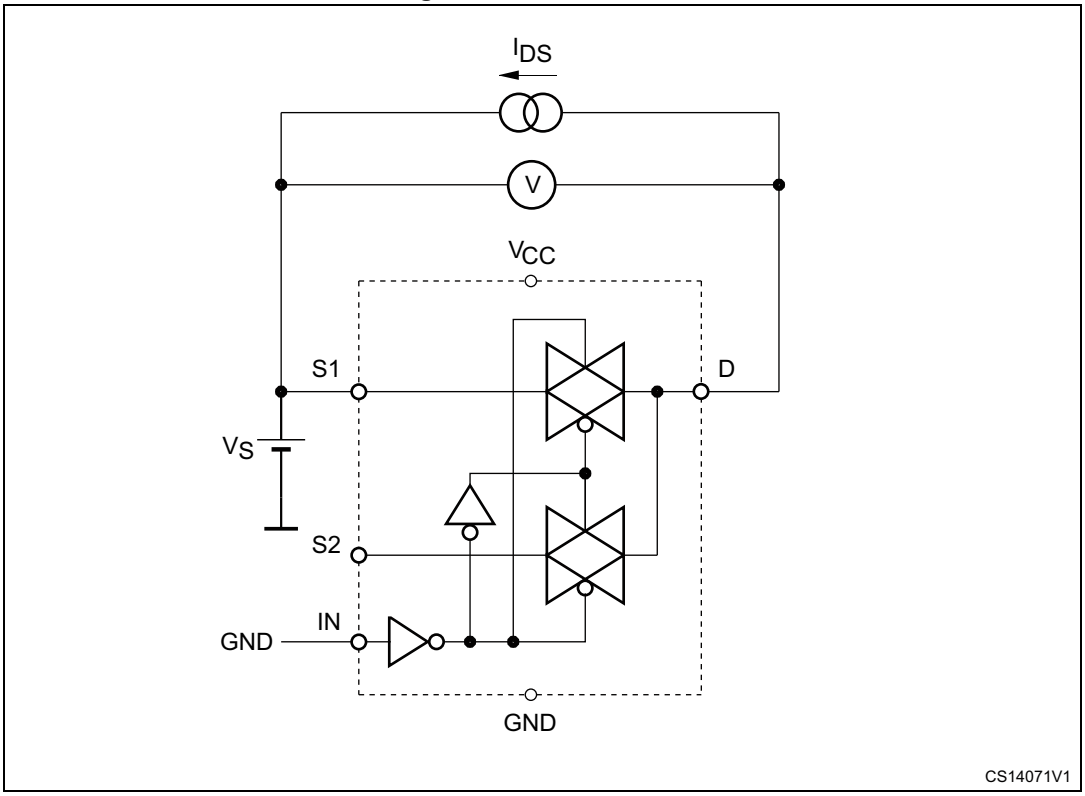



**Figure 5. Bandwidth**

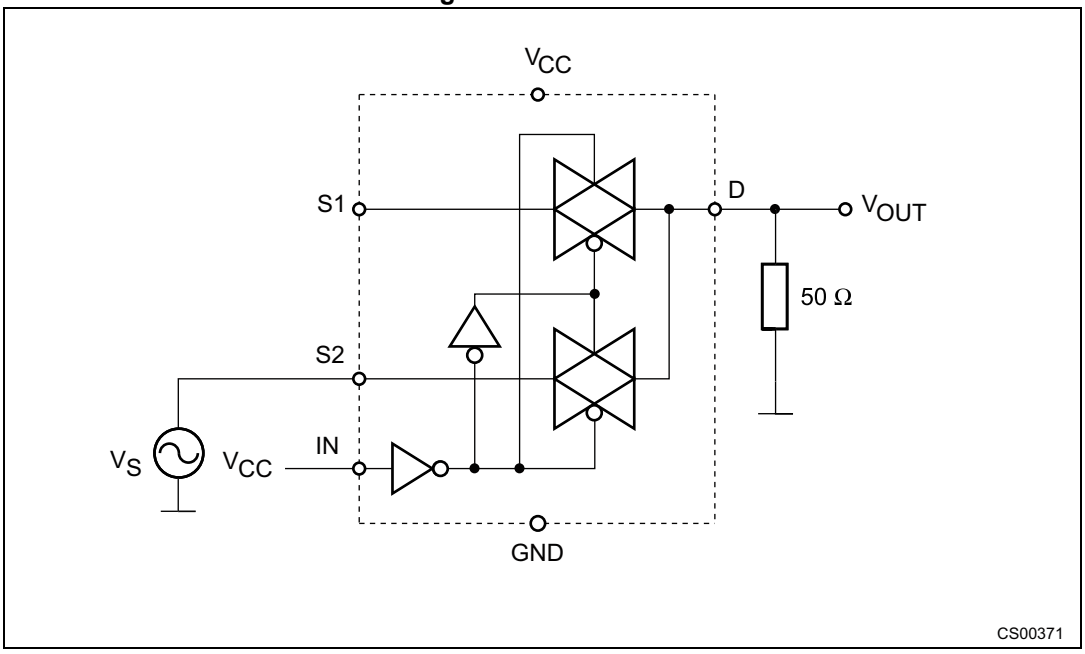


**Figure 6. OFF-leakage**

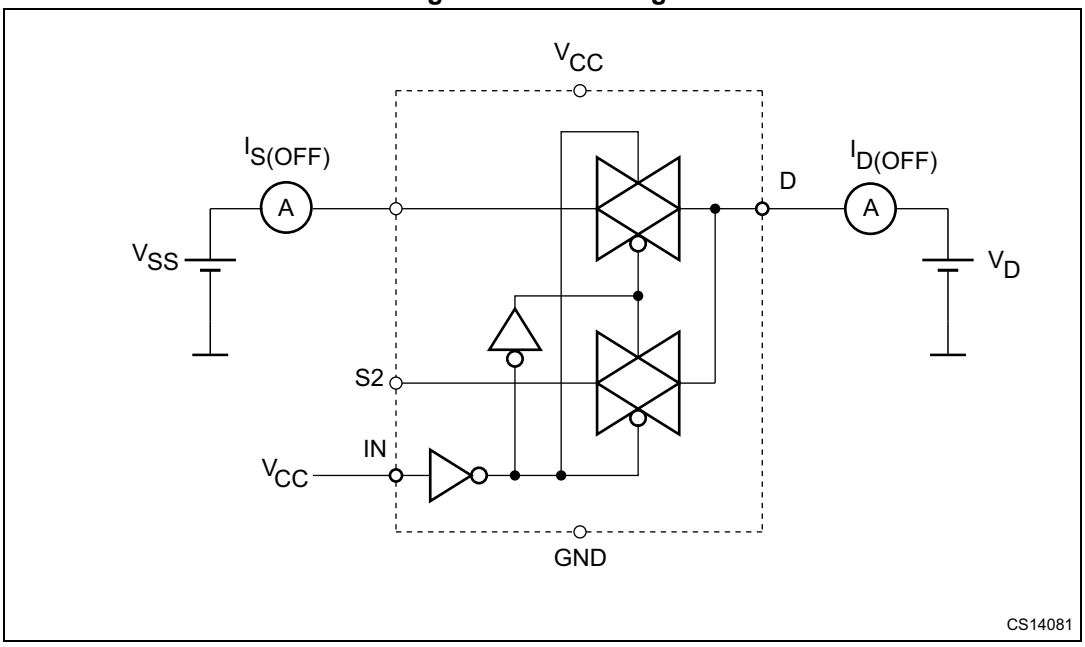



**Figure 7. Channel-to-channel crosstalk**

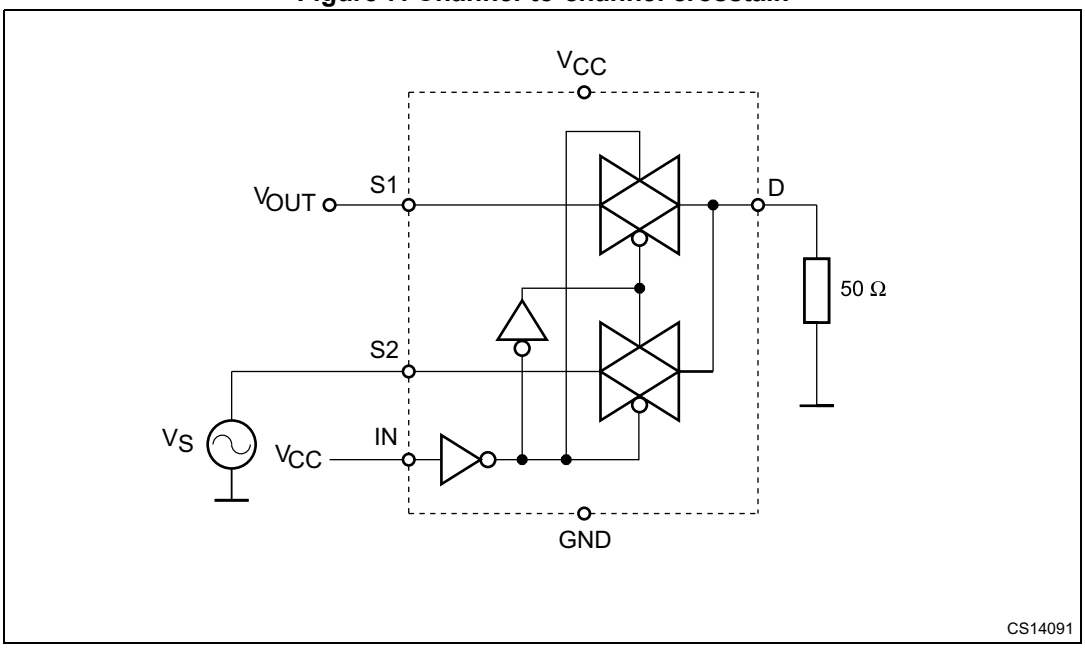


**Figure 8. OFF-isolation**

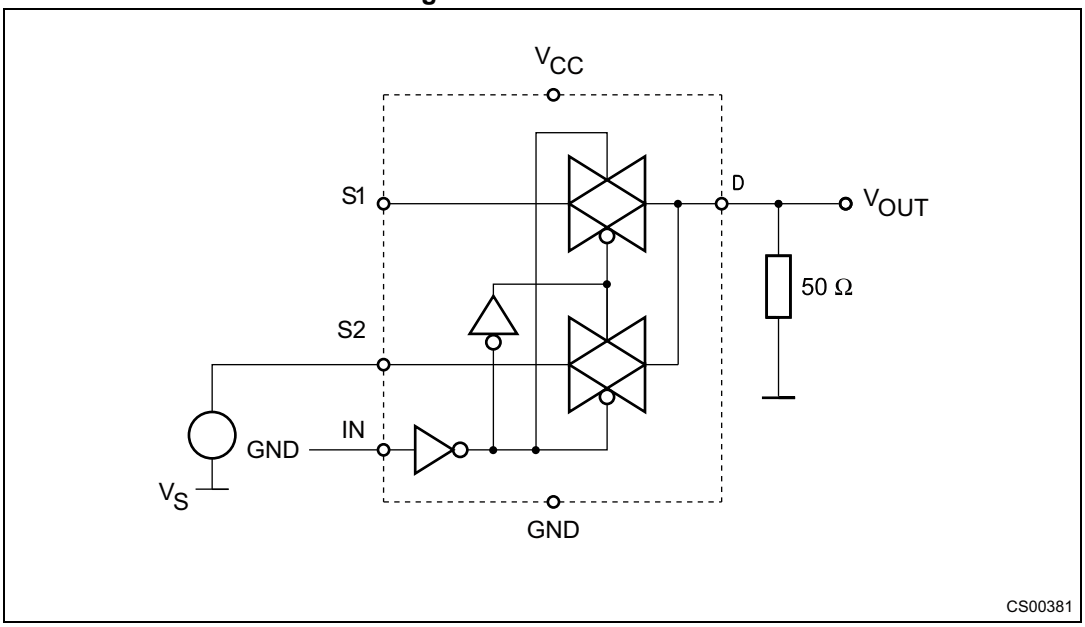
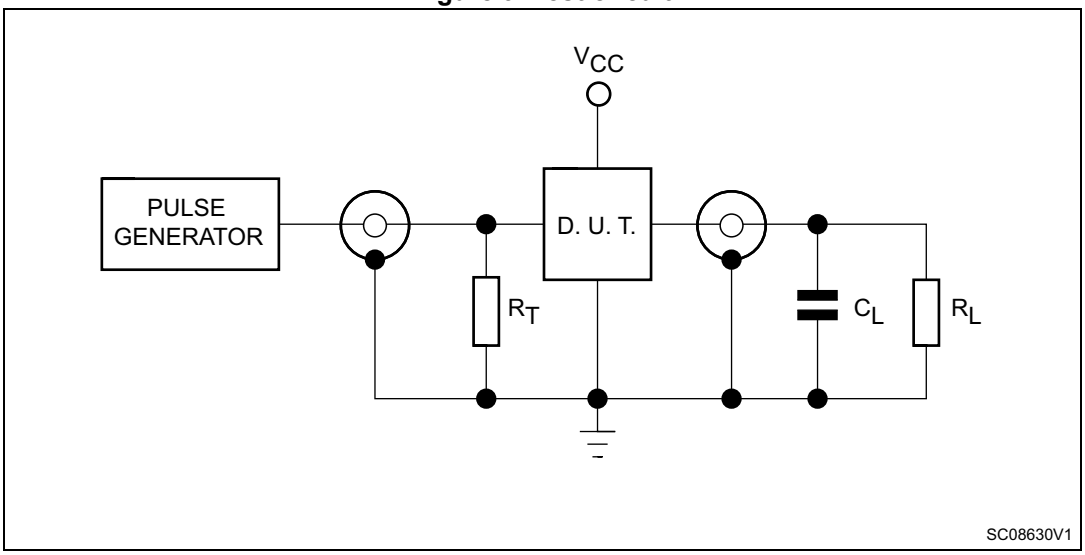



**Figure 9. Test circuit**




1. $C_L$ = 5/35 pF or equivalent (includes jig capacitance).
2. $R_L$ = 50 Ω or equivalent.
3. $R_T$ = $Z_{OUT}$ of pulse generator (typically 50 Ω).

**Figure 10. Break-before-make time delay**

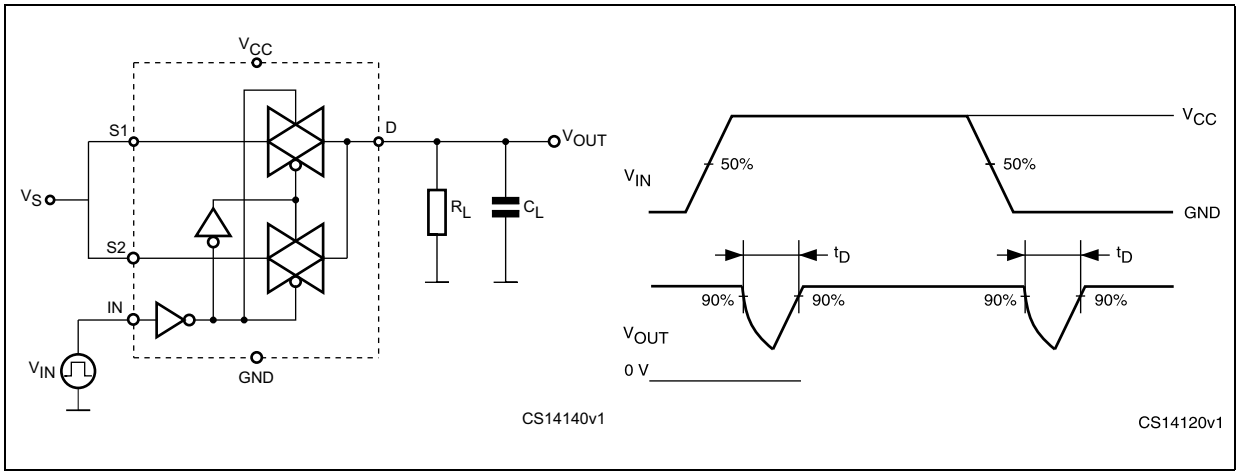



**Figure 11. Switching time and charge injection ($V_{GEN}$ = 0 V, $R_{GEN}$ = 0 Ω, $R_L$ = 1 MΩ, $C_L$ = 100 pF)**

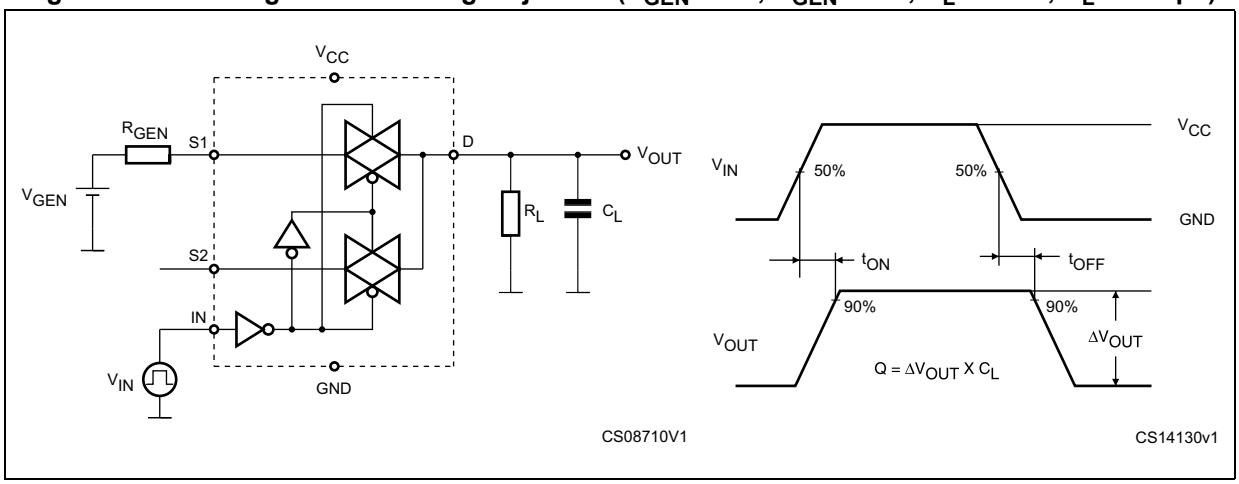
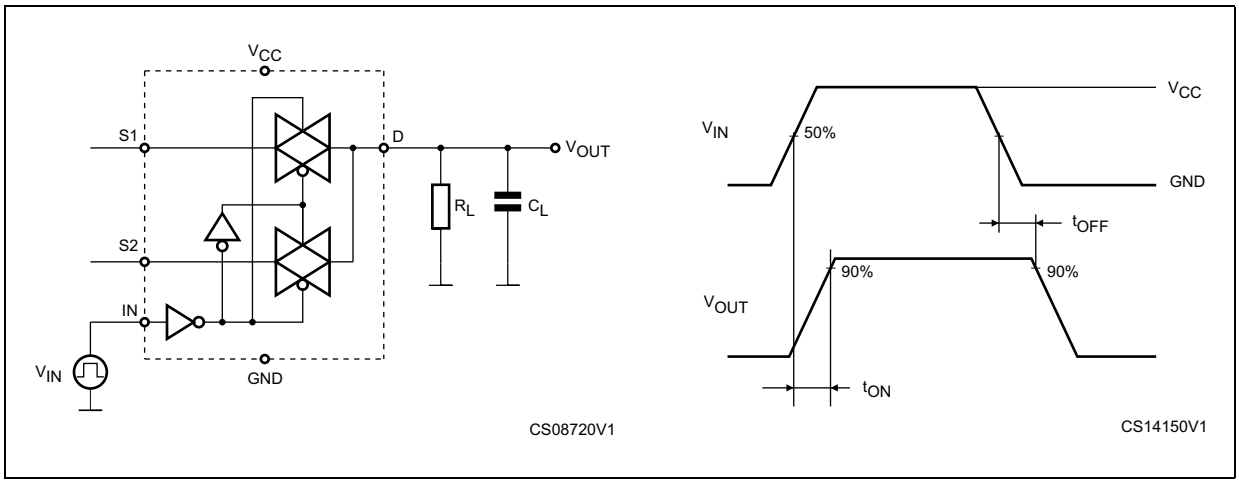


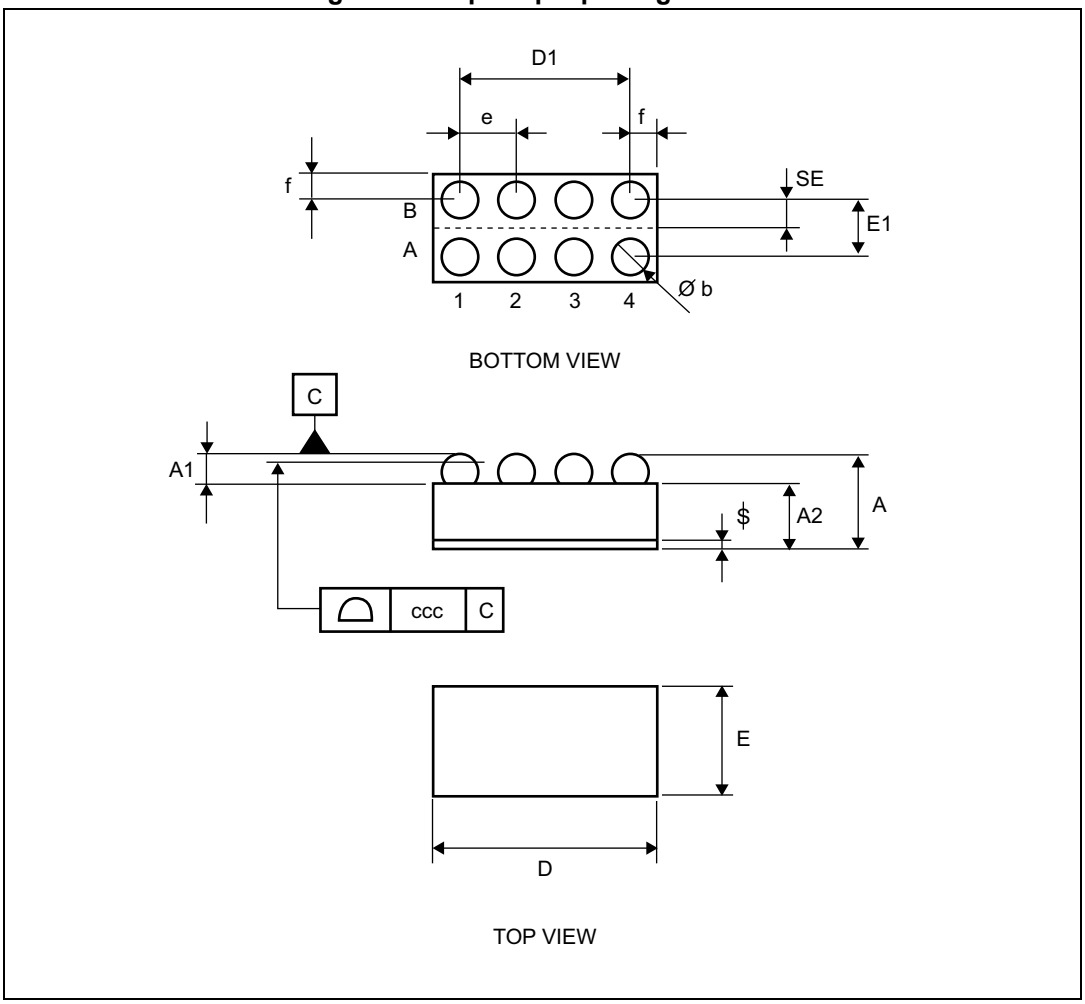

**Figure 12. Turn-on, turn-off delay time**



# 6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

**Figure 13. Flip Chip 8 package outline**




1. Drawing is not to scale.

Table 9. Flip Chip 8 mechanical data

| Symbol | Dimensions (mm) | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 0.535 | 0.58 | 0.625 |
| A1 | 0.18 | 0.205 | 0.23 |
| A2 | 0.355 | 0.375 | 0.395 |
| b | 0.215 | 0.255 | 0.295 |
| D | 1.85 | 1.9 | 1.95 |
| D1 | | 1.5 | |
| e | 0.45 | 0.5 | 0.55 |
| E | 0.85 | 0.9 | 0.95 |
| E1 | 0.45 | 0.5 | 0.55 |
| SE | | 0.25 | |
| f | 0.19 | 0.2 | 0.21 |
| ccc | | 0.08 | |

Figure 14. Flip Chip 8 footprint

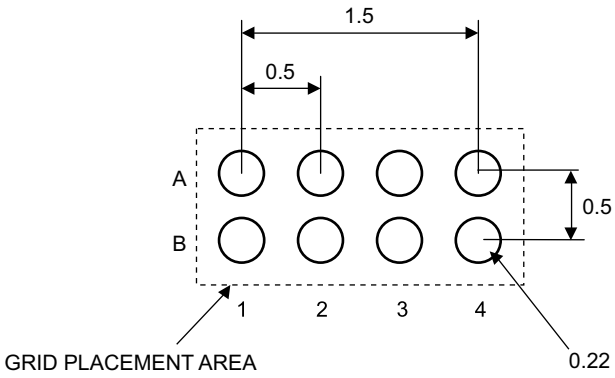


**Figure 15. Flip Chip 8 tape and reel**

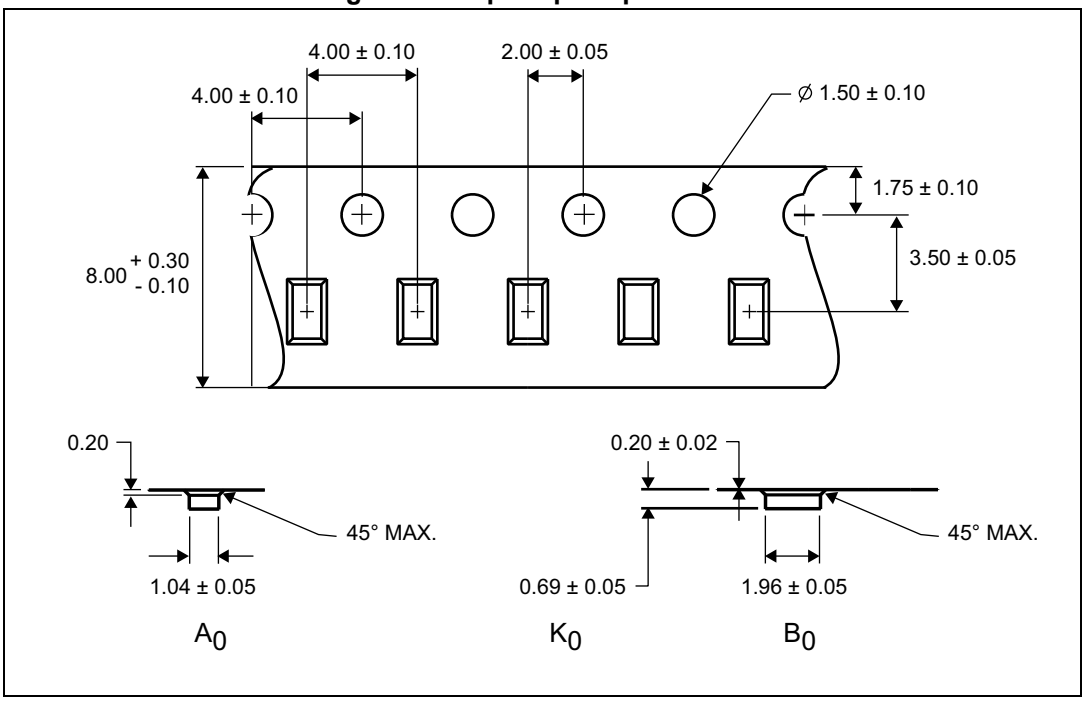



**Figure 16. Tape orientation**

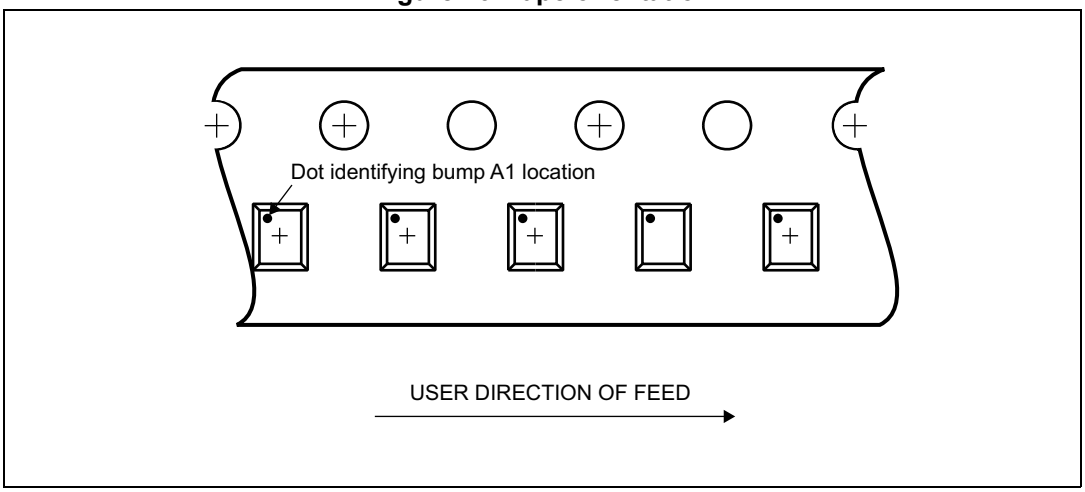
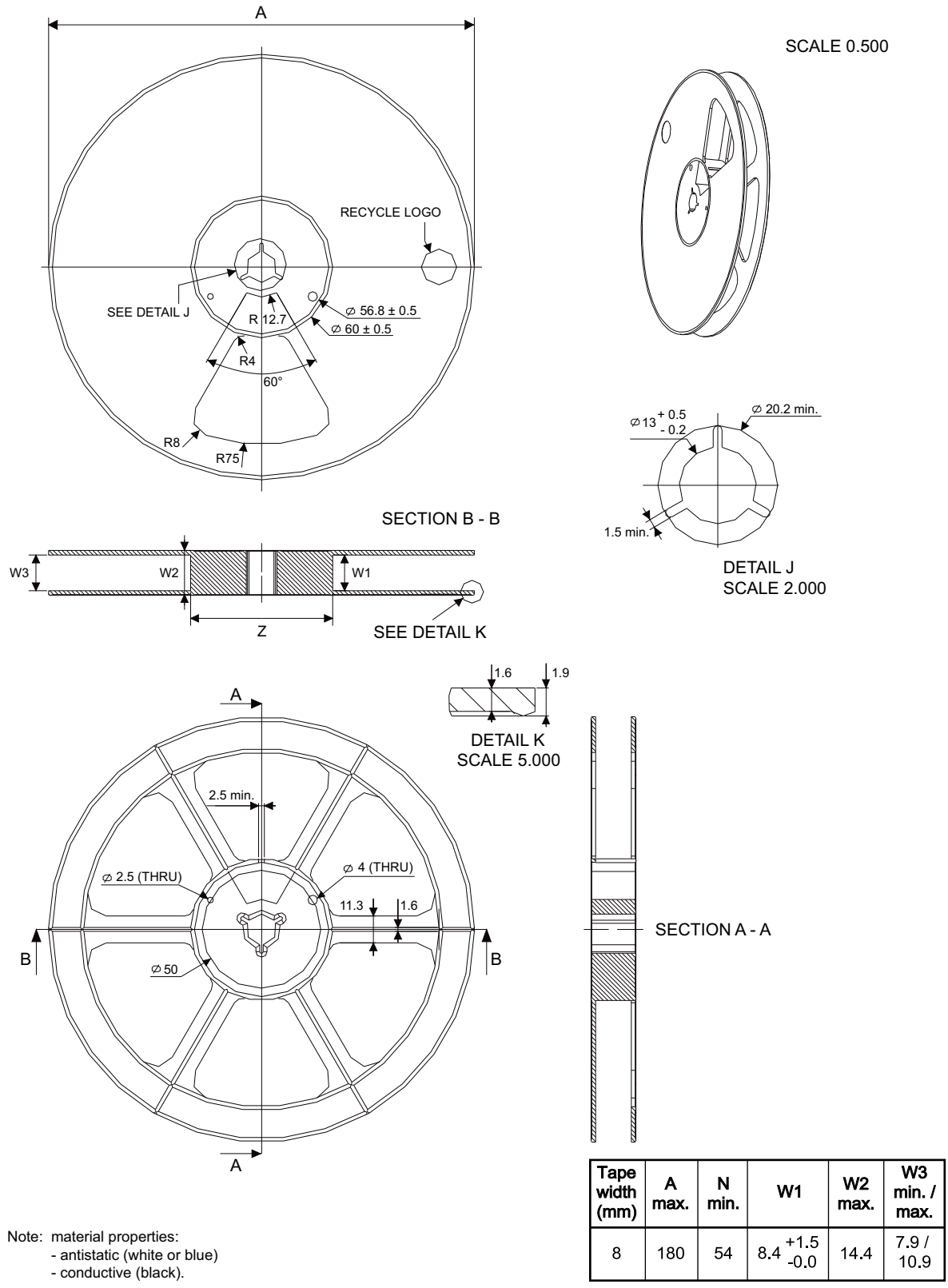


**Figure 17. Reel information**

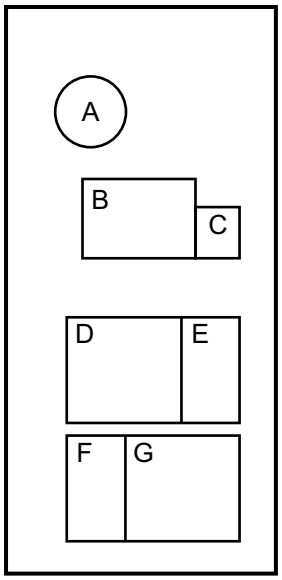



| Tape width (mm) | A max. | N min. | W1 | W2 max. | W3 min. / max. |
|---|---|---|---|---|---|
| 8 | 180 | 54 | 8.4 +1.5 -0.0 | 14.4 | 7.9 / 10.9 |

Note: material properties:
- antistatic (white or blue)
- conductive (black).

# 7 Package marking information

**Table 10. Device topside marking information**

| Marking composition: Flip Chip 8 | |
|---|---|
| **Package face: top** | **Legend** |
|  | ■ Unmarkable surface<br>☐ Marking composition field<br><br>A - 53312 - dot<br>B - 53313 - standard ST logo (0000093)<br>C - 53323 - ECO level<br>D - 53314 - marking area<br>E - 53318 - additional information (max. char. allowed = 1)<br>F - 53319 - Assembly year (Y)<br>G - 53322 - Assembly week (WW) |

# 8 Revision history

Table 11. Document revision history

| Date | Revision | Changes |
|---|---|---|
| 11-Sep-2008 | 1 | Initial release. |
| 19-Feb-2009 | 2 | Updated: $I_{ON}$ values in *Table 6: DC specifications*. |
| 15-May-2013 | 3 | Slightly redrawn *Figure 3* to *Figure 15* and *Figure 17*.<br>Updated *Figure 16* (added “Dot identifying bump A1 location”).<br>Updated *Section 3: Maximum ratings* (added cross-references).<br>Corrected units in *Table 8*.<br>Updated *Section 6: Package mechanical data* (updated ECOPACK text).<br>Added *Section 7: Package marking information*.<br>Minor corrections throughout document. |

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