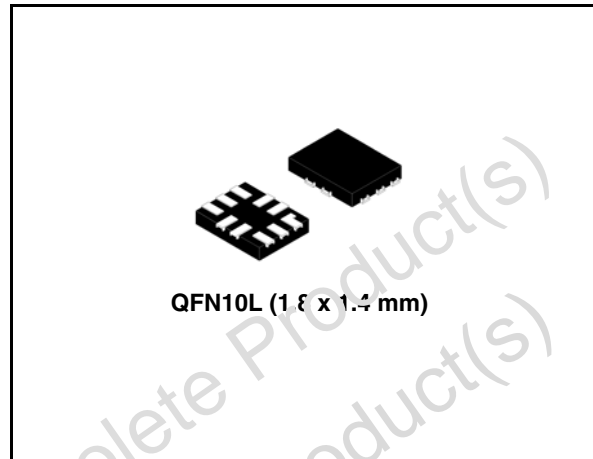


Low voltage 1 Ω dual SPST analog switch

Features

- Ultra low power dissipation:
 $I_{CC} = 0.2 \mu\text{A}$ (max.) at $T_A = 85 \text{ }^\circ\text{C}$
- $R_{PEAK} = 1.30 \Omega$ max ($T_A = 25 \text{ }^\circ\text{C}$)
 at $V_{CC} = 4.3 \text{ V}$
- Wide operating voltage range:
 $V_{CC}(\text{opr}) = 1.65$ to 4.3 V single supply
- 4.3 V tolerant and 1.8 V compatible threshold
 on digital control input at $V_{CC} = 1.65$ to 4.3 V
- Typical bandwidth (-3 dB) at 58 MHz
- Latch-up performance exceeds 100 mA per
 JESD 78, Class II
- ESD performance exceeds JESD22
 2000-V human body model (A114-A)



Description

The STG4210 is a high-speed CMOS low voltage dual analog SPST (single pole single throw) switch fabricated in silicon gate C²MOS technology.

The STG4210 is designed to operate from 1.65 to 4.3 V , making this device ideal for portable applications. The SELn inputs are provided to control the switch operation. The switch S_n is “on” (connected to common ports D_n) when the SELn input is held high and “off” (high impedance state exists between the two ports) when SELn is held low.

Additional key features are fast switching speed and ultra low power consumption. All inputs and outputs are equipped with protection circuits against static discharge, giving them ESD immunity and transient excess voltage.

Table 1. Device summary

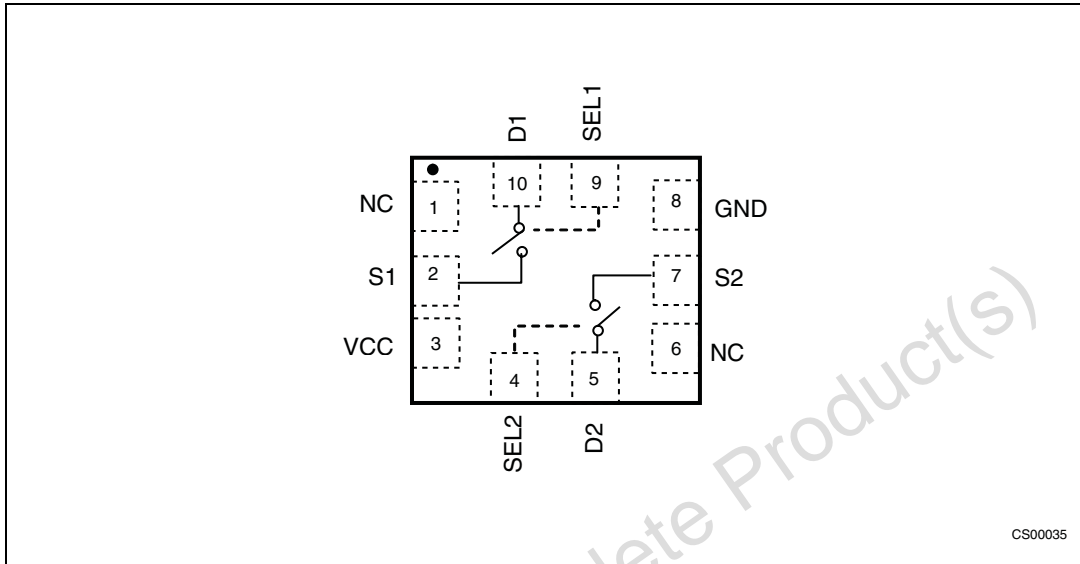
Order code	Package	Packaging
STG4210QTR	QFN10L (1.8 x 1.4 mm)	Tape and reel

Table of contents

1	Pin settings	3
2	Logic diagram	4
3	Maximum rating	5
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4	Electrical characteristics	7
5	Test circuit	10
6	Application diagram	14
7	Package mechanical data	15
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1 Pin settings

Figure 1. Pin connection (top through view)



CS00035

Table 2. Pin description

Pin number	Symbol	Name and function
1	NC	No connection
2	S1	Independent channel
3	V _{CC}	Positive supply voltage
4	SEL2	Selection control
5	D2	Common channel
6	NC	No connection
7	S2	Independent channel
8	GND	Ground (0 V)
9	SEL1	Selection control
10	D1	Common channel

2 Logic diagram

Figure 2. Logic block diagram

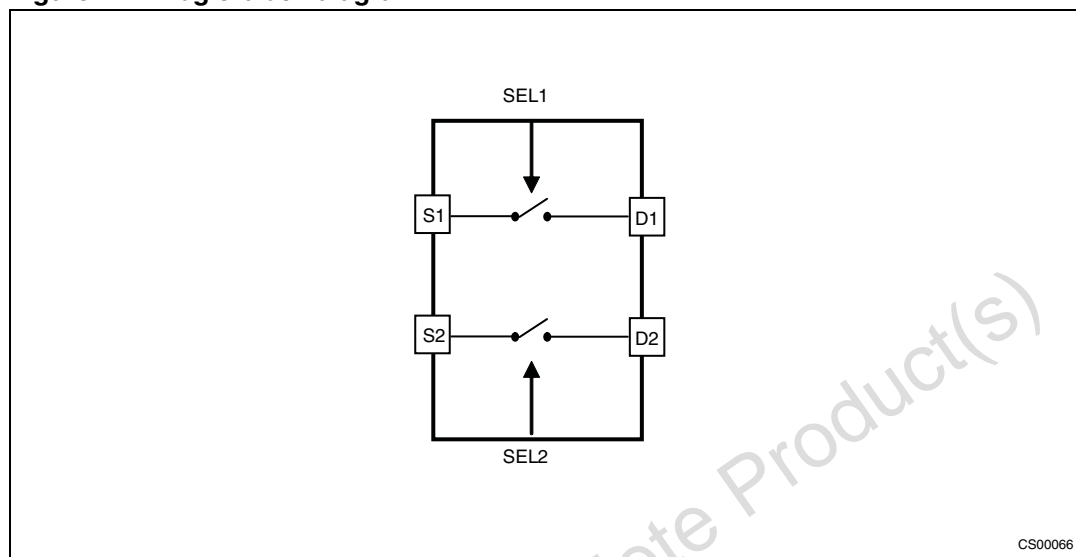


Table 3. Truth table

SELn	Switch Sn
L	OFF ⁽¹⁾
H	Sn is connected to Dn

1. High impedance

3 Maximum rating

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	-0.5 to 5.5	V
V_I	DC input voltage	-0.5 to $V_{CC} + 0.5$	V
V_{IC}	DC control input voltage	-0.5 to 5.5	V
V_O	DC output voltage	-0.5 to $V_{CC} + 0.5$	V
I_{IKC}	DC input diode current on control pin ($V_{SEL} < 0$ V)	-50	mA
I_{IK}	DC input diode current ($V_{SEL} < 0$ V)	± 50	mA
I_{OK}	DC output diode current	± 20	mA
I_O	DC output current	± 300	mA
I_{OP}	DC output current peak (pulse at 1 ms, 10% duty cycle)	± 500	mA
I_{CC} or I_{GND}	DC V_{CC} or ground current	± 100	mA
P_D	Power dissipation at $T_A=70$ °C ⁽¹⁾	1120	mW
T_{STG}	Storage temperature	-65 to 150	°C
T_L	Lead temperature (10 sec)	300	°C

1. Derate above 70 °C by 18.5 mW/°C

3.1 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter		Value	Unit
V_{CC}	Supply voltage		1.65 to 4.3	V
V_I	Input voltage		0 to V_{CC}	V
V_{IC}	Control input voltage		0 to 4.3	V
V_O	Output voltage		0 to V_{CC}	V
T_{op}	Operating temperature		-40 to 85	°C
dt/dv	Input rise and fall time control input	$V_{CC} = 1.65\text{ V to }2.7\text{ V}$	0 to 20	ns/V
		$V_{CC} = 3.0\text{ V to }4.3\text{ V}$	0 to 10	

4 Electrical characteristics

Table 6. DC specifications

Symbol	Parameter	V _{CC} (V)	Test condition	Value					Unit
				T _A = 25 °C			-40 to 85 °C		
				Min	Typ	Max	Min	Max	
V _{IH}	High level input voltage	1.65 – 1.95		0.65 V _{CC}			0.65 V _{CC}		V
		2.3 – 2.5		1.2			1.2		
		2.7 – 3.0		1.3			1.3		
		3.0 – 3.6		1.4			1.4		
		4.3		1.5			1.5		
V _{IL}	Low level input voltage	1.65 – 1.95				0.25		0.25	V
		2.3 – 2.5				0.25		0.25	
		2.7 – 3.0				0.25		0.25	
		3.0 – 3.6				0.30		0.30	
		4.3				0.40		0.40	
R _{PEAK}	Switch ON resistance	4.3	V _S = 0 V to V _{CC} I _S = 100 mA		1.10	1.3		1.5	Ω
		3.6			1.15	1.4		1.6	
		3.0			1.25	1.5		1.8	
		2.7			1.35	1.6		1.9	
		1.8			2.20	2.9		3.5	
R _{FLON}	ON resistance match (1)	4.3	V _S at R _{PEAK} I _S = 100 mA		10				mΩ
		3.6			14				
		3.0			14				
		2.7			15				
		1.8			30				
R _{FLAT}	ON resistance flatness (2)	4.3	V _S = 0 to V _{CC} I _S = 100 mA		0.45	0.50		0.55	Ω
		3.6			0.45	0.50		0.55	
		3.0			0.50	0.55		0.60	
		2.7			0.55	0.60		0.70	
		1.8			1.10	1.70		2.00	
I _{OFF}	OFF state leakage current (Sn), (Dn)	4.3	V _S = 0.3 or 4 V			±0.1		±1	μA
I _{SEL}	SEL leakage current	0 – 4.3	V _{SEL} = 0 to 4.3 V			±0.05		±1	μA

Table 6. DC specifications

Symbol	Parameter	V _{CC} (V)	Test condition	Value					Unit
				T _A = 25 °C			-40 to 85 °C		
				Min	Typ	Max	Min	Max	
I _{CC}	Quiescent supply current	1.65 –4.3	V _{SEL} = V _{CC} or GND			±0.05		±0.2	µA
I _{CCLV}	Quiescent supply current low voltage driving	4.3	V _{SEL} = 1.65 V		±37	±50		±100	µA
			V _{SEL} = 1.80 V		±33	±40		±50	
			V _{SEL} = 2.60 V		±12	±20		±30	

1. $\Delta R_{ON} = R_{ON(max)} - R_{ON(min)}$.
2. Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.

Table 7. AC electrical characteristics (C_L = 35 pF, R_L = 50 Ω, t_r = t_f ≤ ns)

Symbol	Parameter	V _{CC} (V)	Test condition	Value					Unit
				T _A = 25 °C			-40 to 85 °C		
				Min	Typ	Max	Min	Max	
t _{PLH} , t _{PHL}	Propagation delay	1.65 –1.95		0.45					ns
		2.3 –2.7		0.45					
		3.0 –3.3		0.30					
		3.6 –4.3		0.30					
t _{ON}	Turn-ON time	1.65 –1.95	V _S = 0.8 V	120				ns	
		2.3 –2.7	V _S = 1.5 V	65	85		90		
		3.0 –3.3		42	55		65		
		3.6 –4.3		40	55		65		
t _{OFF}	Turn-OFF time	1.65 –1.95	V _S = 0.8 V	45				ns	
		2.3 –2.7	V _S = 1.5 V	18	30		40		
		3.0 –3.3		16	30		40		
		3.6 –4.3		15	30		40		
Q	Charge injection	1.65 –1.95	C _L = 100 pF R _L = 1 MΩ V _{GEN} = 0 V R _{GEN} = 0 Ω	43				pC	
		2.3 –2.7		51					
		3.0 –3.3		51					
		3.6 –4.3		49					
OIRR	Off isolation ⁽¹⁾	1.65 –4.3	V _S = 1 V _{RMS} f = 100 KHz	-66					dB

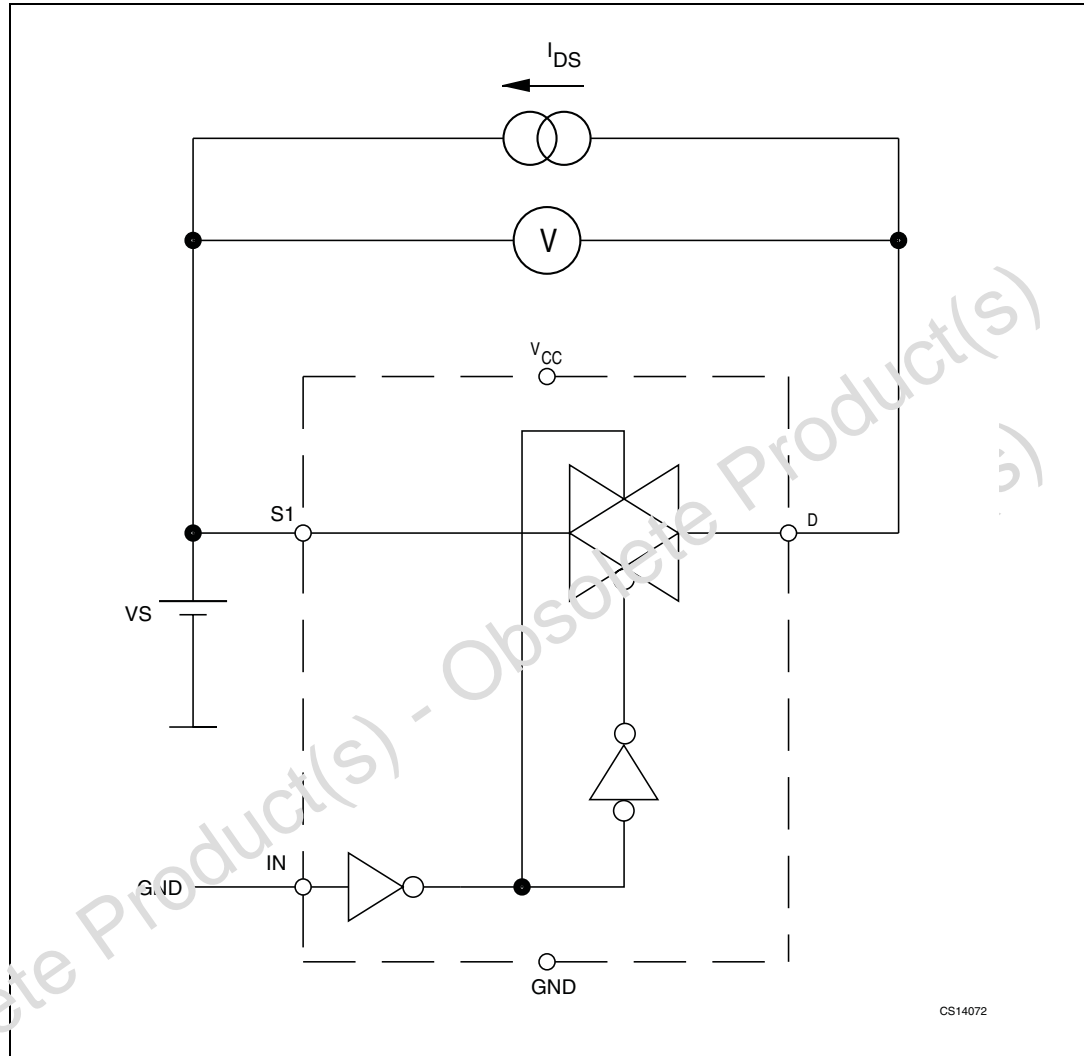
Table 7. AC electrical characteristics ($C_L = 35 \text{ pF}$, $R_L = 50 \text{ } \Omega$, $t_r = t_f \leq 5 \text{ ns}$)

Symbol	Parameter	V_{CC} (V)	Test condition	Value					Unit
				$T_A = 25 \text{ } ^\circ\text{C}$			$-40 \text{ to } 85 \text{ } ^\circ\text{C}$		
				Min	Typ	Max	Min	Max	
Xtalk	Crosstalk	1.65 –4.3	$V_S = 1 V_{RMS}$ $f = 100 \text{ KHz}$		-72				dB
THD	Total harmonic distortion	2.3 –4.3	$f = 20 \text{ Hz to } 20 \text{ kHz}$ $R_L = 600 \text{ } \Omega$ $C_L = 50 \text{ pF}$ $V_{IN} = 2 V_{P-P}$ $V_{DC} = V_{CC}/2$		0.01				%
BW	-3dB bandwidth	1.65 –4.3	$R_L = 50 \text{ } \Omega$ Signal = 0 dBm		58				MHz
C_{SEL}	Control pin input capacitance		$V_{CC} = 0 \text{ V}$		9				pF
C_{ON}	Port capacitance when switch is enabled	3.3	$f = 1 \text{ MHz}$		113				
C_{OFF}	Port capacitance when switch is disabled	3.3	$f = 1 \text{ MHz}$		85				

1. Off isolation = $20 \text{ Log}_{10} (v_D/V_S)$, V_D = output, V_S = input at off switch

5 Test circuit

Figure 3. ON resistance



CS14072

Figure 4. OFF leakage

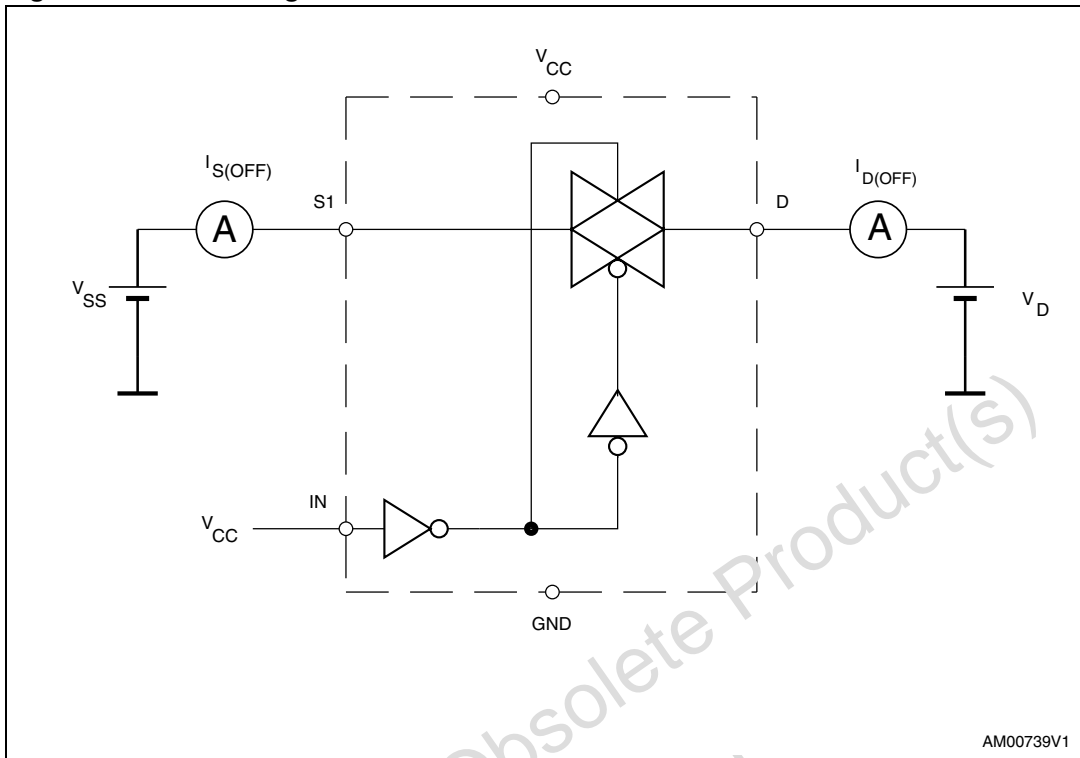


Figure 5. OFF isolation

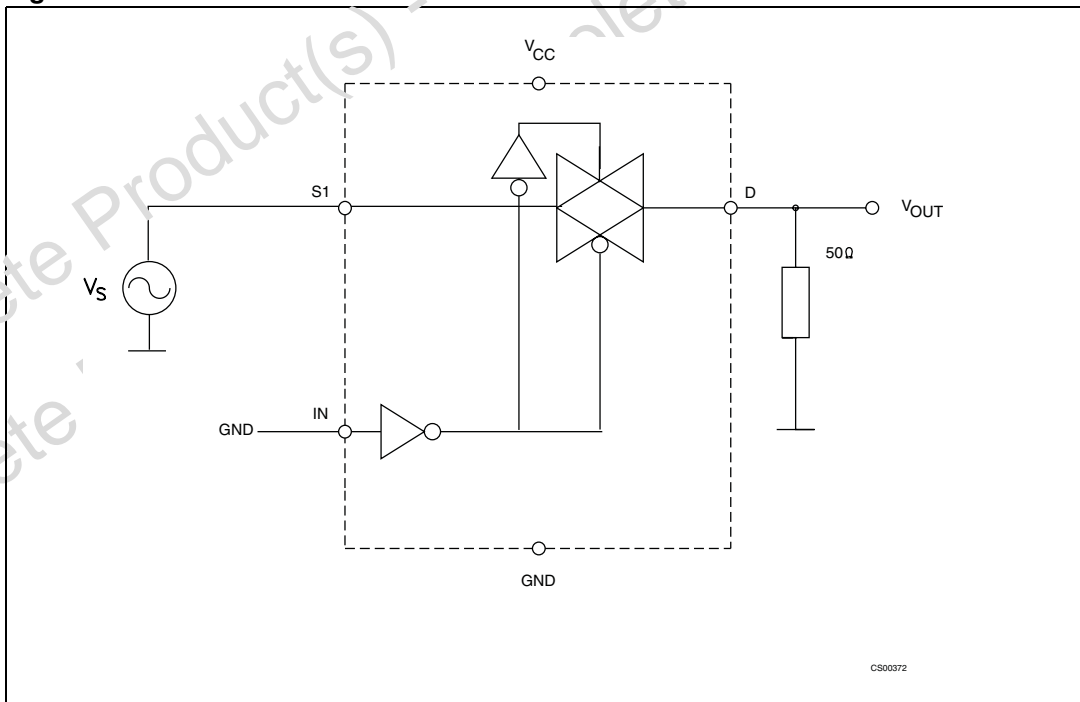


Figure 6. Bandwidth

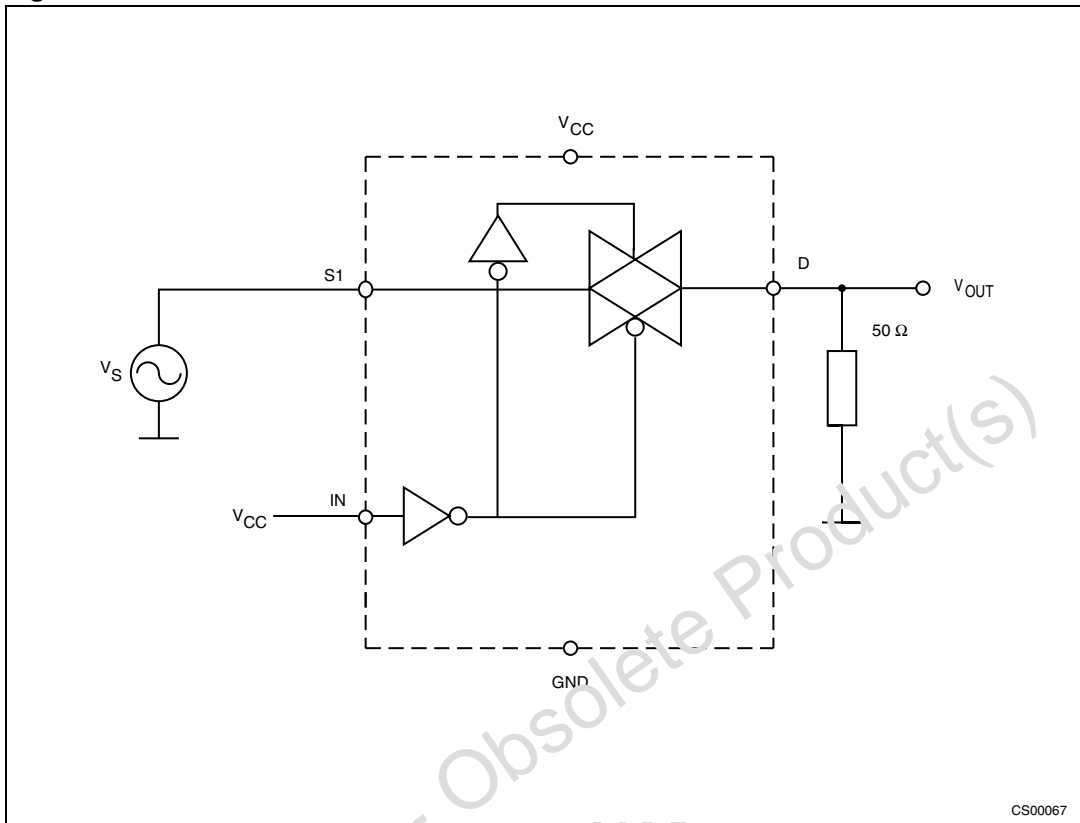


Figure 7. Switch-to-switch crosstalk

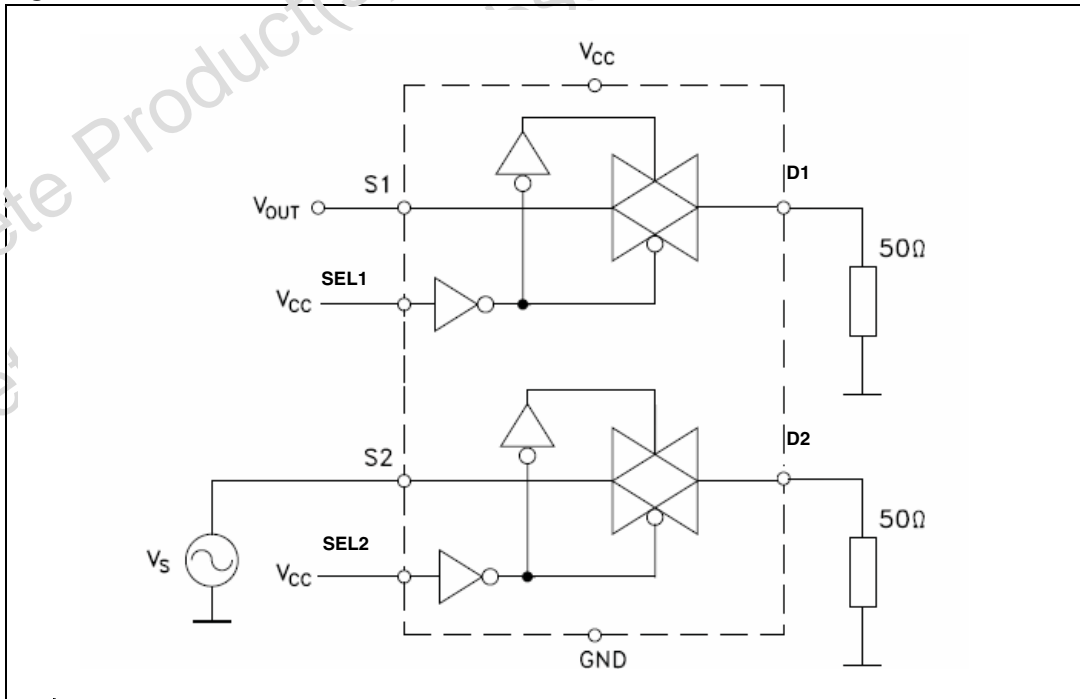
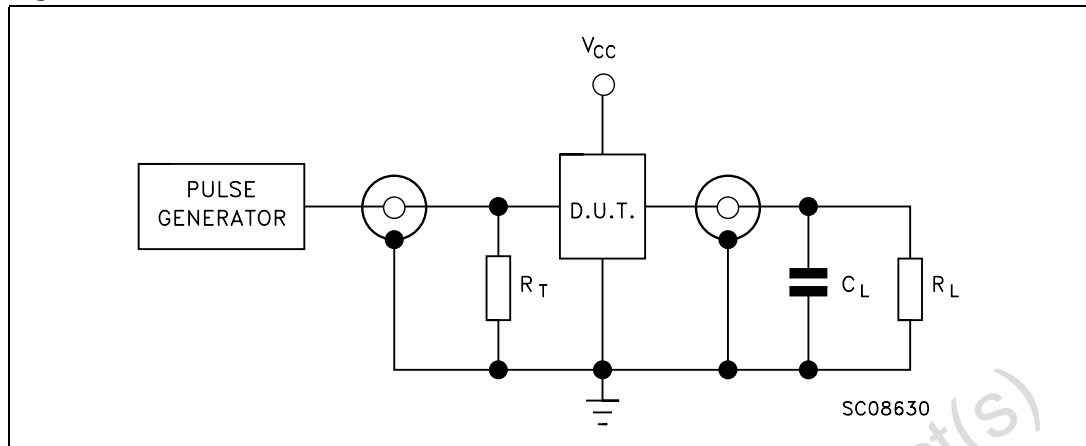


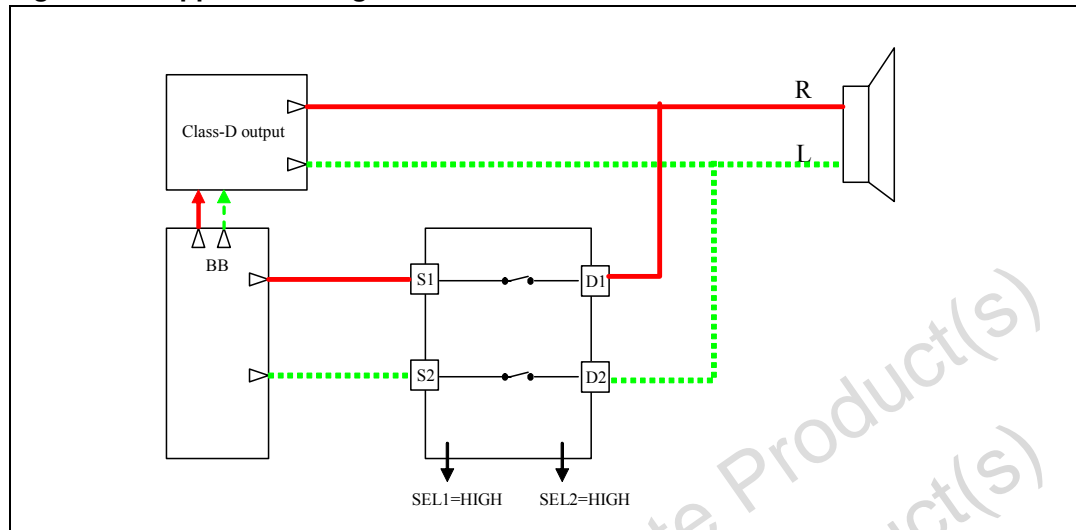
Figure 8. Test circuit



1. $C_L = 5/35$ pF or equivalent (includes jig and probe capacitance)
2. $R_L = 50 \Omega$ or equivalent
3. $R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

6 Application diagram

Figure 9. Application diagram



Obsolete Product(s) - Obsolete Product(s)
Obsolete Product(s) - Obsolete Product(s)

7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK[®] packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 10. QFN10L (1.8 x 1.4 mm) package outline

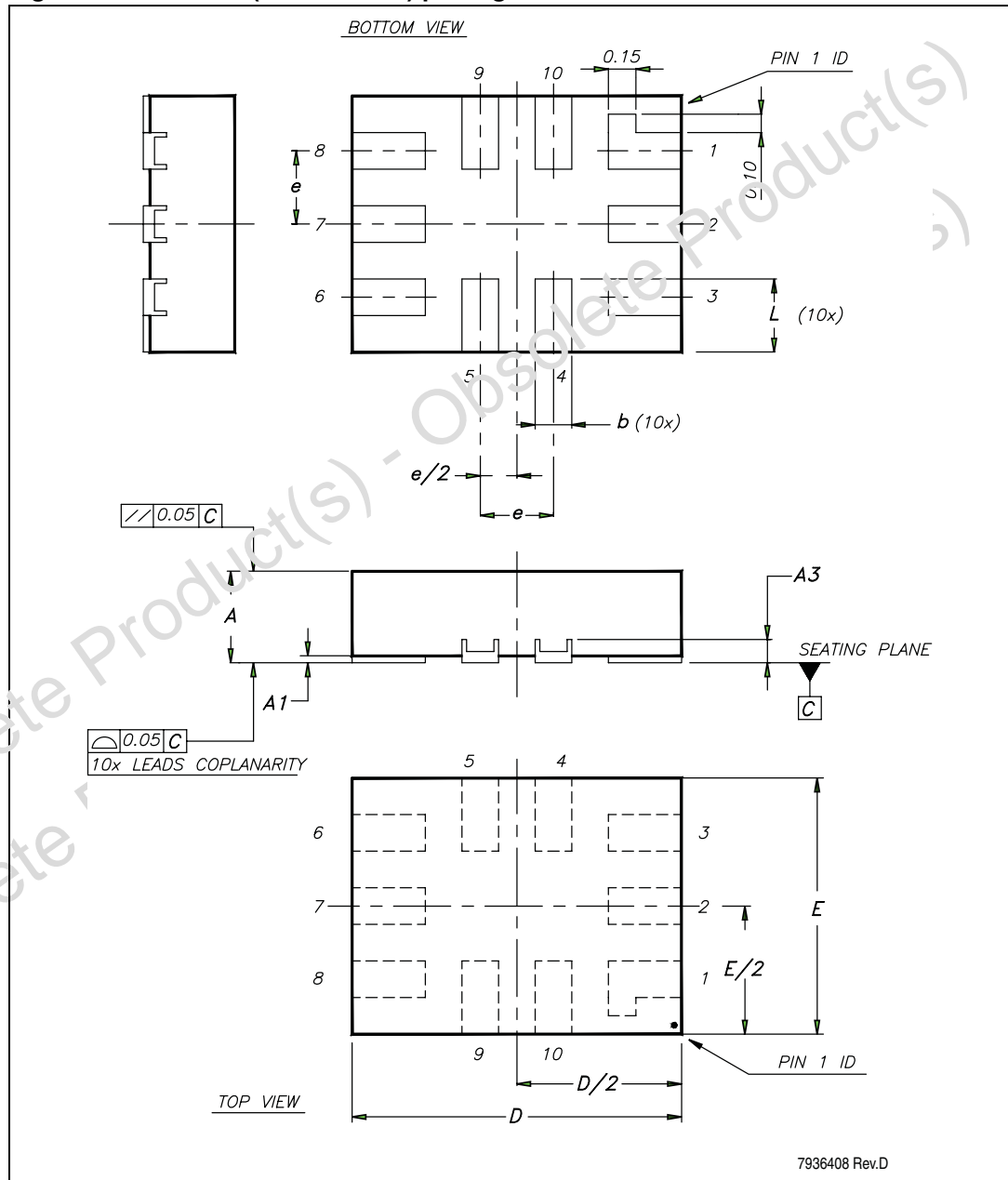


Table 2. QFN10L(1.8 x 1.4 mm) mechanical data

Symbol	Millimeters		
	Min	Typ	Max
A	0.45	0.50	0.55
A1	0	0.02	0.05
A3		0.127	
b	0.15	0.20	0.25
D	1.75	1.80	1.85
E	1.35	1.40	1.45
e		0.40	
L	0.35	0.40	0.45

Obsolete Product(s) - Obsolete Product(s)
Obsolete Product(s) - Obsolete Product(s)

Figure 11. QFN10L (1.8 x 1.4 mm) footprint recommendations

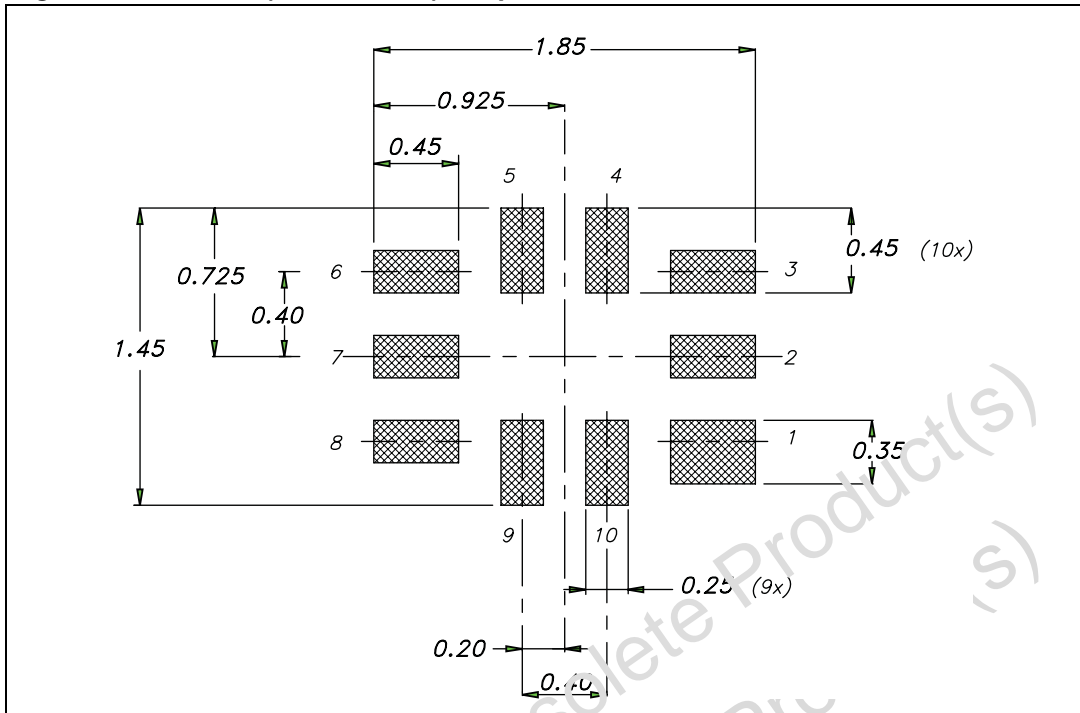


Figure 12. QFN10L (1.8 x 1.4 mm) carrier tape

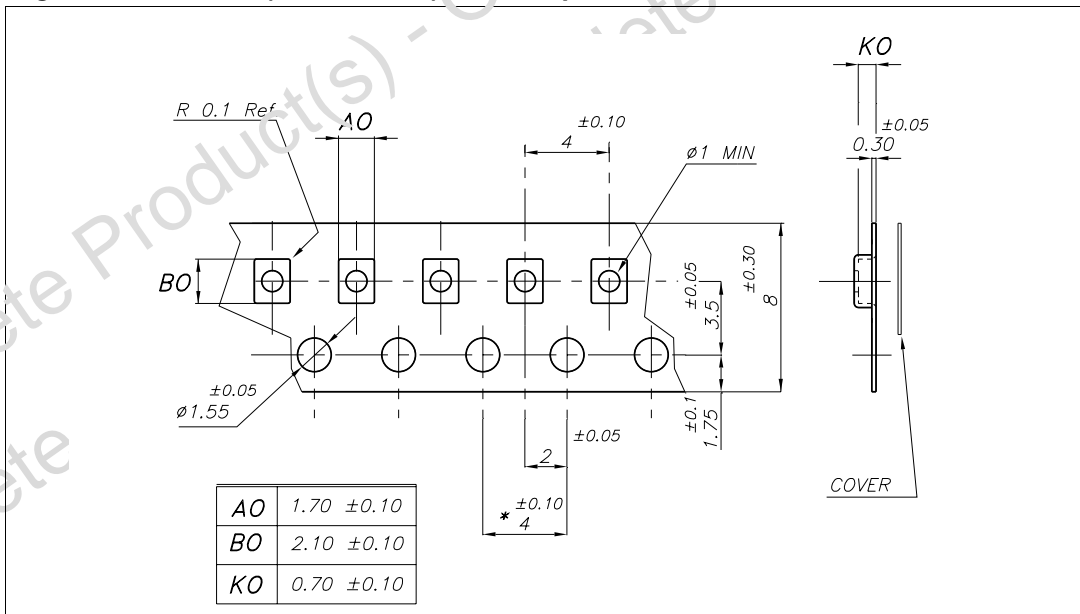


Figure 13. QFN10L (1.8 x 1.4 mm) reel information - front side

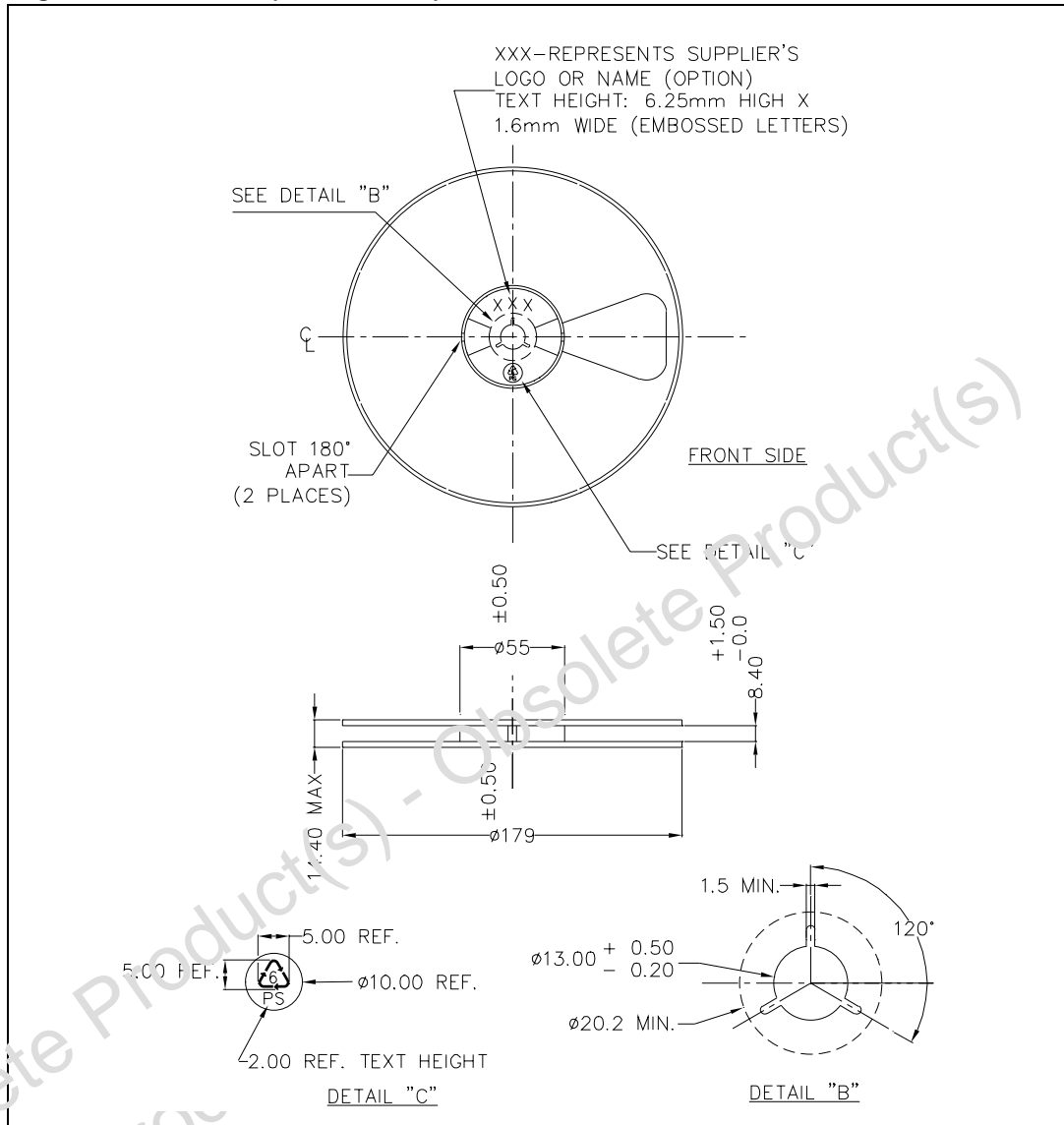
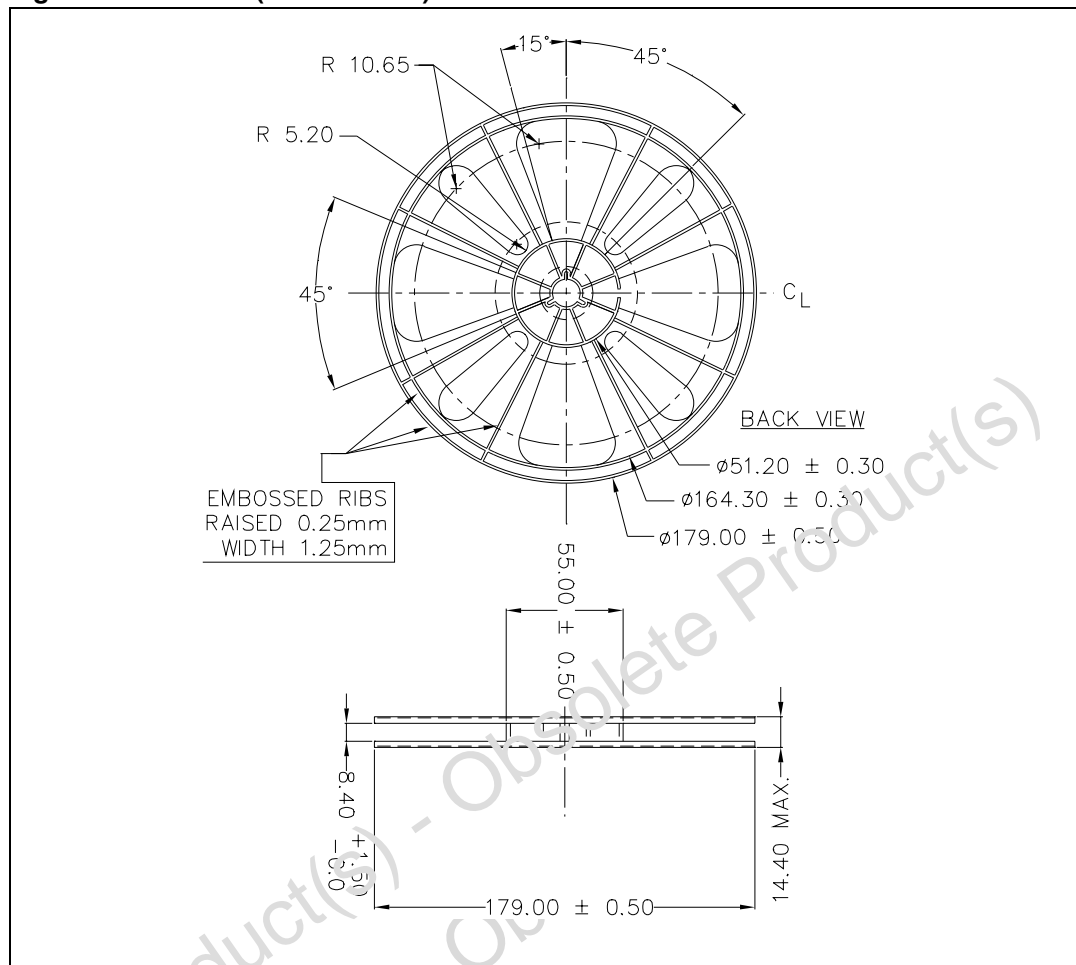


Figure 14. QFN10L(1.8 x 1.4 mm) reel information



8 Revision history

Table 8. Document revision history

Date	Revision	Changes
26-Aug-2008	1	Initial release.

Obsolete Product(s) - Obsolete Product(s)
Obsolete Product(s) - Obsolete Product(s)

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