



# STGF7NB60SL

N-CHANNEL 7A - 600V - TO-220FP

PowerMESH™ IGBT

**Table 1: General Features**

TYPE	V <sub>CES</sub>	V <sub>CE(sat)</sub> (Max) @25°C	I <sub>C</sub> @100°C
STGF7NB60SL	600 V	< 1.6 V	7 A

- POLYSILICON GATE VOLTAGE DRIVEN
- LOW THRESHOLD VOLTAGE
- LOW ON-VOLTAGE DROP
- LOW GATE CHARGE
- HIGH CURRENT CAPABILITY

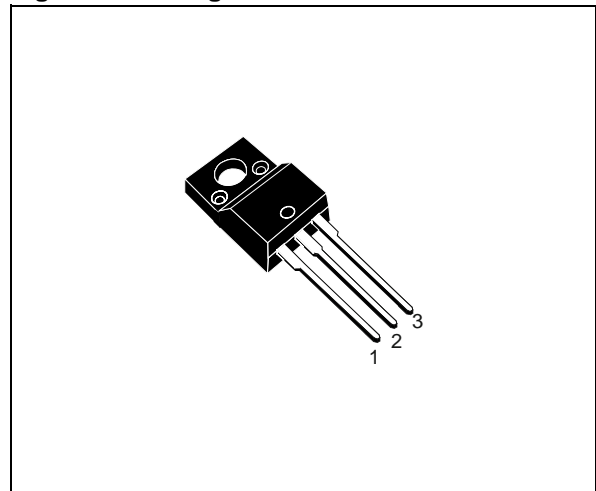
### DESCRIPTION

Using the latest high voltage technology based on a patented strip layout, STMicroelectronics has designed an advanced family of IGBTs, the PowerMESH™ IGBTs, with outstanding performances. The suffix "S" identifies a family optimized achieve minimum on-voltage drop for low frequency applications (<1kHz).

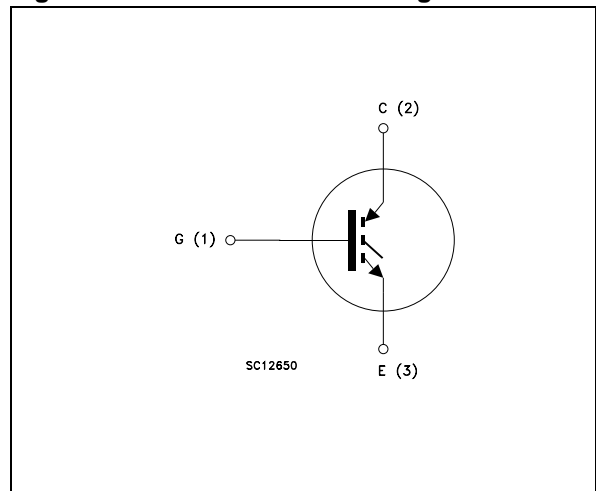
### APPLICATIONS

- LIGHT DIMMER
- STATIC RELAYS

**Figure 1: Package**



**Figure 2: Internal Schematic Diagram**



**Table 2: Order Codes**

SALES TYPE	MARKING	PACKAGE	PACKAGING
STGF7NB60SL	GF7NB60SL	TO-220FP	TUBE

Rev.3

**Table 3: Absolute Maximum ratings**

Symbol	Parameter	Value	Symbol
V <sub>CES</sub>	Collector-Emitter Voltage (V <sub>GS</sub> = 0)	600	V
V <sub>ECR</sub>	Reverse Battery Protection	20	V
V <sub>GE</sub>	Gate-Emitter Voltage	± 20	V
I <sub>C</sub>	Collector Current (continuous) at 25°C	15	A
I <sub>C</sub>	Collector Current (continuous) at 100°C	7	A
I <sub>CM</sub> (1)	Collector Current (pulsed)	20	A
P <sub>TOT</sub>	Total Dissipation at T <sub>C</sub> = 25°C	25	W
	Derating Factor	0.2	W/°C
V <sub>ISO</sub>	Insulation Withstand Voltage A.C.	2500	V
T <sub>stg</sub>	Storage Temperature	- 55 to 150	°C
T <sub>j</sub>	Operating Junction Temperature		

(1)Pulse width limited by max. junction temperature.

**Table 4: Thermal Data**

R <sub>thj-case</sub>	Thermal Resistance Junction-case Max	5	°C/W
R <sub>thj-amb</sub>	Thermal Resistance Junction-ambient Max	62.5	°C/W

**ELECTRICAL CHARACTERISTICS (T<sub>CASE</sub> =25°C UNLESS OTHERWISE SPECIFIED)**

**Table 5: Off**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>BR(CES)</sub>	Collectro-Emitter Breakdown Voltage	I <sub>C</sub> = 250 μA, V <sub>GE</sub> = 0	600			V
V <sub>BR(ECS)</sub>	Emitter-Collector Breakdown Voltage	I <sub>C</sub> = 1mA, V <sub>GE</sub> = 0	20			V
I <sub>CES</sub>	Collector-Emitter Leakage Current (V <sub>CE</sub> = 0)	V <sub>GE</sub> = Max Rating T <sub>C</sub> =25°C T <sub>C</sub> =125°C			10 100	μA μA
I <sub>GES</sub>	Gate-Emitter Leakage Current (V <sub>CE</sub> = 0)	V <sub>GE</sub> = ± 20 V , V <sub>CE</sub> = 0			±100	nA

**Table 6: On**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>GE(th)</sub>	Gate Threshold Voltage	V <sub>CE</sub> = V <sub>GE</sub> , I <sub>C</sub> = 250 μA	1.2		2.4	V
V <sub>CE(SAT)</sub>	Collector-Emitter Saturation Voltage	V <sub>GE</sub> =4.5 V, I <sub>C</sub> = 7A, T <sub>j</sub> = 25°C V <sub>GE</sub> =4.5 V, I <sub>C</sub> = 7A, T <sub>j</sub> = 125°C		1.2 1.1	1.6	V V

## ELECTRICAL CHARACTERISTICS (CONTINUED)

Table 7: Dynamic

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs}$	Forward Transconductance	$V_{CE} = 15 \text{ V}, I_C = 7 \text{ A}$		5		S
$C_{ies}$ $C_{oes}$ $C_{res}$	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{CE} = 25 \text{ V}, f = 1 \text{ MHz}, V_{GE} = 0$		800 60 10		pF pF pF
$Q_g$ $Q_{ge}$ $Q_{gc}$	Total Gate Charge Gate-Emitter Charge Gate-Collector Charge	$V_{CE} = 480 \text{ V}, I_C = 7 \text{ A},$ $V_{GE} = 5 \text{ V}$ (see Figure 20)		16 2.5 8.5	22	nC nC nC
$I_{CL}$	Turn-Off SOA Minimum Current	$V_{clamp} = 480 \text{ V}, T_j = 125^\circ\text{C}$ $R_G = 1 \text{ K}\Omega, V_{GE} = 5 \text{ V}$	20			A
tscw	Short Circuit Withstand Time	$V_{ce} = 0.5 V_{BR(CES)}, V_{GE} = 5 \text{ V},$ $T_j = 125^\circ\text{C}, R_G = 1 \text{ K}\Omega$		14		$\mu\text{s}$

Table 8: Switching On

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ $t_r$	Turn-on Delay Time Current Rise Time	$V_{CC} = 480 \text{ V}, I_C = 7 \text{ A}, R_G = 1 \text{ K}\Omega,$ $V_{GE} = 5 \text{ V}$ (see Figure 18)		1.1 0.25		$\mu\text{s}$ $\mu\text{s}$
$(di/dt)_{on}$ $E_{on}$	Turn-on Current Slope Turn-on Switching Losses	$V_{CC} = 480 \text{ V}, I_C = 7 \text{ A}, R_G = 1 \text{ K}\Omega$ $V_{GE} = 5 \text{ V}, T_j = 125^\circ\text{C}$		45 2.7		A/ $\mu\text{s}$ mJ

Table 9: Switching Off

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_c$ $t_r(V_{off})$ $t_{d(off)}$ $t_f$ $E_{off(**)}$	Cross-over Time Off Voltage Rise Time Delay Time Current Fall Time Turn-off Switching Loss	$V_{CC} = 480 \text{ V}, I_C = 7 \text{ A},$ $R_{GE} = 1 \text{ K}\Omega, V_{GE} = 5 \text{ V}$ (see Figure 18)		2.7 1.6 5.2 1.1 4.1		$\mu\text{s}$ $\mu\text{s}$ $\mu\text{s}$ $\mu\text{s}$ mJ
$t_c$ $t_r(V_{off})$ $t_{d(off)}$ $t_f$ $E_{off(**)}$	Cross-over Time Off Voltage Rise Time Delay Time Fall Time Turn-off Switching Loss	$V_{CC} = 480 \text{ V}, I_C = 7 \text{ A},$ $R_{GE} = 1 \text{ K}\Omega, V_{GE} = 5 \text{ V}$ $T_j = 125^\circ\text{C}$ (see Figure 18)		4.4 2.4 6.4 1.7 7.1		$\mu\text{s}$ $\mu\text{s}$ $\mu\text{s}$ $\mu\text{s}$ mJ

(\*\*)Turn-off losses include also the tail of the collector current.

Figure 3: Output Characteristics

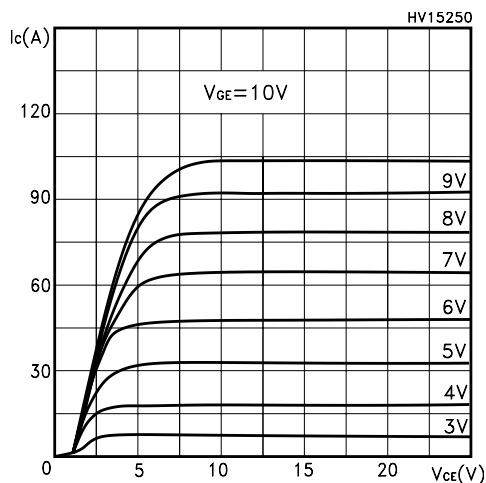


Figure 4: Transconductance

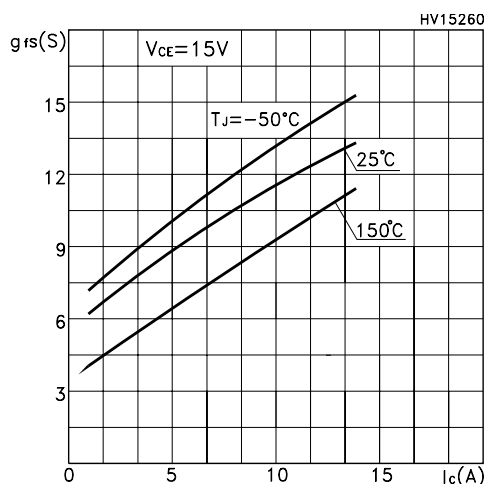


Figure 5: Collector-Emitter On Voltage vs Collector Current

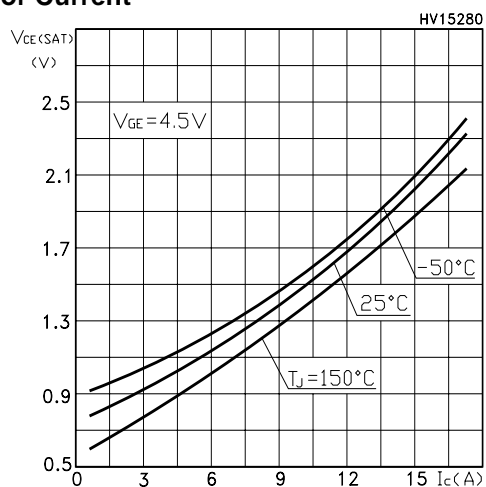


Figure 6: Transfer Characteristics

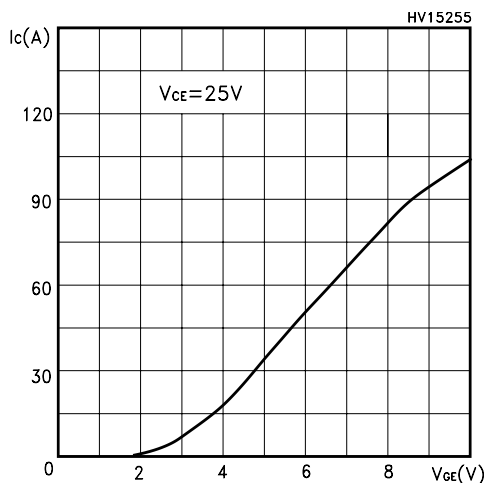


Figure 7: Collector-Emitter On Voltage vs Temperature

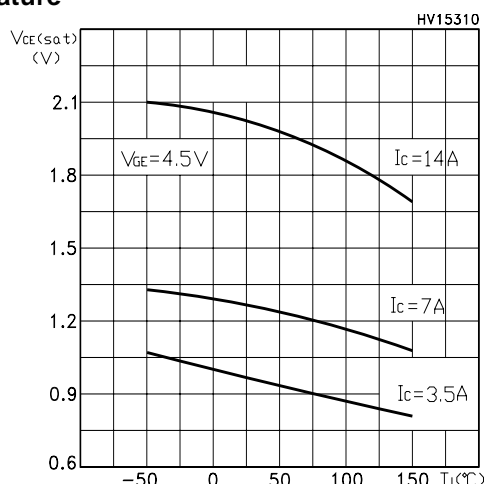


Figure 8: Normalized Collector-Emitter On Voltage vs Temperature

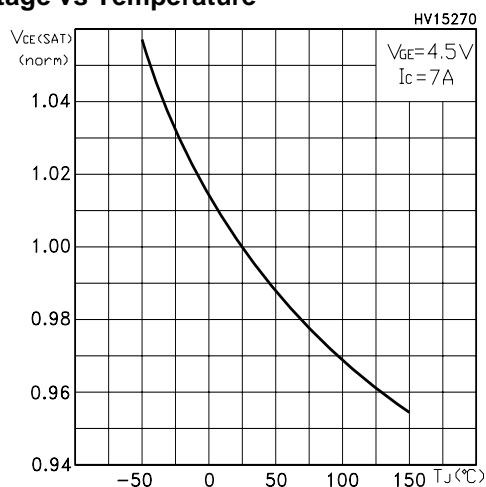


Figure 9: Gate Threshhold vs Temperature

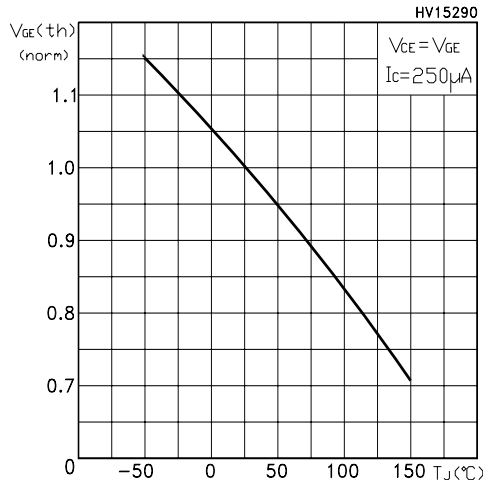


Figure 10: Capacitance Variations

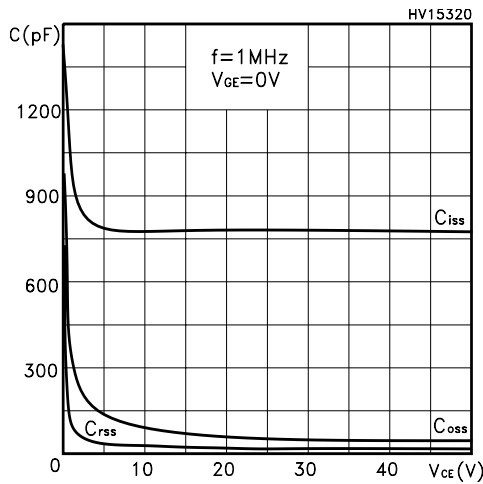


Figure 11: Total Switching Losses vs Gate Resistance

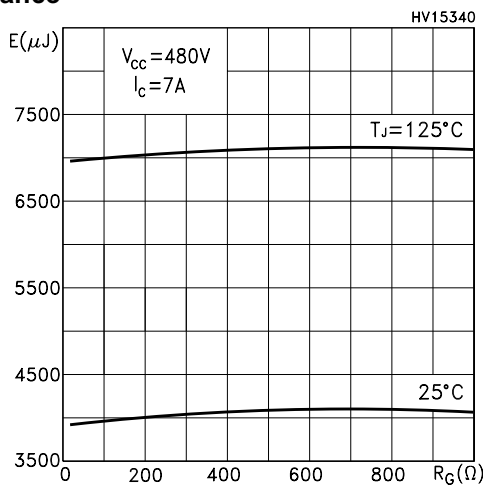


Figure 12: Normalized Breakdown Voltage vs Temperature

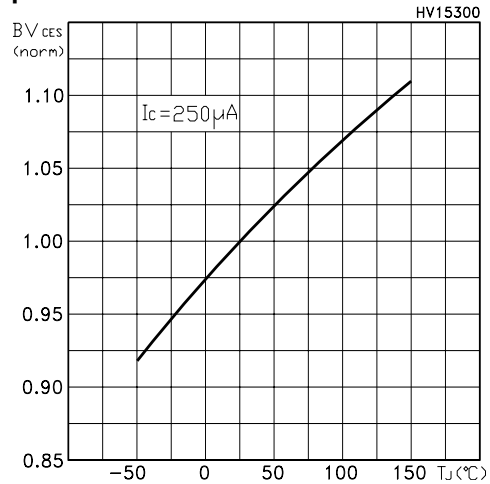


Figure 13: Gate Charge vs Gate-Emitter Voltage

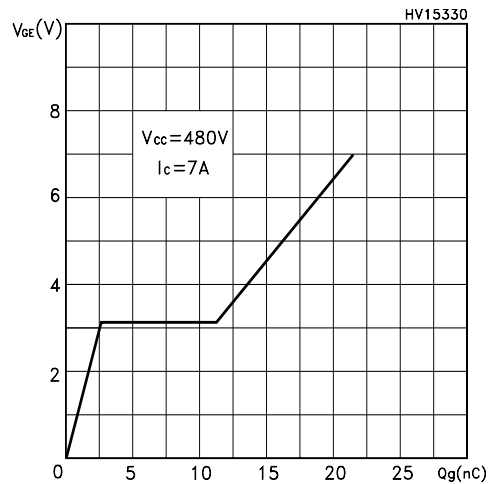


Figure 14: Total Switching Losses vs Temperature

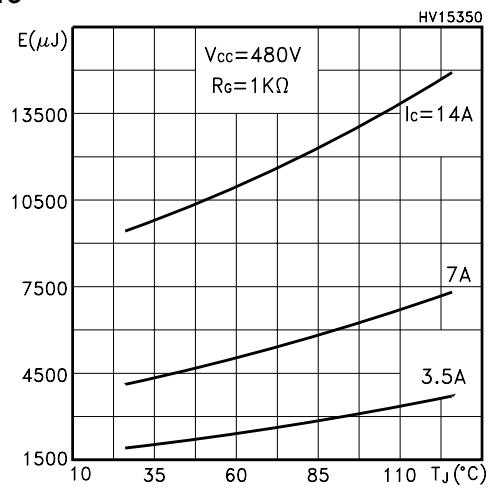


Figure 15: Total Switching Losses vs Collector Current

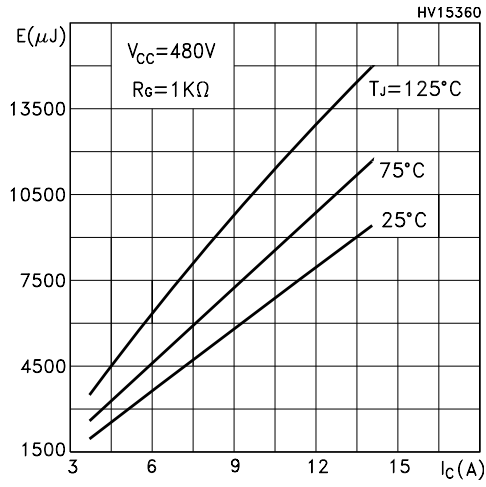


Figure 17: Turn-Off SOA

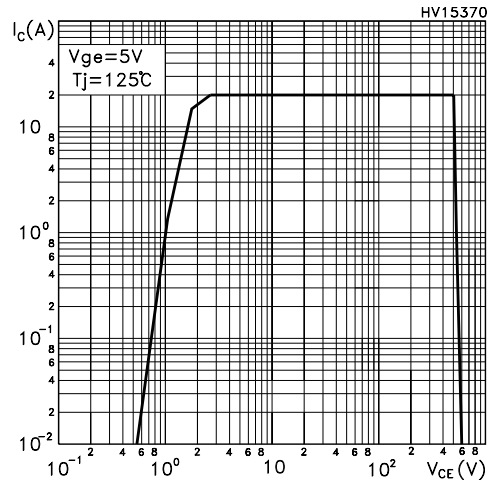


Figure 16: Thermal Impedance

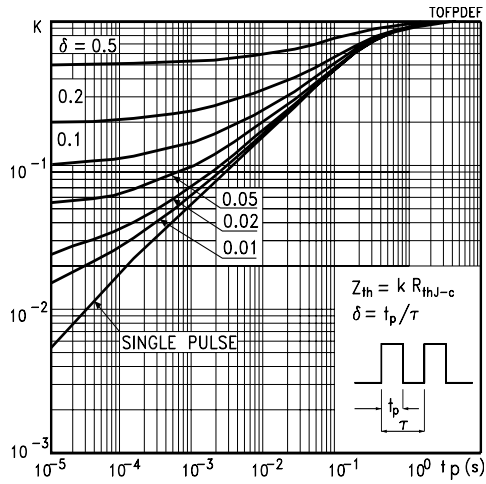


Figure 18: Test Circuit for Inductive Load Switching

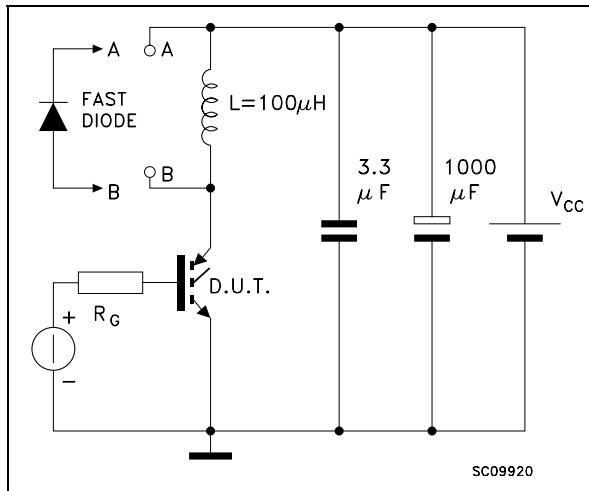


Figure 19: Switching Waveforms

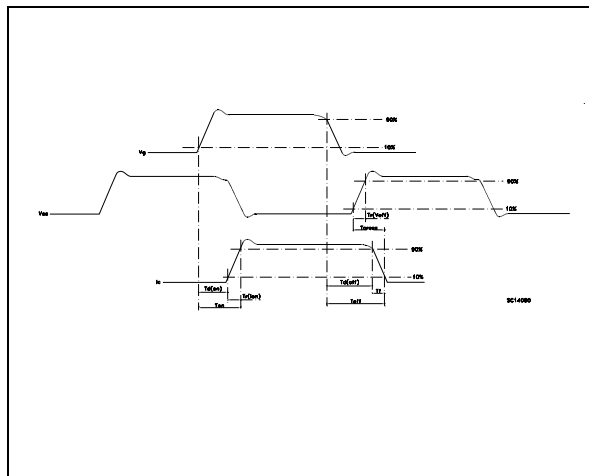
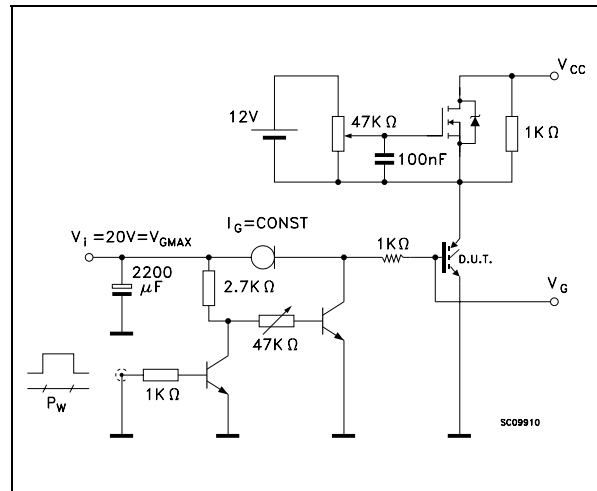


Figure 20: Gate Charge Test Circuit



**Table 10: Revision History**

<b>Date</b>	<b>Revision</b>	<b>Description of Changes</b>
04-June-2004	2	Stylesheet update. No content change
02-Sep-2004	3	Datasheet updated, see table1



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[IGW30N60H3FKSA1](#) [STGWA8M120DF3](#) [IGW08T120FKSA1](#) [IGW75N60H3FKSA1](#) [HGTG40N60B3](#) [FGH60N60SMD\\_F085](#)  
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