STH170N8F7-2

N-channel 80 V, 0.0028 Ω typ., 120 A, STripFET™ F7 Power MOSFET in a H²PAK-2 package

Datasheet — production data

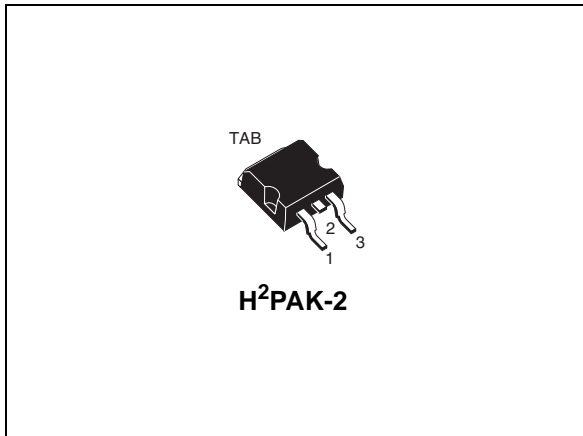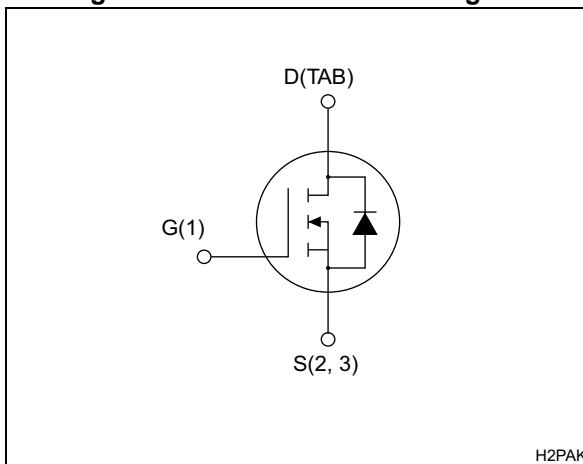
H²PAK-2

Figure 1. Internal schematic diagram

Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STH170N8F7-2	80 V	0.0037 Ω	120 A	250 W

- Among the lowest $R_{DS(on)}$ on the market
- Excellent figure of merit (FoM)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness

Applications

- Switching applications

Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Table 1. Device summary

Order code	Marking	Package	Packaging
STH170N8F7-2	170N8F7	H²PAK-2	Tape and reel

Contents

1   Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	80	V
V_{GS}	Gate-source voltage	± 20	V
I_D[1]	Drain current (continuous)	120	A
I_D[1]	Drain current (continuous) at T_C = 100 °C	120	A
I_{DM}	Drain current (pulsed)	480	A
P_{TOT}[1]	Total dissipation at T_C = 25 °C	250	W
T_J	Operating junction temperature	-55 to 175	°C
T_{stg}	Storage temperature		°C

1. Limited by package and rated according to $R_{thj\text{-}c}$.

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	0.6	°C/W
$R_{thj\text{-}pcb}$[1]	Thermal resistance junction-pcb	35	°C/W

1. When mounted on FR-4 board of 1 inch^2, 2oz Cu.

Table 4. Avalanche data

Symbol	Parameter	Value	Unit
I_{AV}	Not-repetitive avalanche current, (pulse width limited by T_{jmax})	35	A
E_{AS}	Single pulse avalanche energy (starting TJ = 25 °C, I_D = I_{AV}, V_{DD} = 50 V)	615	mJ

2   Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS}= 0, I_D = 250 µA	80			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0, V_{DS} = 80 V			1	µA
		V_{GS} = 0, V_{DS} = 80 V, T_C=125 °C			100	µA
I_{GSS}	Gate body leakage current	V_{DS} = 0, V_{GS} = +20 V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 250 µA	2.5		4.5	V
$R_{DS(on)}$	Static drain-source on- resistance	V_{GS}= 10 V, I_D= 60 A		0.0028	0.0037	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{GS}=0, V_{DS} =40 V, f=1 MHz,	-	8710	-	pF
C_{oss}	Output capacitance		-	1330	-	pF
C_{rss}	Reverse transfer capacitance		-	78	-	pF
Q_g	Total gate charge	V_{DD}=40 V, I_D = 120 A V_{GS} =10 V *Figure 14*	-	120	-	nC
Q_{gs}	Gate-source charge		-	43	-	nC
Q_{gd}	Gate-drain charge		-	26	-	nC

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD}= 40 V, I_D= 60 A, R_G= 4.7 Ω, V_{GS}= 10 V *Figure 13*	-	38	-	ns
t_r	Rise time		-	53	-	ns
$t_{d(off)}$	Turn-off delay time		-	79	-	ns
t_f	Fall time		-	37	-	ns

Table 8. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		120	A
I_{SDM}[1]	Source-drain current (pulsed)		-		480	A
V_{SD}[2]	Forward on voltage	I_{SD} = 120 A, V_{GS}=0	-		1.2	V
t_{rr}	Reverse recovery time	I_{SD} = 120 A, di/dt = 100 A/µs, V_{DD}= 64 V, T_j=150 °C	-	54		ns
Q_{rr}	Reverse recovery charge		-	78		nC
I_{RRM}	Reverse recovery current		-	2.9		A

1. Pulse width limited by safe operating area.

2. Pulsed: pulse duration=300 µs, duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area
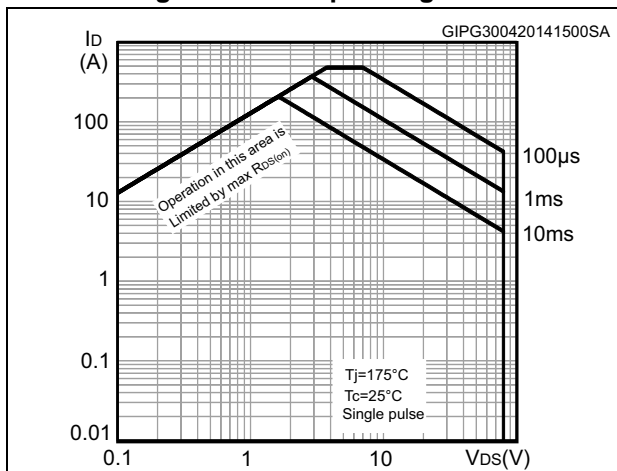
Figure 3. Thermal impedance

$$Z_{th} = k\ R_{thJ-c}$$
$$\delta = t_P/\tau$$
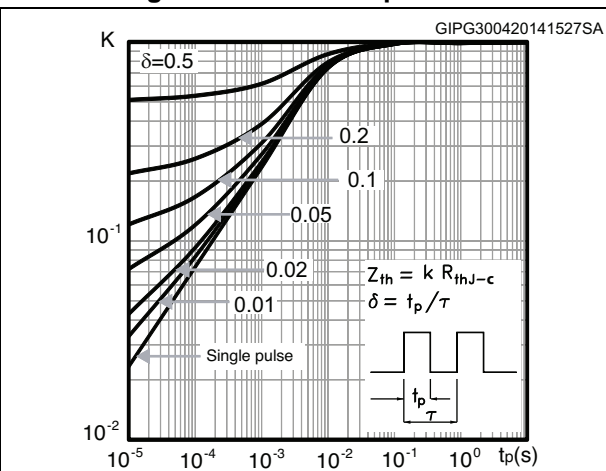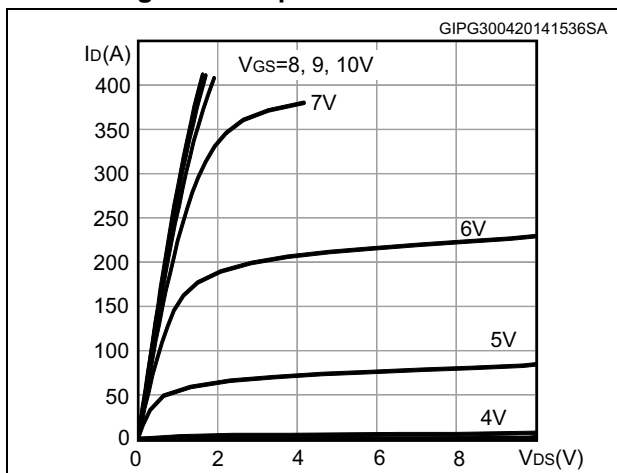
Figure 4. Output characteristics

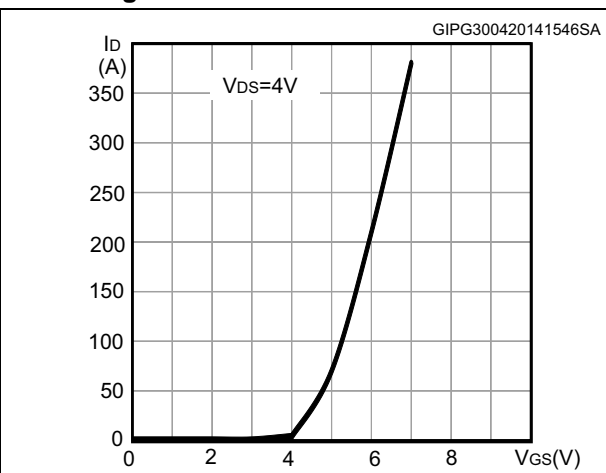**Figure 5. Transfer characteristics**

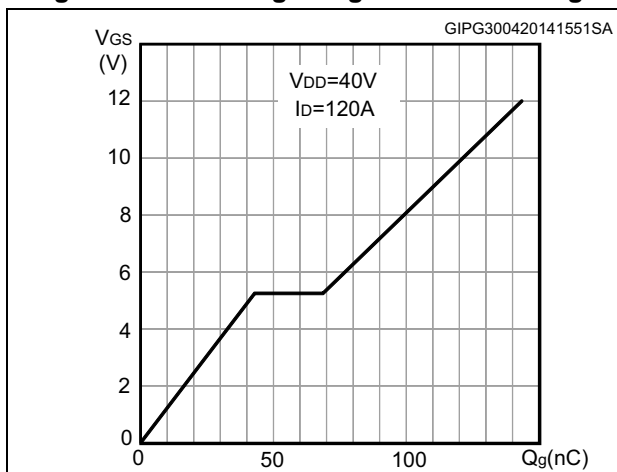
Figure 6. Gate charge vs gate-source voltage

Figure 7. Static drain-source on-resistance

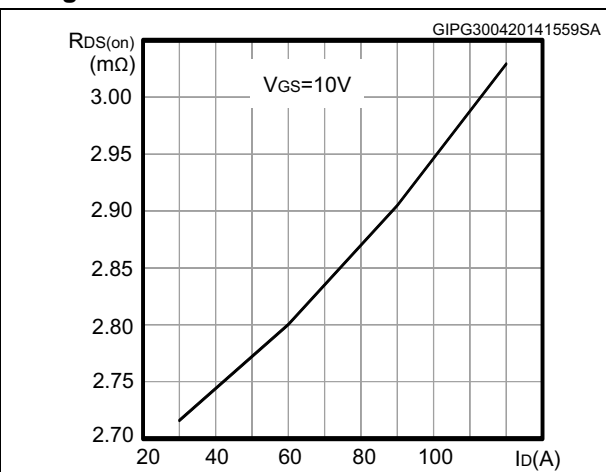**Figure 8. Capacitance variations**

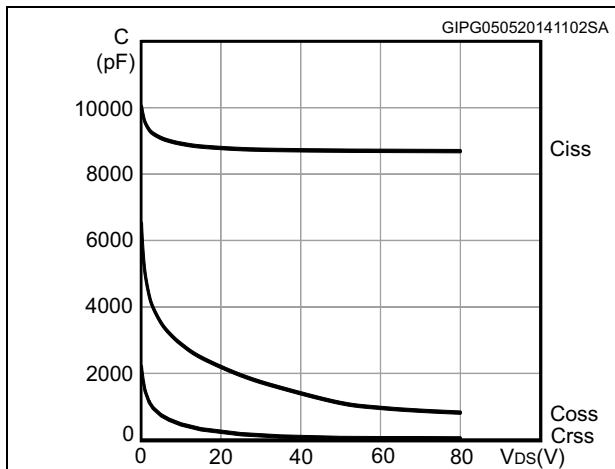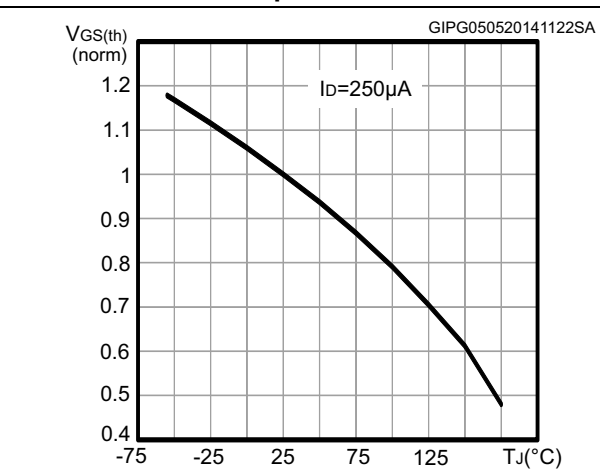**Figure 9. Normalized gate threshold voltage vs temperature**

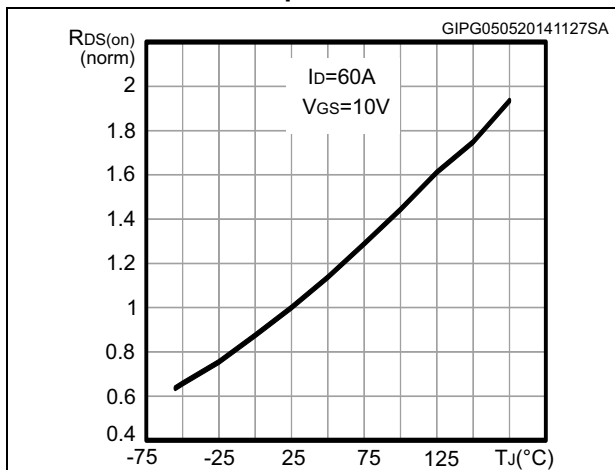**Figure 10. Normalized on-resistance vs temperature**

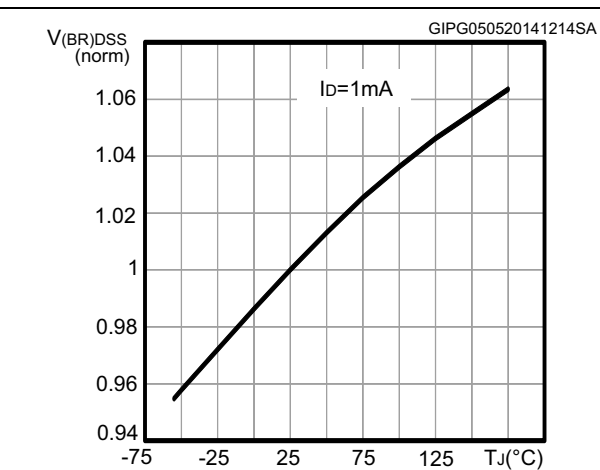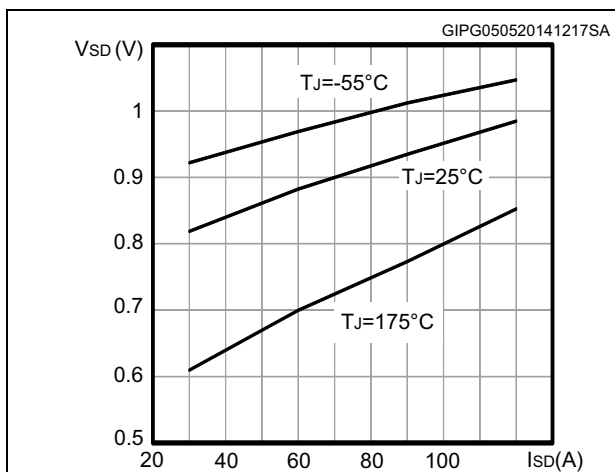**Figure 11. Normalized V(BR)DSS vs temperature**

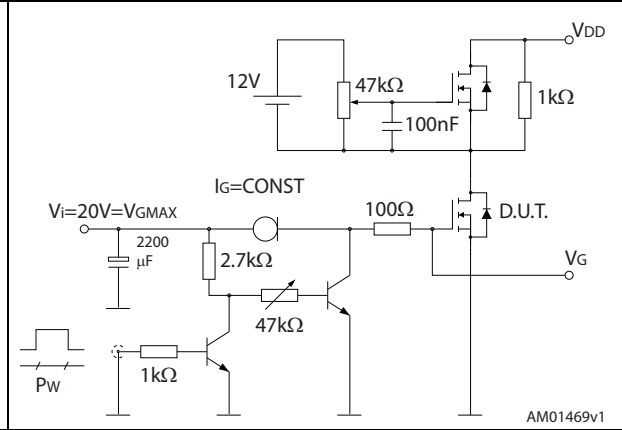**Figure 12. Source-drain diode forward characteristics**

3 Test circuits

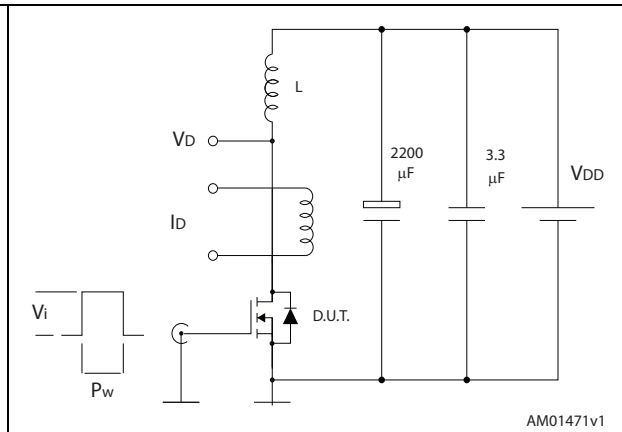**Figure 13. Switching times test circuit for resistive load**

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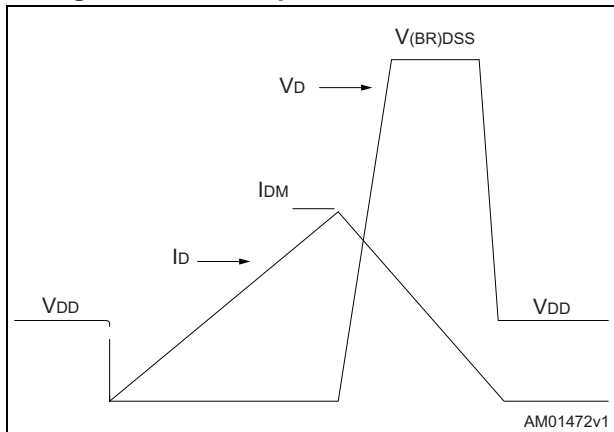**Figure 14. Gate charge test circuit**

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Figure 15. Test circuit for inductive load switching and diode recovery times
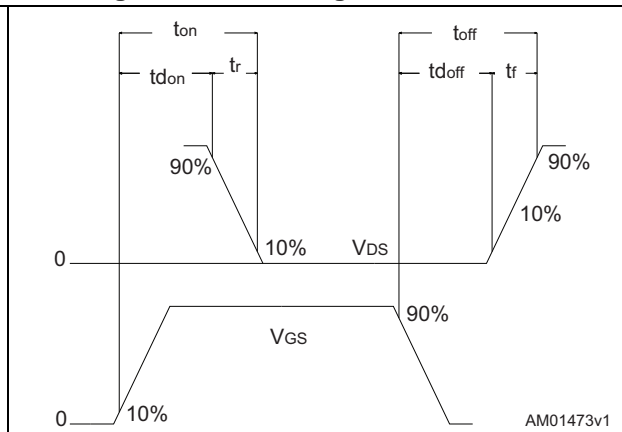

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Figure 16. Unclamped inductive load test circuit

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Figure 17. Unclamped inductive waveform

AM01472v1
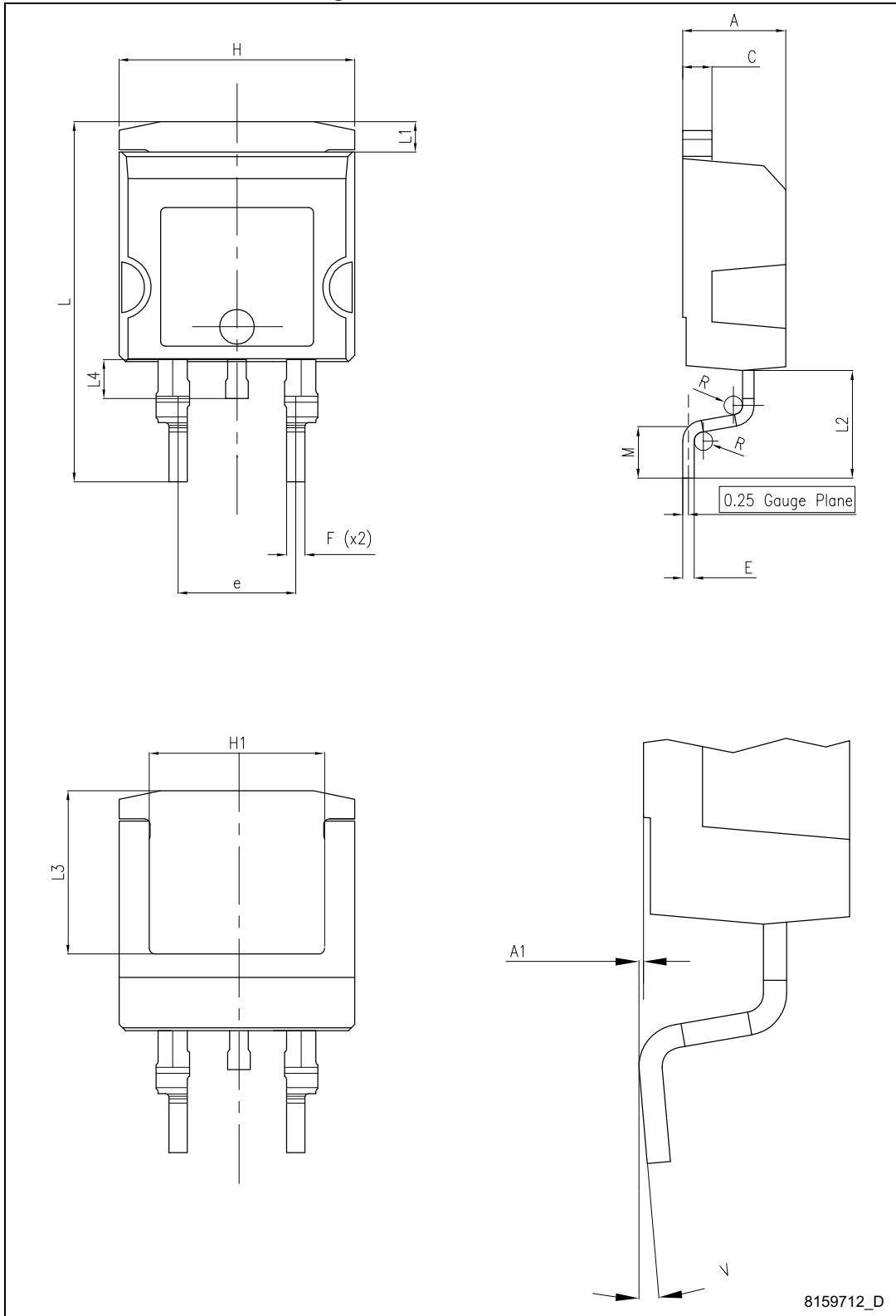
Figure 18. Switching time waveform

AM01473v1

4   Package information

Figure 19. H²PAK-2 outline

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Table 9. H²PAK-2 mechanical data

Dim.	mm		
	Min.	**Typ.**	**Max.**
A	4.30		4.80
A1	0.03		0.20
C	1.17		1.37
e	4.98		5.18
E	0.50		0.90
F	0.78		0.85
H	10.00		10.40
H1	7.40		7.80
L	15.30	-	15.80
L1	1.27		1.40
L2	4.93		5.23
L3	6.85		7.25
L4	1.5		1.7
M	2.6		2.9
R	0.20		0.60
V	0°		8°

Figure 20. H²PAK-2 recommended footprint (dimensions are in mm)
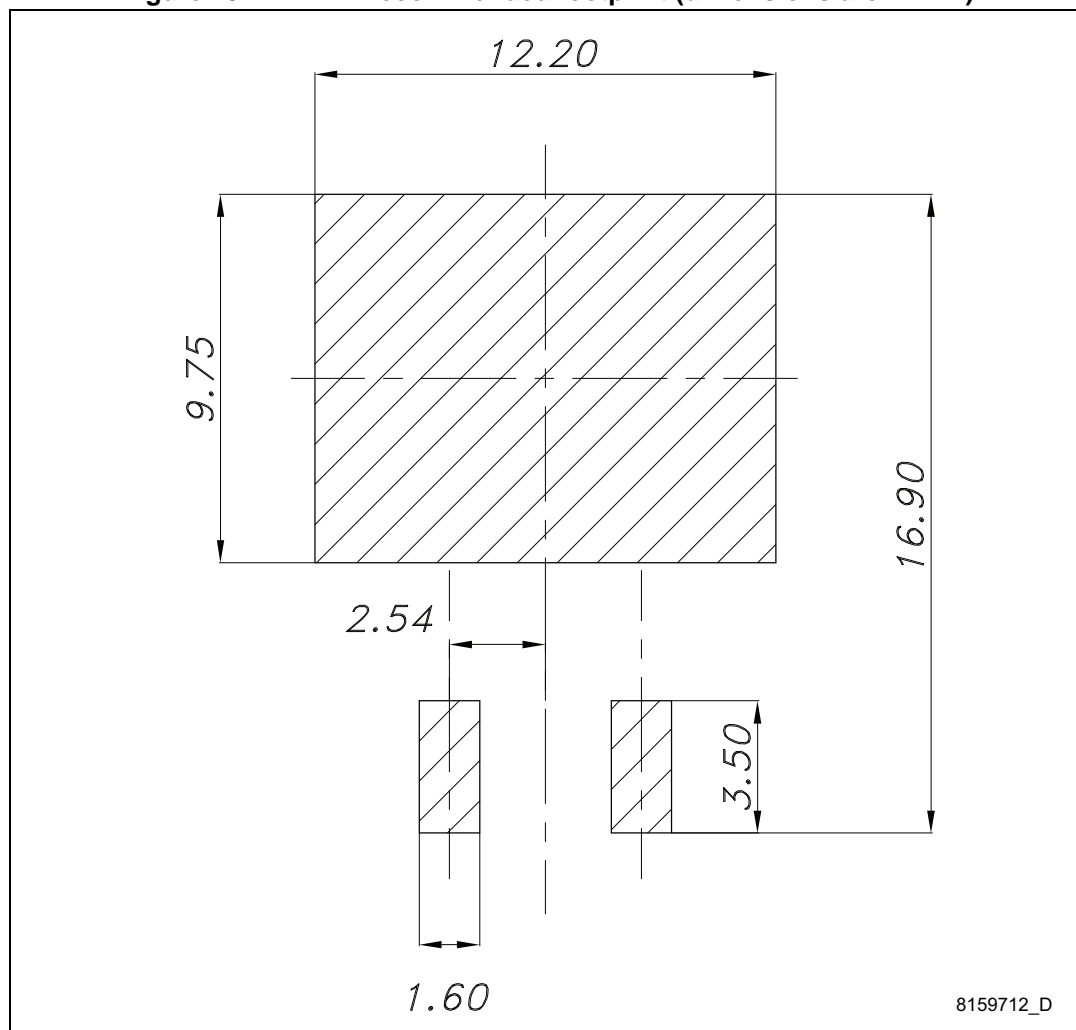
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5 Packing information

Figure 21. Tape

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Figure 22. Reel

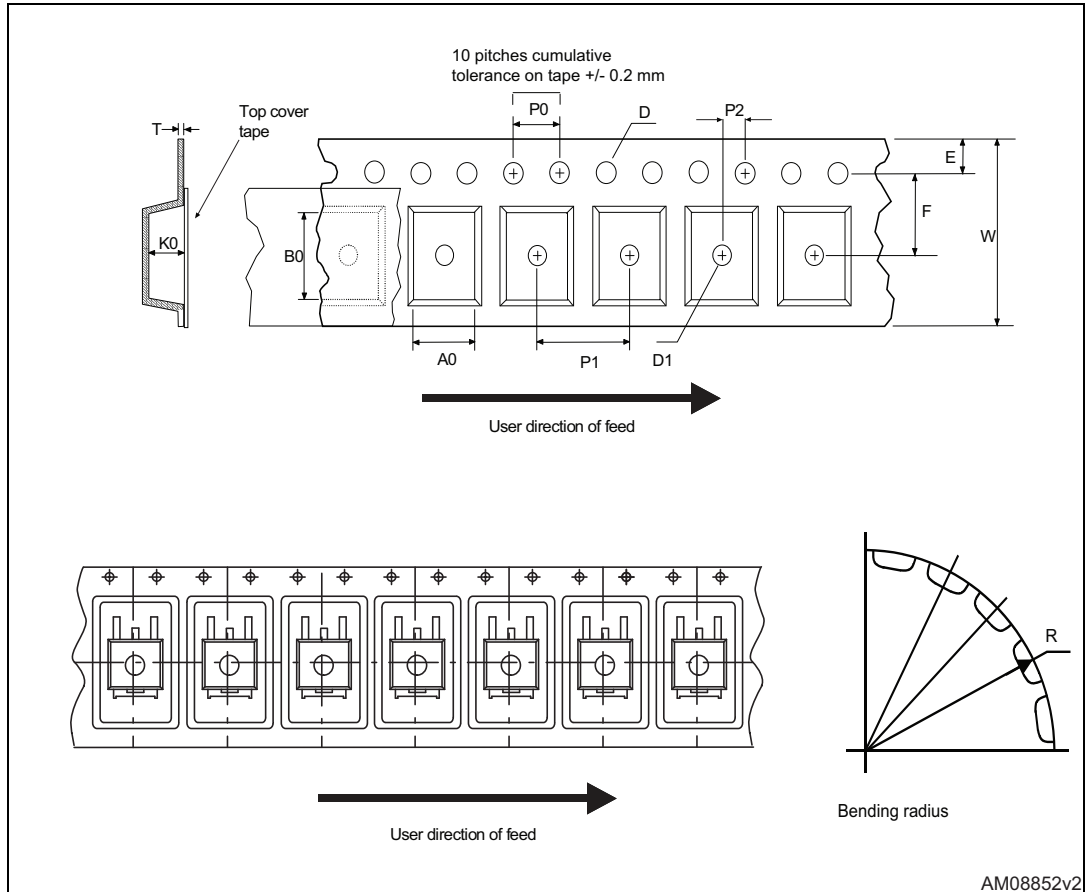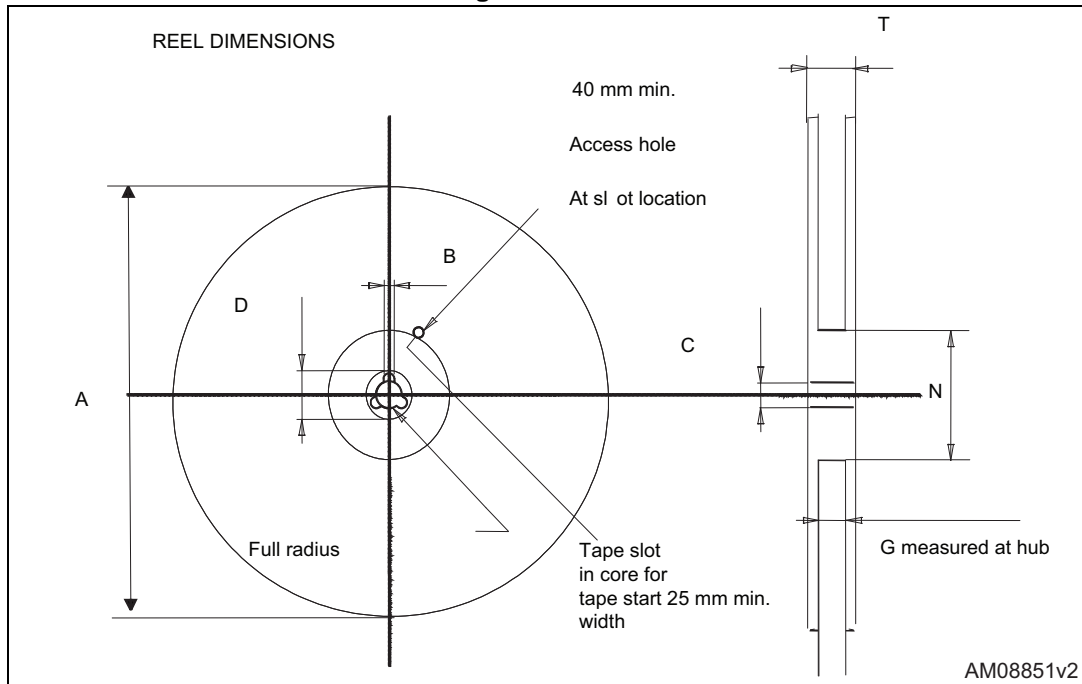**Table 10. H²PAK-2 tape and reel mechanical data**

Dim.	Tape mm Min.	Tape mm Max.	Dim.	Reel mm Min.	Reel mm Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base qty		1000
P2	1.9	2.1	Bulk qty		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

6 Revision history

Table 11. Document revision history

Date	Revision	Changes
20-May-2014	1	First release.
20-Feb-2015	2	Document status promoted from preliminary to production data. Updated *Section 4: Package information*. Updated title, features and description in cover page.

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