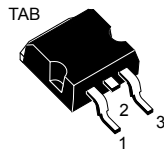
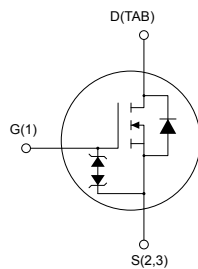


## Automotive-grade N-channel 950 V, 280 mΩ typ., 17.5 A MDmesh K5 Power MOSFET in an H<sup>2</sup>PAK-2 package


**H<sup>2</sup>PAK-2**


NCHG10TAB523TZ

### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>	P <sub>TOT</sub>
STH22N95K5-2AG	950 V	330 mΩ	17.5 A	250 W



- AEC-Q101 qualified
- Industry's lowest R<sub>DS(on)</sub> x area
- Industry's best FoM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

### Applications

- Switching applications

### Description

This very high voltage N-channel Power MOSFET is designed using MDmesh K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.



#### Product status link

[STH22N95K5-2AG](#)

#### Product summary<sup>(1)</sup>

<b>Order code</b>	STH22N95K5-2AG
<b>Marking</b>	22N95K5
<b>Package</b>	H <sup>2</sup> PAK-2
<b>Packing</b>	Tape and reel

1. The HTRB test was performed at 80% V<sub>(BR)DSS</sub> in compliance with AEC-Q101 rev. C. All the other tests were performed according to rev. D.

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	±30	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ °C}$	17.5	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ °C}$	11	A
$I_D^{(1)}$	Drain current (pulsed)	50	A
$P_{TOT}$	Total power dissipation at $T_C = 25\text{ °C}$	250	W
ESD	Gate-source human body model ( $R = 1.5\text{ k}\Omega$ , $C = 100\text{ pF}$ )	5	kV
$dv/dt^{(2)}$	Peak diode recovery voltage slope	4.5	V/ns
$dv/dt^{(3)}$	MOSFET $dv/dt$ ruggedness	50	
$T_J$	Operating junction temperature range	-55 to 150	°C
$T_{stg}$	Storage temperature range		

1. Pulse width limited by safe operating area.
2.  $I_{SD} \leq 17.5\text{ A}$ ,  $di/dt \leq 100\text{ A}/\mu\text{s}$ ;  $V_{DS\text{ peak}} \leq V_{(BR)DSS}$ .
3.  $V_{DS} \leq 760\text{ V}$ .

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	0.5	°C/W
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	30	°C/W

1. When mounted on FR-4 board of 1 inch<sup>2</sup>, 2 oz Cu.

**Table 3. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or not repetitive (pulse width limited by $T_J$ max.)	6	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J = 25\text{ °C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	182	mJ

## 2 Electrical characteristics

$T_C = 25\text{ °C}$  unless otherwise specified.

**Table 4. On/off-state**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	950			V
$I_{DSS}$	Zero-gate voltage drain current	$V_{GS} = 0\text{ V}, V_{DS} = 950\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}, V_{DS} = 950\text{ V}, T_C = 125\text{ °C}^{(1)}$			50	$\mu\text{A}$
$I_{GSS}$	Gate body leakage current	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 100\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 9\text{ A}$		280	330	m $\Omega$

1. Defined by design, not subject to production test.

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 100\text{ V}, f = 1\text{ MHz}, V_{GS} = 0\text{ V}$	-	1550	-	pF
$C_{oss}$	Output capacitance		-	140	-	pF
$C_{rss}$	Reverse transfer capacitance		-	1	-	pF
$C_{o(er)}^{(1)}$	Equivalent capacitance energy related	$V_{GS} = 0\text{ V}, V_{DS} = 0\text{ to }760\text{ V}$	-	65	-	pF
$C_{o(tr)}^{(2)}$	Equivalent capacitance time related			178	-	pF
$R_g$	Intrinsic gate resistance	$f = 1\text{ MHz}, I_D = 0\text{ A}$	-	3.5	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 760\text{ V}, I_D = 17.5\text{ A}, V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 15. Test circuit for gate charge behavior)	-	48	-	nC
$Q_{gs}$	Gate-source charge		-	9	-	nC
$Q_{gd}$	Gate-drain charge		-	32.5	-	nC

1.  $C_{o(er)}$  is a constant capacitance value that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .

2.  $C_{o(tr)}$  is a constant capacitance value that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 475\text{ V}, I_D = 9\text{ A}, R_G = 4.7\text{ }\Omega$ $V_{GS} = 10\text{ V}$	-	18	-	ns
$t_r$	Rise time		-	9	-	ns
$t_{d(off)}$	Turn-off delay time	(see Figure 14. Test circuit for resistive load switching times and Figure 19. Switching time waveform)	-	65	-	ns
$t_f$	Fall time		-	18	-	ns

**Table 7. Source-drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		17.5	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		50	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 17.5 \text{ A}, V_{GS} = 0 \text{ V}$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 17.5 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}, V_{DD} = 60 \text{ V}$ (see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	513		ns
$Q_{rr}$	Reverse recovery charge		-	12		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	46		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 17.5 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}, V_{DD} = 60 \text{ V}, T_j = 150 \text{ }^\circ\text{C}$ (see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	670		ns
$Q_{rr}$	Reverse recovery charge		-	15		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	44		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

**Table 8. Gate-source Zener diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR) GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1 \text{ mA}, I_D = 0 \text{ A}$	$\pm 30$	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

## 2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

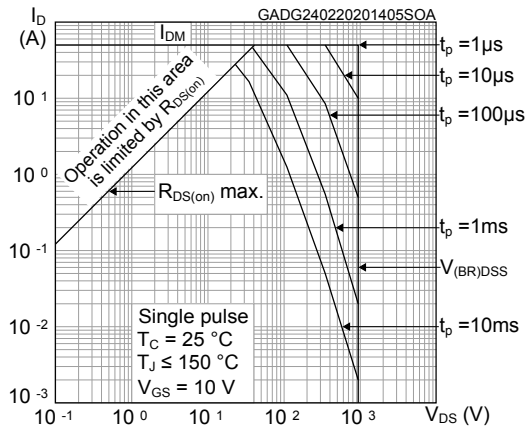


Figure 2. Maximum transient thermal impedance

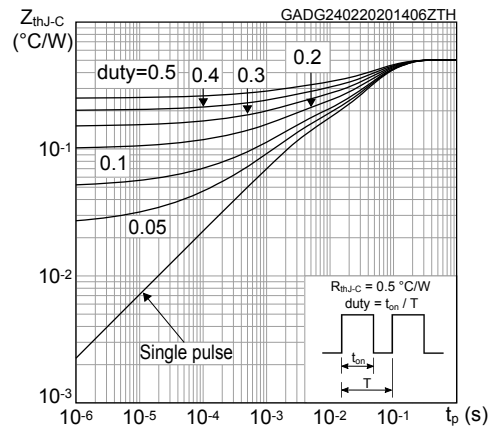


Figure 3. Typical output characteristics

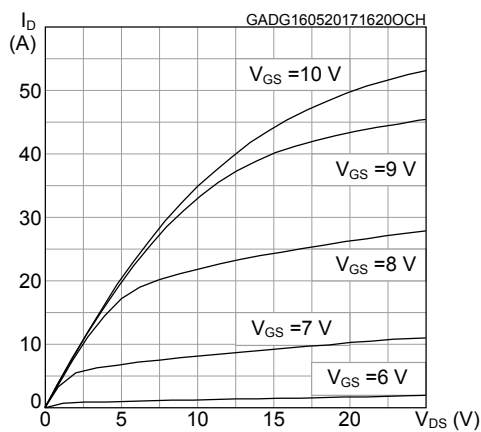


Figure 4. Typical transfer characteristics

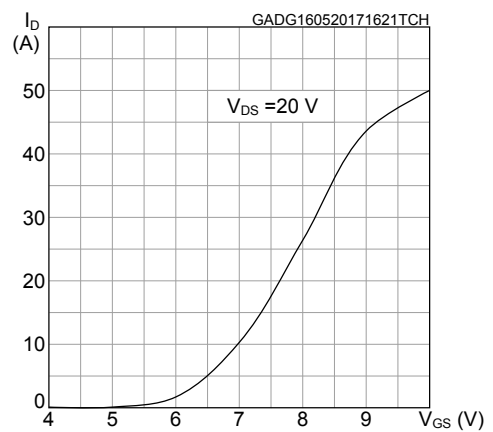


Figure 5. Typical gate charge characteristics

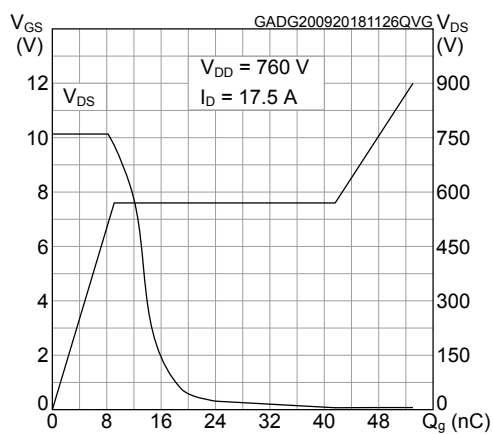


Figure 6. Typical drain-source on-resistance

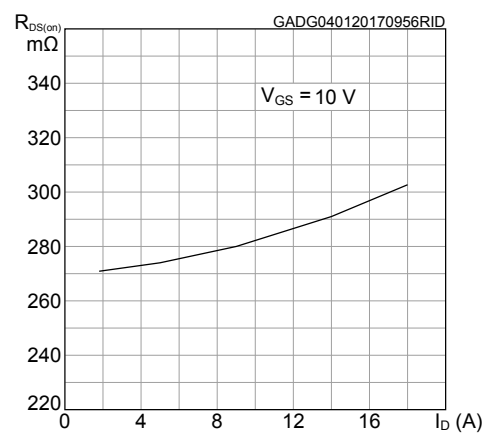


Figure 7. Typical capacitance characteristics

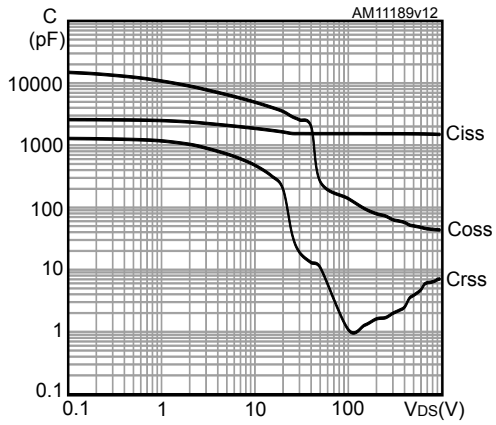


Figure 8. Typical output capacitance stored energy

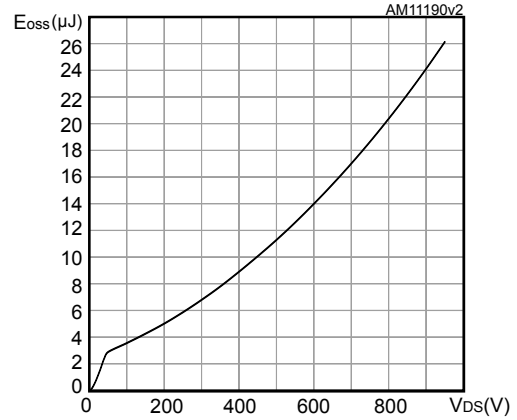


Figure 9. Normalized gate threshold vs temperature

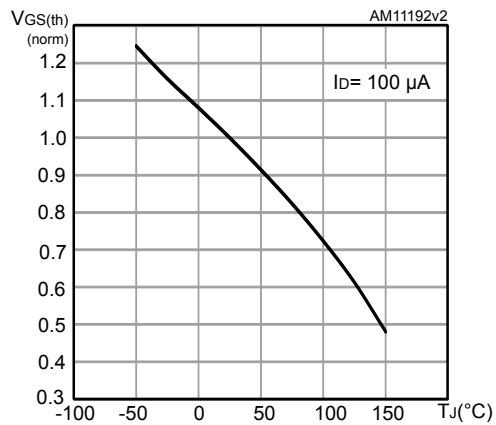


Figure 10. Normalized on-resistance vs temperature

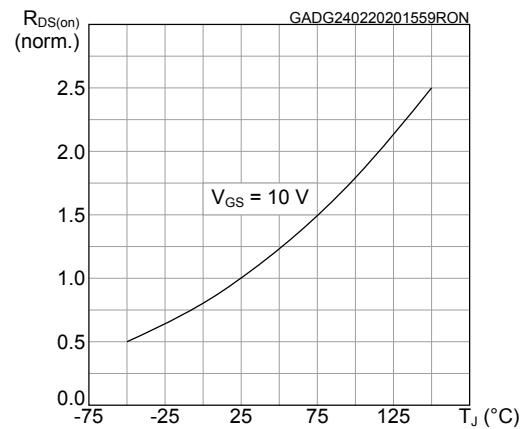


Figure 11. Maximum avalanche energy vs starting Tj

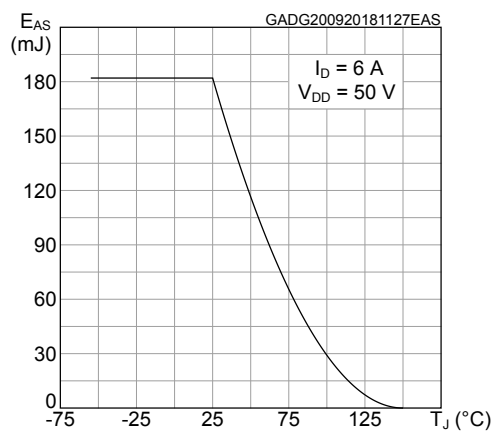
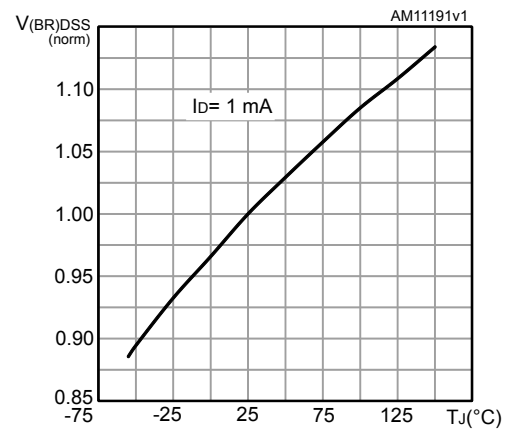
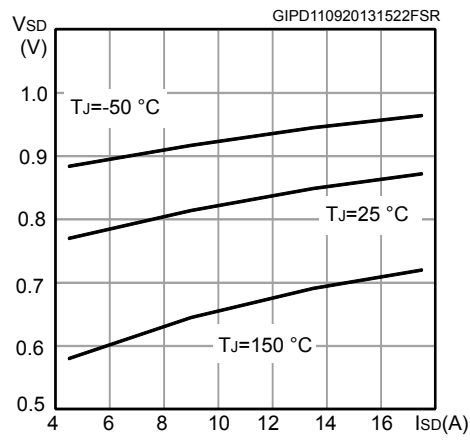


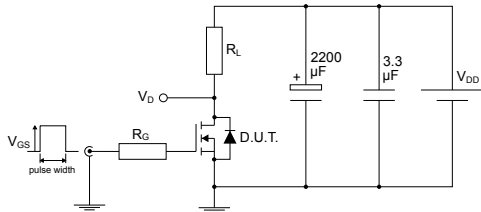
Figure 12. Normalized breakdown voltage vs temperature



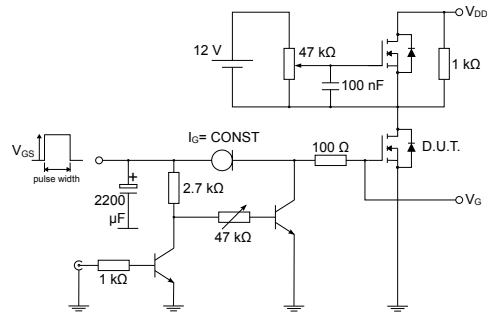
**Figure 13. Typical reverse diode forward characteristics**



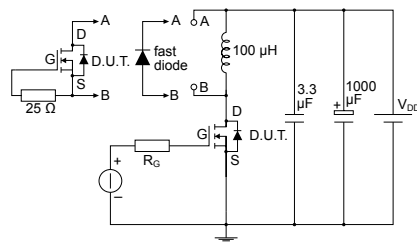
### 3 Test circuits

**Figure 14. Test circuit for resistive load switching times**


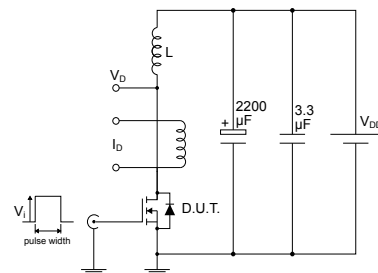
AM01468v1

**Figure 15. Test circuit for gate charge behavior**


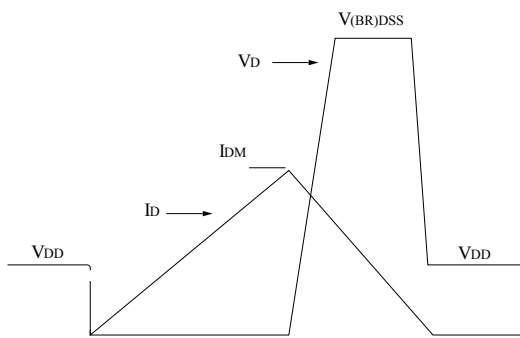
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**Figure 16. Test circuit for inductive load switching and diode recovery times**


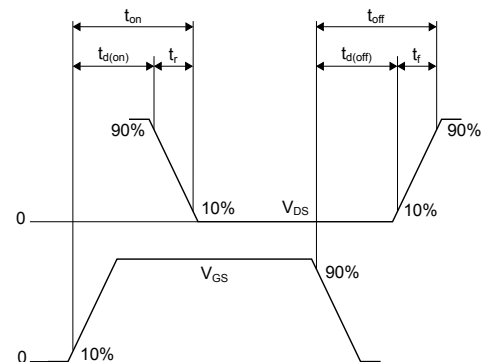
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**Figure 17. Unclamped inductive load test circuit**


AM01471v1

**Figure 18. Unclamped inductive waveform**


AM01472v1

**Figure 19. Switching time waveform**


AM01473v1

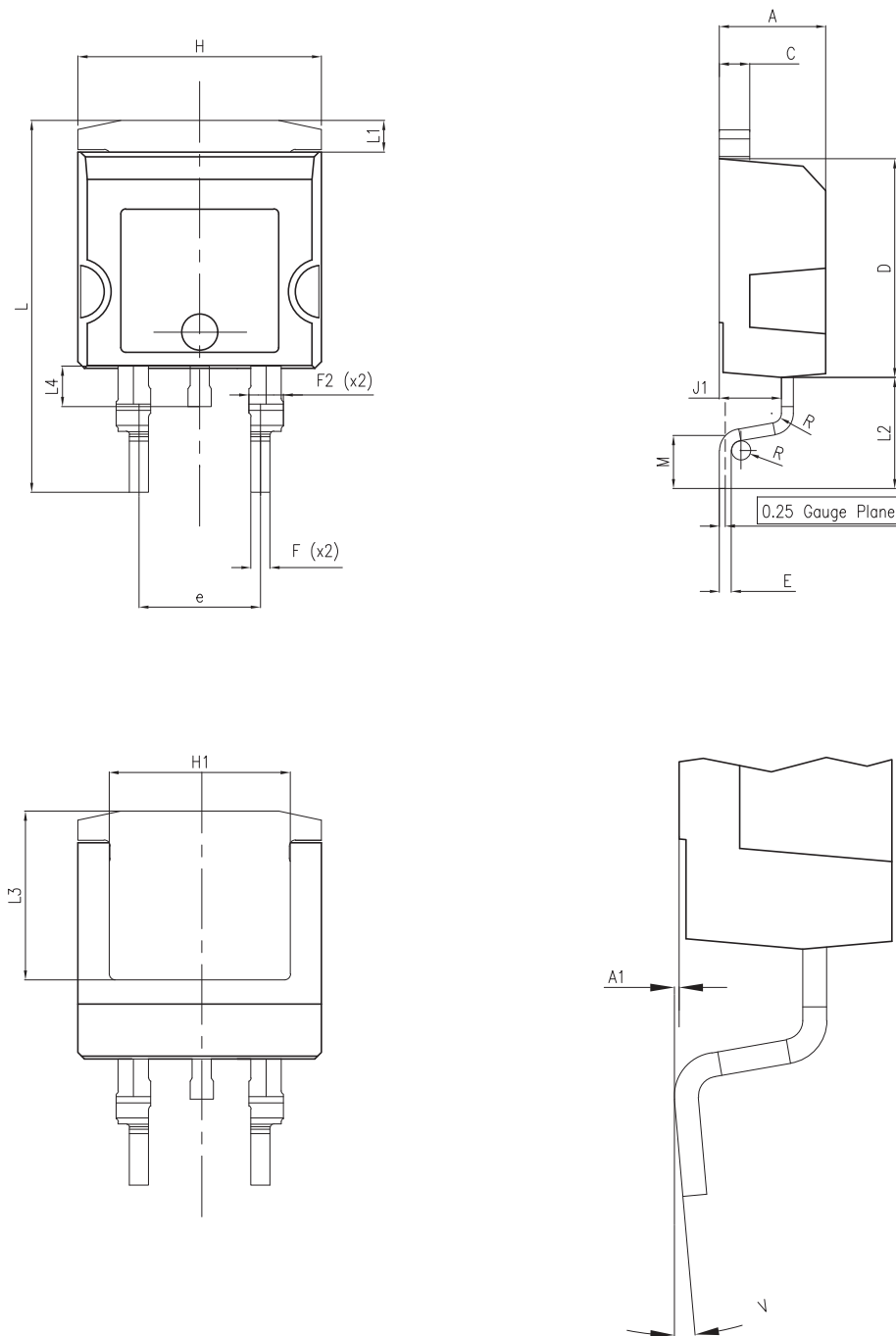


## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 4.1 H<sup>2</sup>PAK-2 package information

Figure 20. H<sup>2</sup>PAK-2 package outline

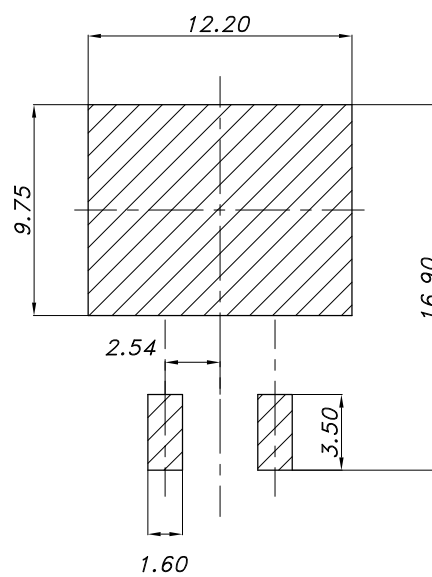


8159712\_9

**Table 9. H<sup>2</sup>PAK-2 package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.30		4.70
A1	0.03		0.20
C	1.17		1.37
D	8.95		9.35
e	4.98		5.18
E	0.50		0.90
F	0.78		0.85
F2	1.14		1.70
H	10.00		10.40
H1	7.40	-	7.80
J1	2.49		2.69
L	15.30		15.80
L1	1.27		1.40
L2	4.93		5.23
L3	6.85		7.25
L4	1.50		1.70
M	2.60		2.90
R	0.20		0.60
V	0°		8°

**Figure 21. H<sup>2</sup>PAK-2 recommended footprint**

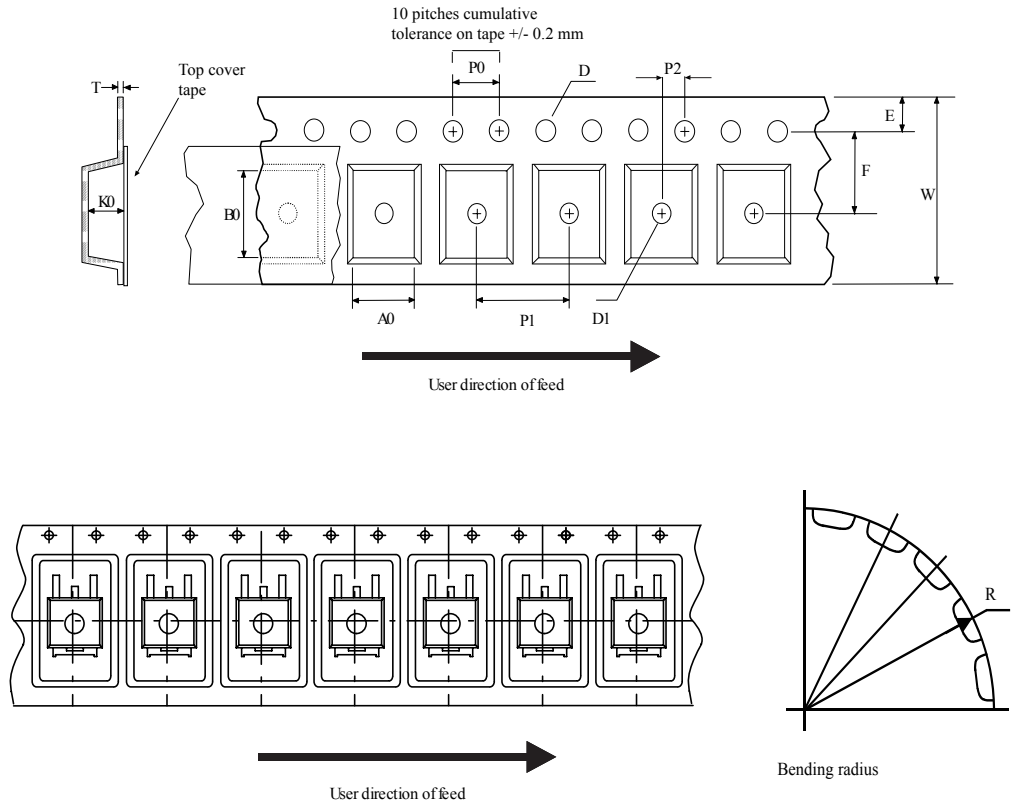


8159712\_9

*Note: Dimensions are in mm.*

## 4.2 Packing information

Figure 22. Tape outline



AM08852v2

Figure 23. Reel outline

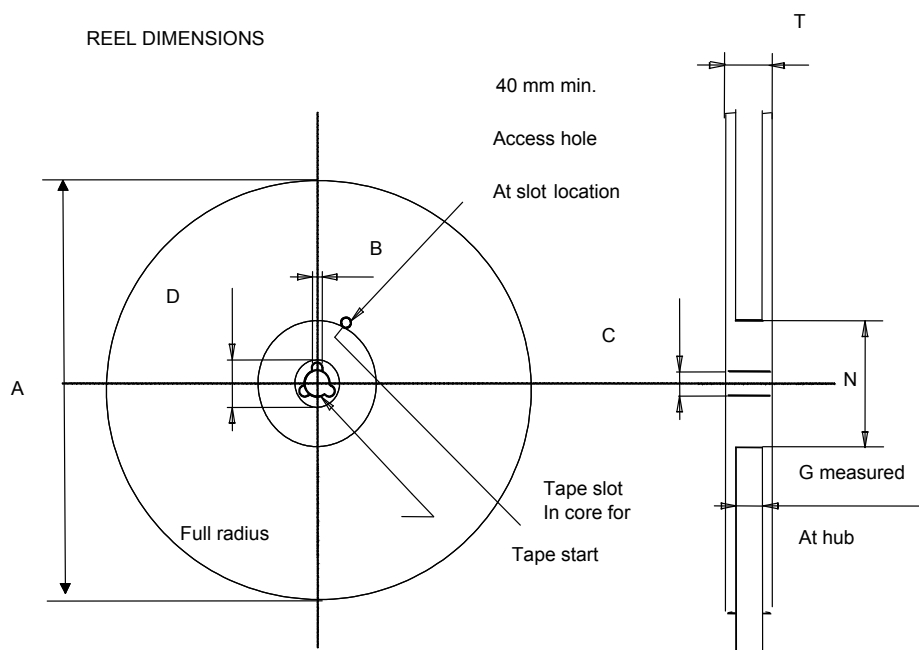


Table 10. Tape and reel mechanical data

Dim.	Tape		Dim.	Reel	
	mm			mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base quantity		1000
P2	1.9	2.1	Bulk quantity		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

## Revision history

**Table 11. Document revision history**

Date	Revision	Changes
04-Jul-2017	1	First release.
20-Sep-2018	2	Updated <i>Table 2. Thermal data, Figure 5. Gate charge vs gate-source voltage</i> and <i>Figure 11. Maximum avalanche energy vs starting T<sub>J</sub></i> . Updated <i>Section 4.1 H<sup>2</sup>PAK-2 package information</i> .
07-Mar-2019	3	Modified <i>Table 1. Absolute maximum ratings</i> . Minor text changes.
4-Mar-2020	4	Updated <i>Section 2.1 Electrical characteristics (curves)</i> . Minor text changes.
23-Apr-2020	5	Updated <i>Section 4.1 H<sup>2</sup>PAK-2 package information</i> .

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[SSM6P69NU,LF](#) [DMP22D4UFO-7B](#) [DMN1006UCA6-7](#)