

## Automotive-grade N-channel 40 V, 1.4 mΩ typ., 180 A STripFET™ F3 Power MOSFET in a H<sup>2</sup>PAK-2 package

Datasheet - production data

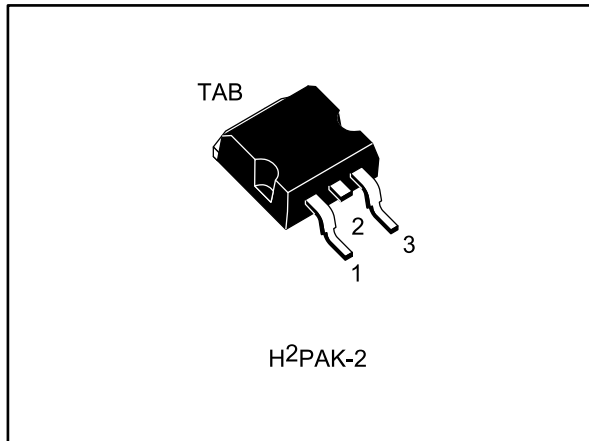


Figure 1: Internal schematic diagram

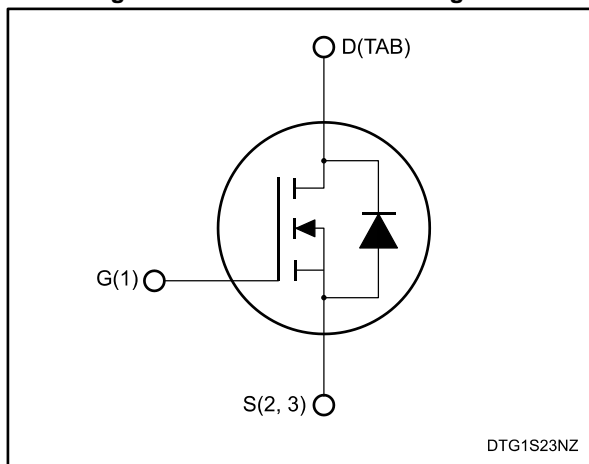


Table 1: Device summary

Order code	Marking	Package	Packing
STH270N4F3-2	270N4F3	H <sup>2</sup> PAK-2	Tape and reel

### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>
STH270N4F3-2	40 V	1.7 mΩ	190 A

- Designed for automotive applications and AEC-Q101 qualified
- Conduction losses reduced
- Low profile, very low parasitic inductance, high current package

### Applications

- Switching applications

### Description

This device is an N-channel Power MOSFET developed using STripFET™ F3 technology. It is designed to minimize on-resistance and gate charge to provide superior switching performance.

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# 1 Electrical ratings

**Table 2: Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	40	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	180	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	180	A
$I_D^{(2)}$	Drain current (pulsed)	720	A
$P_{TOT}^{(3)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	300	W
$E_{AS}^{(4)}$	Single pulse avalanche energy	1000	mJ
$T_J$	Operating junction temperature	-55 to 175	$^\circ\text{C}$
$T_{stg}$	Storage temperature		$^\circ\text{C}$

**Notes:**

- (1) Current limited by package  
 (2) Pulse width limited by safe operating area  
 (3) This value is rated according to  $R_{thj-c}$   
 (4) Starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $I_D = 80$ ,  $V_{DD} = 32\text{ V}$

**Table 3: Thermal resistance**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max.	0.5	$^\circ\text{C/W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max.	35	$^\circ\text{C/W}$

**Notes:**

- (1) When mounted on FR-4 board of 1 inch<sup>2</sup>, 2 oz Cu

## 2 Electrical characteristics

(T<sub>CASE</sub> = 25 °C unless otherwise specified)

**Table 4: On/off-state**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage (V <sub>GS</sub> = 0)	I <sub>D</sub> = 250 μA	40			V
I <sub>DSS</sub>	Zero gate voltage drain current (V <sub>GS</sub> = 0)	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 40 V			10	μA
		V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 40 V; T <sub>C</sub> = 125 °C			100	μA
I <sub>GSS</sub>	Gate body leakage current	V <sub>DS</sub> = 0, V <sub>GS</sub> = ±20 V			±200	nA
V <sub>GS(th)</sub>	Gate threshold voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2		4	V
R <sub>DS(on)</sub>	Static drain-source on-resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 80 A		1.4	1.7	mΩ

**Table 5: Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C <sub>iss</sub>	Input capacitance	V <sub>DS</sub> = 25 V, f = 1 MHz, V <sub>GS</sub> = 0	-	7400	-	pF
C <sub>oss</sub>	Output capacitance			1800		pF
C <sub>rss</sub>	Reverse transfer capacitance			50		pF
Q <sub>g</sub>	Total gate charge	V <sub>DD</sub> = 20 V, I <sub>D</sub> = 160 A V <sub>GS</sub> = 10 V See <a href="#">Figure 14: "Test circuit for gate charge behavior"</a>	-	110	-	nC
Q <sub>gs</sub>	Gate-source charge			30		nC
Q <sub>gd</sub>	Gate-drain charge			25		nC

**Table 6: Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t <sub>d(on)</sub>	Turn-on delay time	V <sub>DD</sub> = 20 V, I <sub>D</sub> = 80 A, R <sub>G</sub> = 4.7 Ω, V <sub>GS</sub> = 10 V See <a href="#">Figure 2: "Safe operating area"</a>	-	25	-	ns
t <sub>r</sub>	Rise time			180		ns
t <sub>d(off)</sub>	Turn-off delay time			110		ns
t <sub>f</sub>	Fall time			45		ns

Table 7: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}^{(1)}$	Source-drain current				180	A
$I_{SDM}^{(2)}$	Source-drain current (pulsed)				720	A
$V_{SD}^{(3)}$	Forward on voltage	$I_{SD} = 180\text{ A}, V_{GS} = 0$			1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 160\text{ A},$ $di/dt = 100\text{ A}/\mu\text{s},$ $V_{DD} = 32\text{ V}, T_j = 150$ $^{\circ}\text{C}$ <i>Figure 15: "Test circuit for inductive load switching and diode recovery times"</i>		70		ns
$Q_{rr}$	Reverse recovery charge			225		nC
$I_{RRM}$	Reverse recovery current				3.2	

**Notes:**

- <sup>(1)</sup>Current limited by package
- <sup>(2)</sup>Pulse width limited by safe operating area
- <sup>(3)</sup>Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.2 Electrical characteristics (curves)

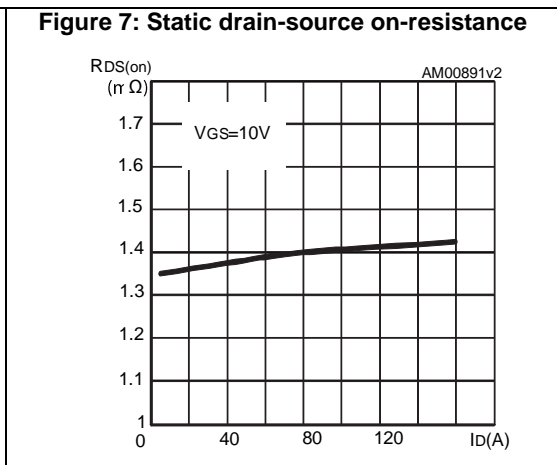
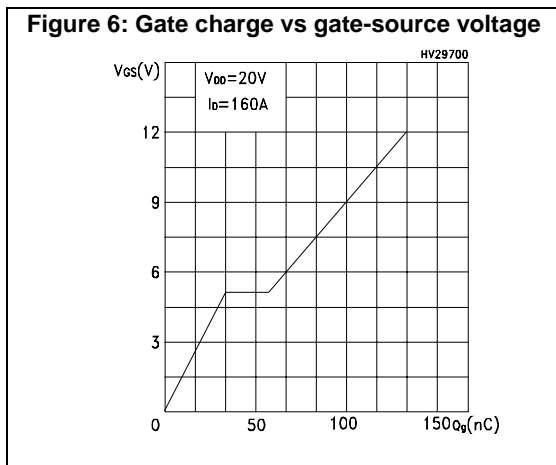
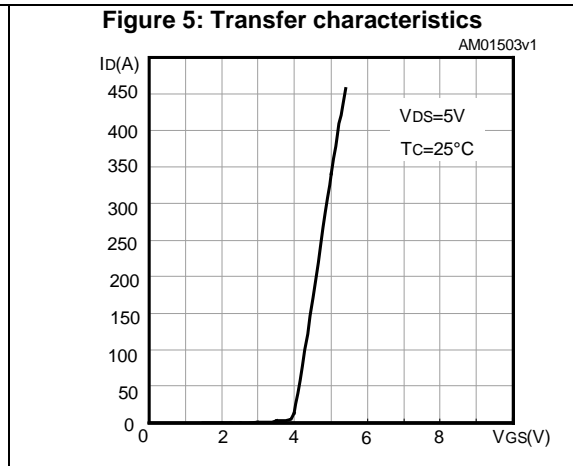
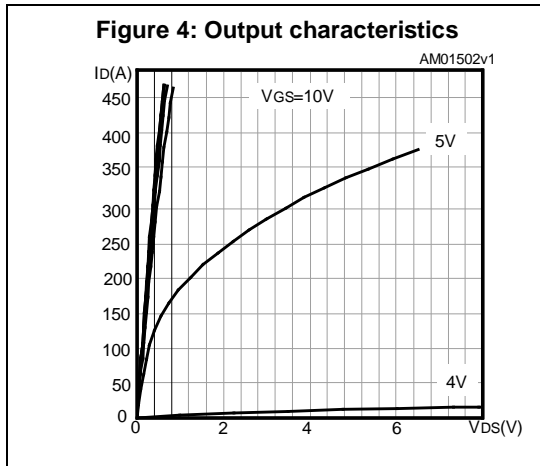
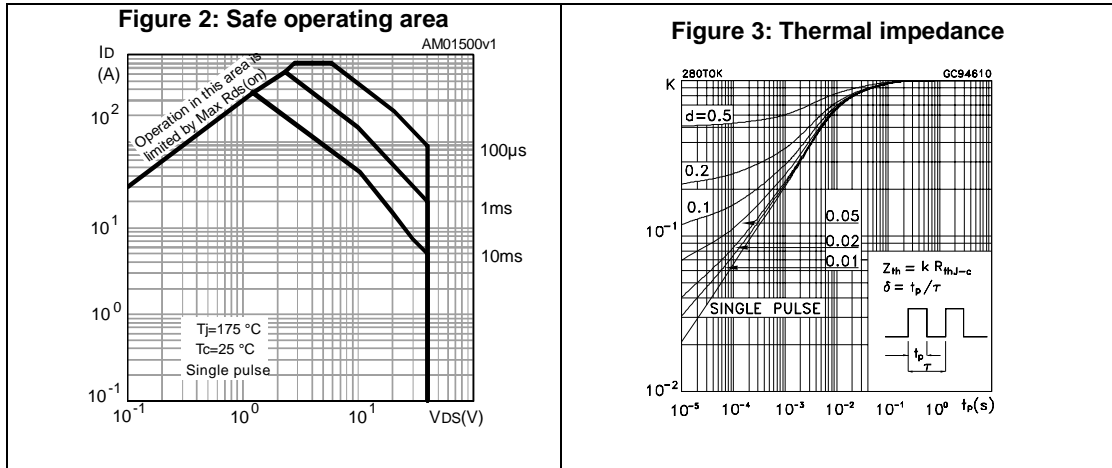


Figure 8: Capacitance variations

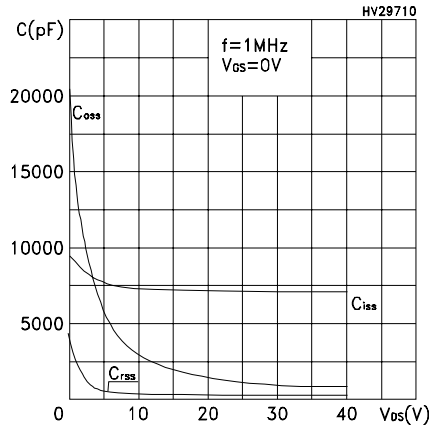


Figure 9: Normalized gate threshold voltage vs temperature

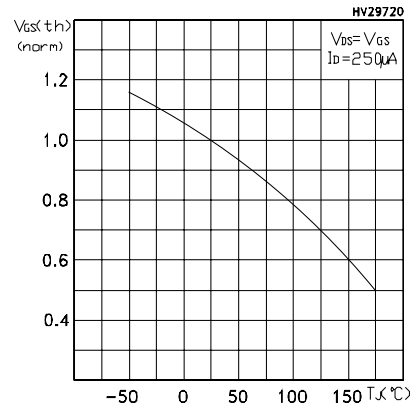


Figure 10: Normalized on-resistance vs temperature

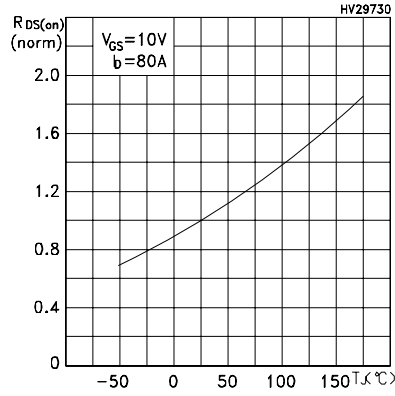


Figure 11: Normalized V(BR)DSS vs temperature

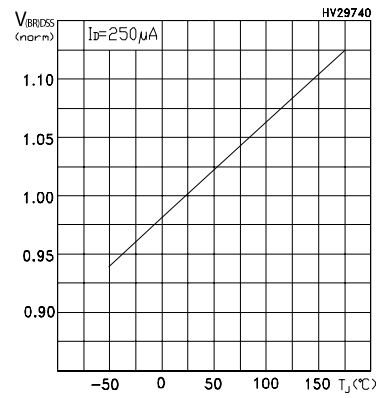
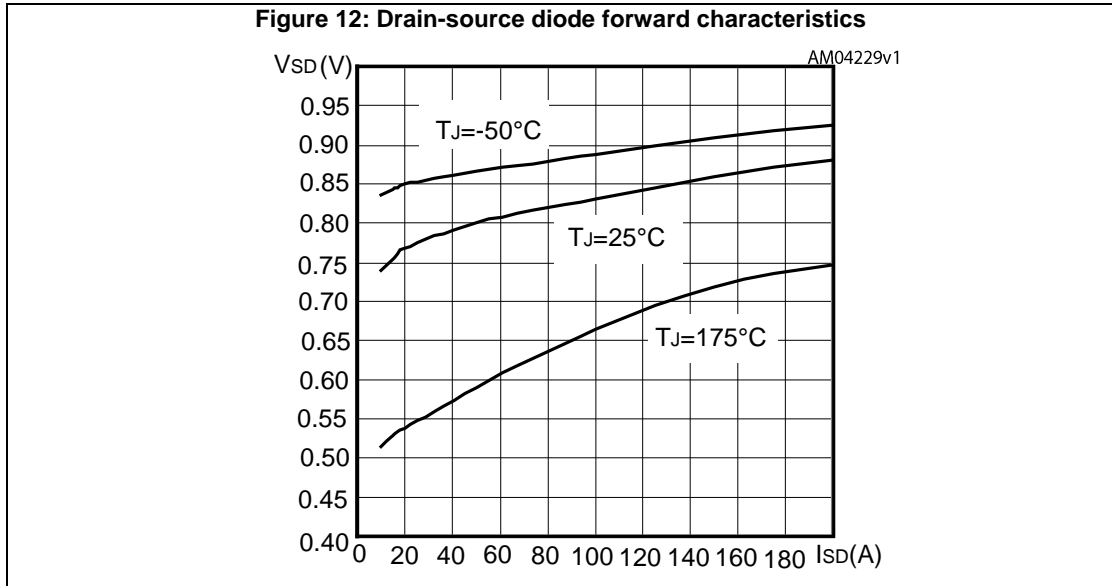


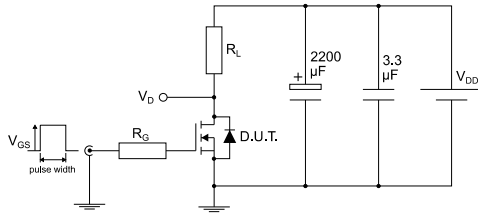
Figure 12: Drain-source diode forward characteristics





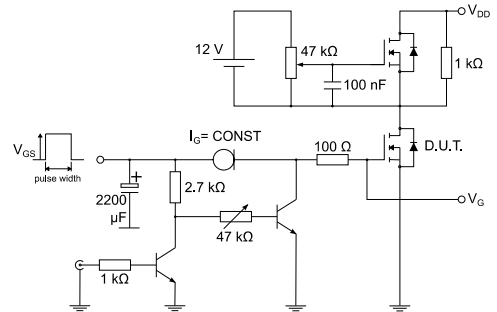
### 3 Test circuits

**Figure 13: Test circuit for resistive load switching times**



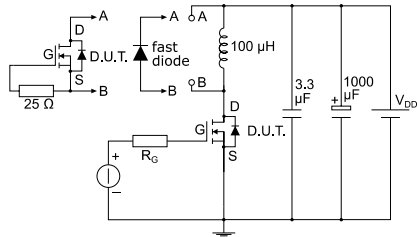
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**Figure 14: Test circuit for gate charge behavior**



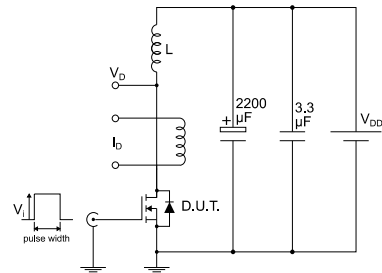
AM01469v1

**Figure 15: Test circuit for inductive load switching and diode recovery times**



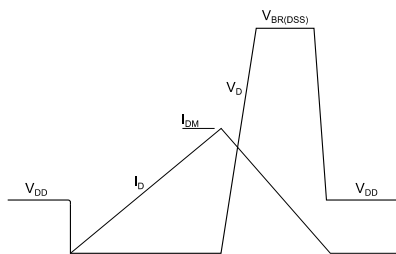
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**Figure 16: Unclamped inductive load test circuit**



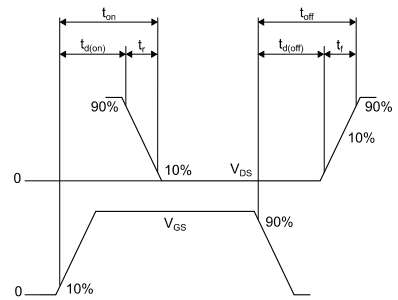
AM01471v1

**Figure 17: Unclamped inductive waveform**



AM01472v1

**Figure 18: Switching time waveform**



AM01473v1

## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

### 4.1 H<sup>2</sup>PAK-2 package information

Figure 19: H<sup>2</sup>PAK-2 package outline

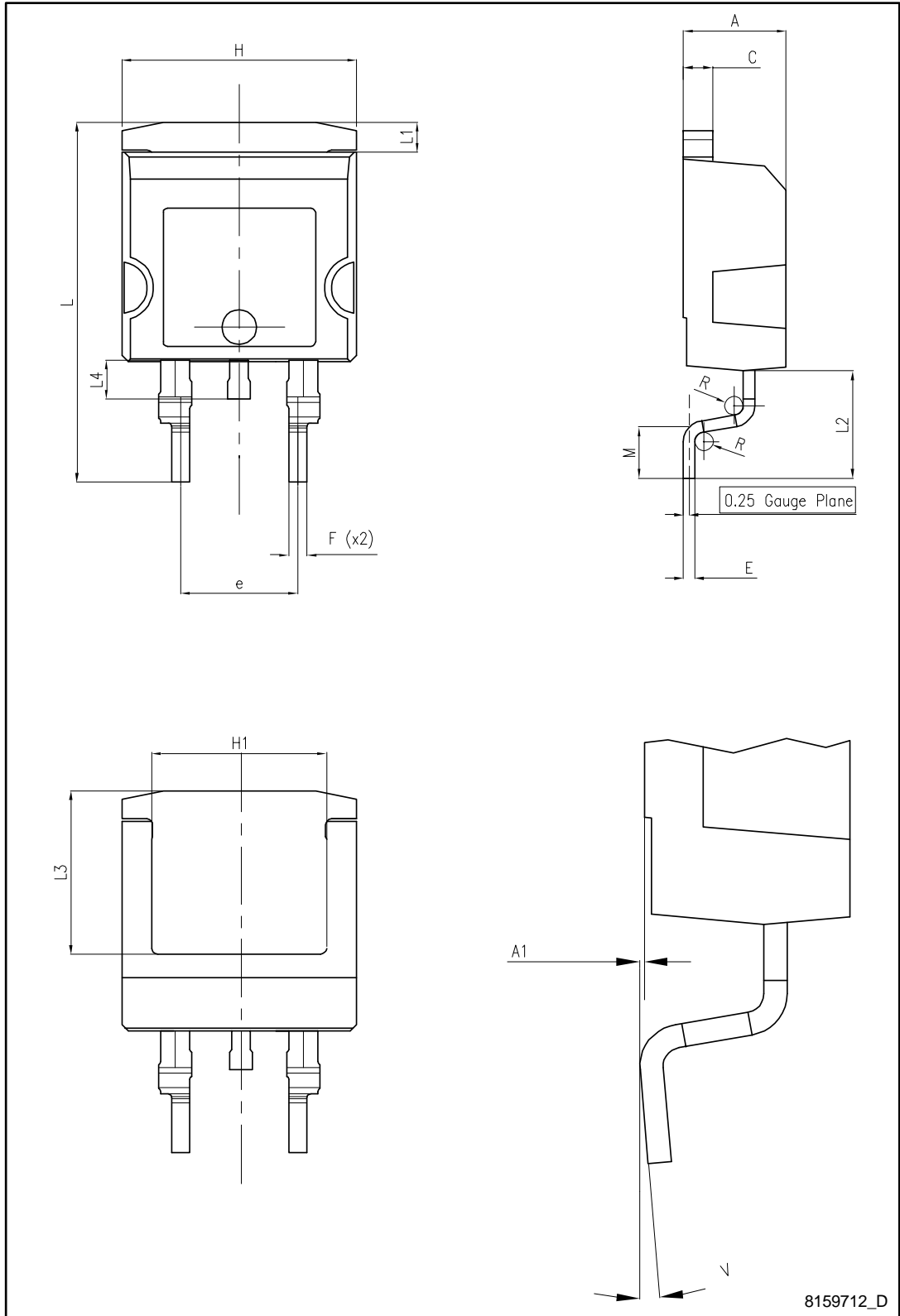
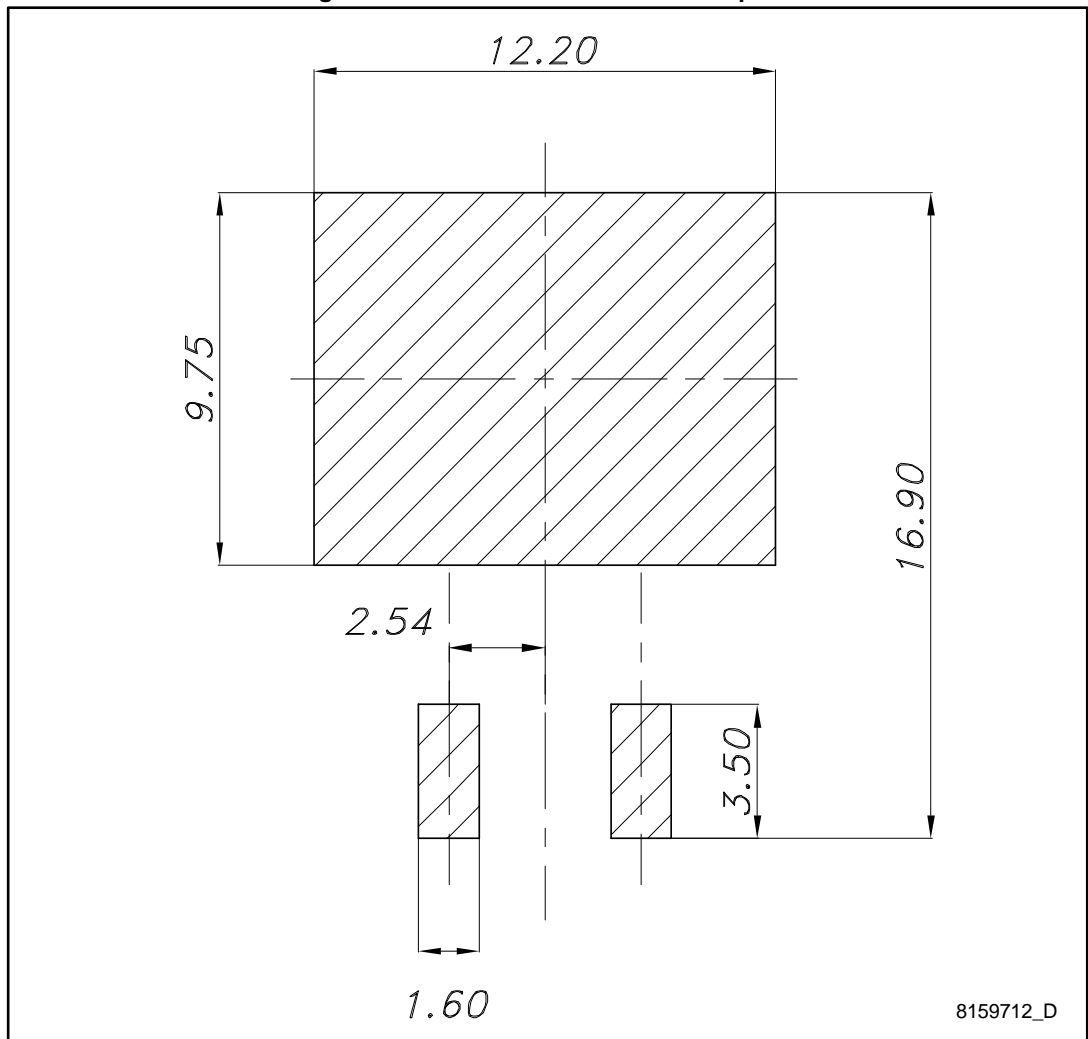


Table 8: H<sup>2</sup>PAK-2 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.30	-	4.80
A1	0.03		0.20
C	1.17		1.37
e	4.98		5.18
E	0.50		0.90
F	0.78		0.85
H	10.00		10.40
H1	7.40		7.80
L	15.30		15.80
L1	1.27		1.40
L2	4.93		5.23
L3	6.85		7.25
L4	1.5		1.7
M	2.6		2.9
R	0.20		0.60
V	0°		8°

Figure 20: H<sup>2</sup>PAK-2 recommended footprint



8159712\_D

# 5 Packaging information

Figure 21: Tape outline

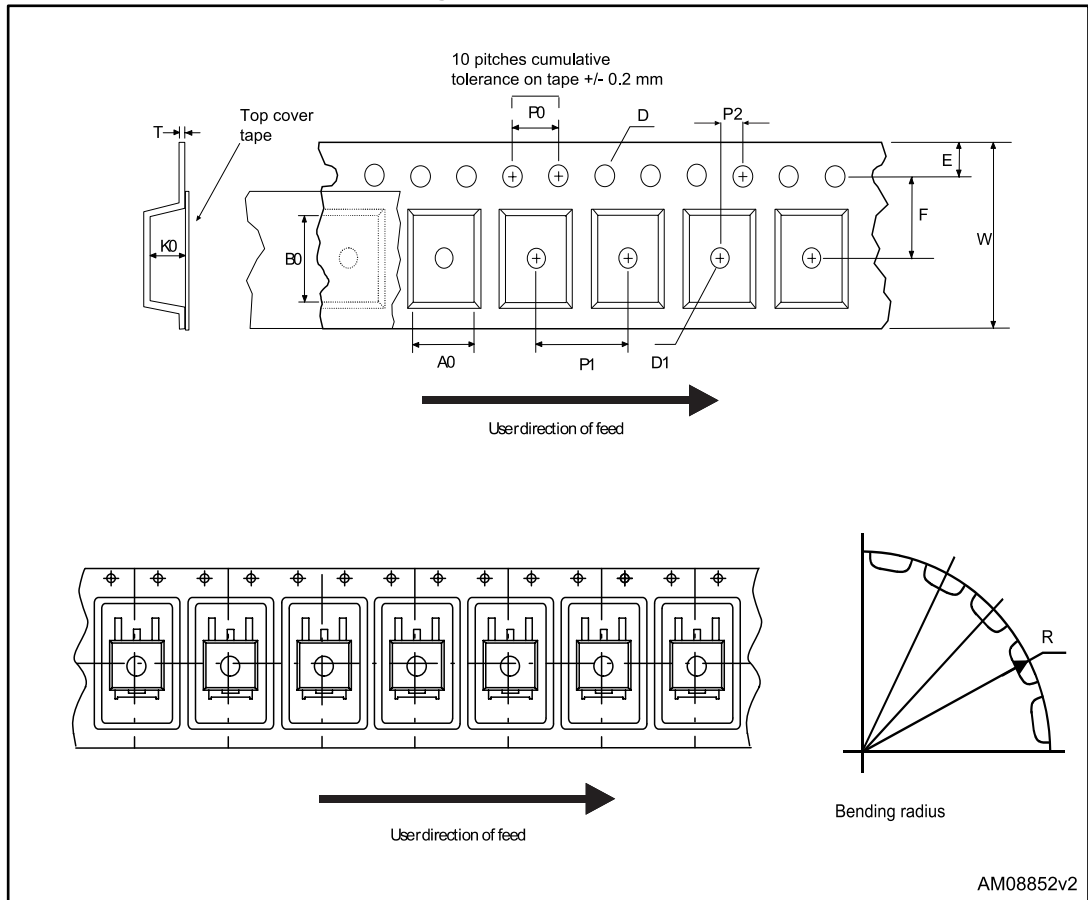


Figure 22: Reel outline

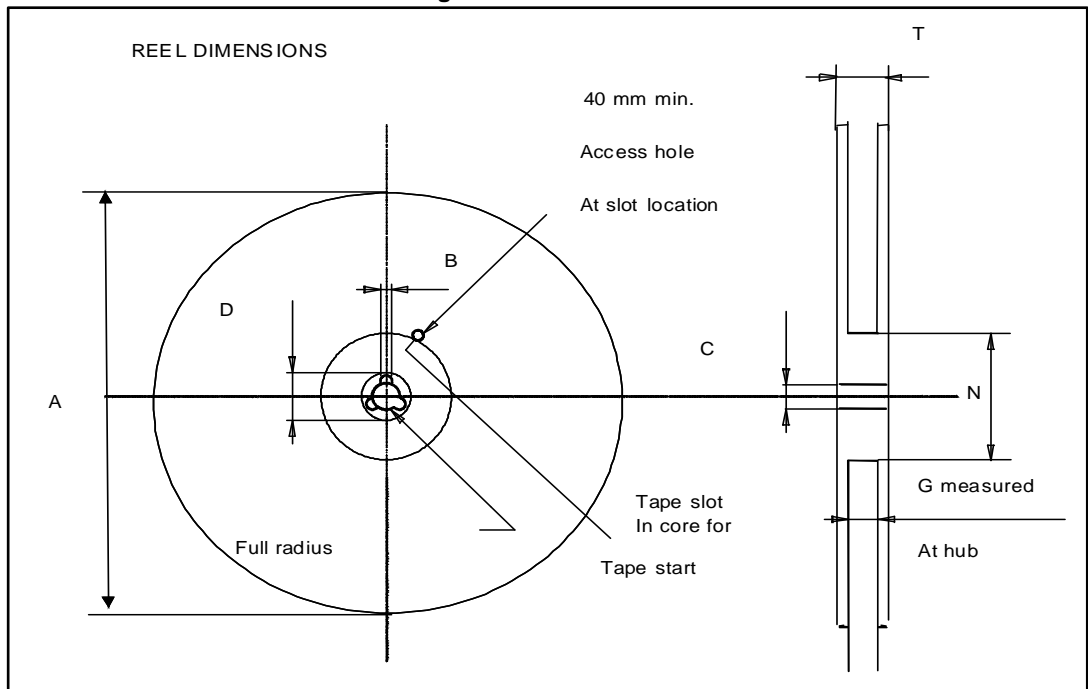


Table 9: Tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base quantity		1000
P2	1.9	2.1	Bulk quantity		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

## 6 Revision history

**Table 10: Document revision history**

Date	Revision	Changes
10-Jan-2010	1	Initial release.
14-Mar-2013	2	<ul style="list-style-type: none"><li>• Added H<sup>2</sup>PAK-2 package.</li><li>• Updated: package and packing information.</li><li>• Minor text changes</li></ul>
02-Dec-2014	3	<ul style="list-style-type: none"><li>• Updated: H<sup>2</sup>PAK-6 package information.</li><li>• Updated the title, features and description.</li><li>• Minor text changes.</li></ul>
22-Oct-2015	4	<ul style="list-style-type: none"><li>• Updated the title and features.</li><li>• Minor text changes.</li></ul>



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