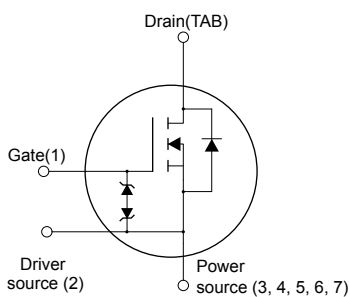
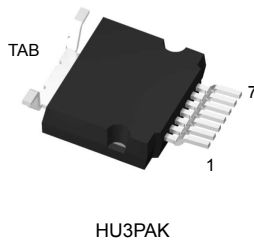


## Automotive-grade N-channel 600 V, 84 mΩ typ., 29 A MDmesh DM6 Power MOSFET in an HU3PAK package




N-chG1DS2PS34567DTABZ



### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>
STHU36N60DM6AG	600 V	99 mΩ	29 A

- AEC-Q101 qualified 
- Fast-recovery body diode
- Lower R<sub>DS(on)</sub> per area vs previous generation
- Low gate charge, input capacitance and resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected
- Excellent switching performance thanks to the extra driving source pin

### Applications

- Switching applications

### Description

This high-voltage N-channel Power MOSFET is part of the MDmesh DM6 fast-recovery diode series. Compared with the previous MDmesh fast generation, DM6 combines very low recovery charge (Q<sub>rr</sub>), recovery time (t<sub>rr</sub>) and excellent improvement in R<sub>DS(on)</sub> per area with one of the most effective switching behaviors available in the market for the most demanding high-efficiency bridge topologies and ZVS phase-shift converters.

#### Product status link

[STHU36N60DM6AG](#)

#### Product summary

<b>Order code</b>	STHU36N60DM6AG
<b>Marking</b>	36N60DM6
<b>Package</b>	HU3PAK
<b>Packing</b>	Tape and reel

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	$\pm 25$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	29	A
	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	18	
$I_D^{(1)}$	Drain current (pulsed)	103	A
$P_{TOT}$	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	210	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	100	V/ns
$di/dt^{(3)}$	Peak diode recovery current slope	1000	A/ $\mu\text{s}$
$dv/dt^{(3)}$	MOSFET $dv/dt$ ruggedness	100	V/ns
$T_J$	Operating junction temperature range	-55 to 150	$^\circ\text{C}$
$T_{stg}$	Storage temperature range		$^\circ\text{C}$

1. Pulse width limited by safe operating area.
2.  $I_{SD} \leq 29\text{ A}$ ,  $V_{DS(peak)} < V_{(BR)DSS}$ ,  $V_{DD} = 400\text{ V}$
3.  $V_{DS} \leq 480\text{ V}$

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thJC}$	Thermal resistance, junction-to-case	0.6	$^\circ\text{C/W}$
$R_{thJB}^{(1)}$	Thermal resistance, junction-to-board	30	

1. When mounted on 1 inch<sup>2</sup> FR-4, 2 Oz copper board.

**Table 3. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or not repetitive (pulse width limited by $T_{jmax}$ )	6	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 100\text{ V}$ )	630	mJ

## 2 Electrical characteristics

$T_C = 25\text{ °C}$  unless otherwise specified

**Table 4. On/off-state**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$	600			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 600\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ , $V_{DS} = 600\text{ V}$ , $T_C = 125\text{ °C}^{(1)}$			200	
$I_{GSS}$	Gate body leakage current	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 25\text{ V}$			$\pm 5$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	3.25	4.00	4.75	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 14.5\text{ A}$		84	99	m $\Omega$

1. Specified By Design – Not tested in production.

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$	-	1960	-	pF
$C_{oss}$	Output capacitance		-	140	-	pF
$C_{rSS}$	Reverse transfer capacitance		-	2	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }480\text{ V}$ , $V_{GS} = 0\text{ V}$	-	335	-	pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	1.5	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 480\text{ V}$ , $I_D = 29\text{ A}$ , $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 15. Test circuit for gate charge behavior)	-	46	-	nC
$Q_{gs}$	Gate-source charge		-	13	-	nC
$Q_{gd}$	Gate-drain charge		-	22	-	nC

1.  $C_{oss\text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ .

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$ , $I_D = 14.5\text{ A}$ , $R_G = 4.7\text{ }\Omega$ ,	-	16	-	ns
$t_r$	Rise time	$V_{GS} = 10\text{ V}$	-	5.3	-	ns
$t_{d(off)}$	Turn-off delay time	(see Figure 14. Switching times test circuit for resistive load and Figure 19. Switching time waveform)	-	50	-	ns
$t_f$	Fall time		-	7	-	ns

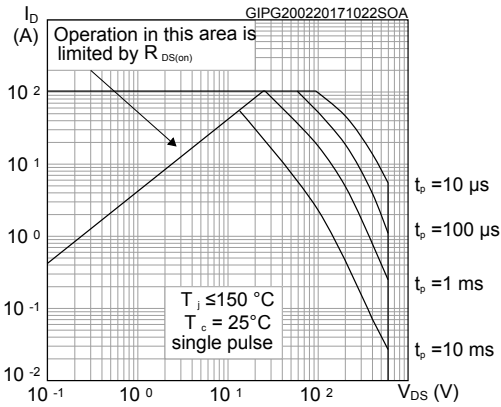
**Table 7. Source-drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		29	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		103	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 29\text{ A}, V_{GS} = 0\text{ V}$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 29\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, V_{DD} = 60\text{ V}$ (see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	110		ns
$Q_{rr}$	Reverse recovery charge		-	0.5		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	9		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 29\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, V_{DD} = 60\text{ V},$ $T_j = 150\text{ }^\circ\text{C}$ (see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	215		ns
$Q_{rr}$	Reverse recovery charge		-	2		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	17		A

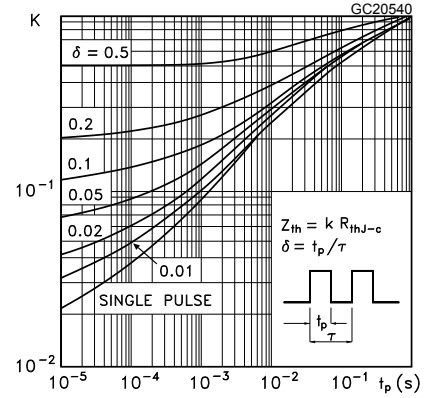
1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)

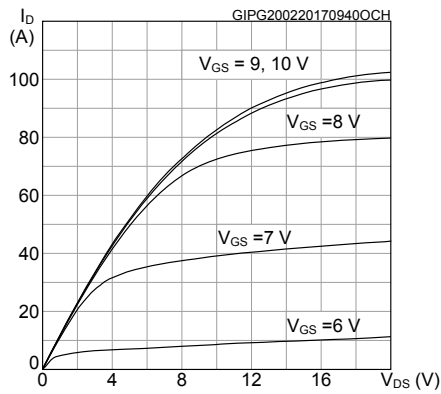
**Figure 1. Safe operating area**



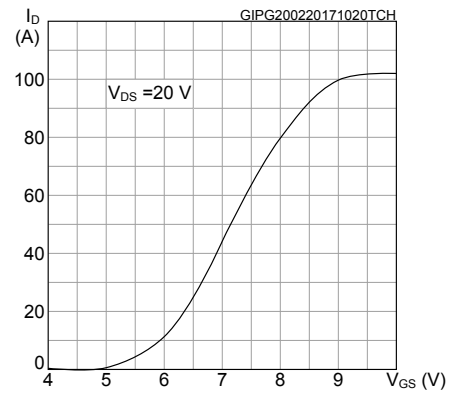
**Figure 2. Thermal impedance**



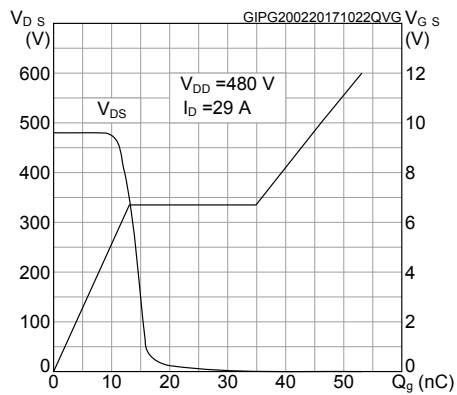
**Figure 3. Output characteristics**



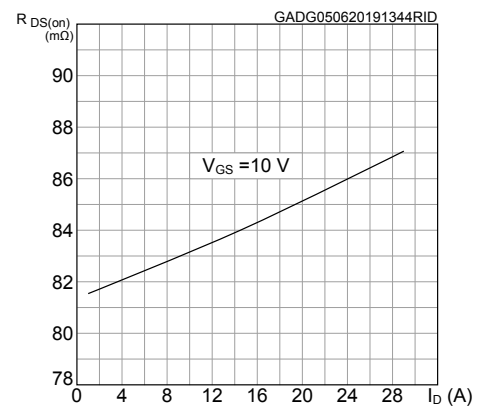
**Figure 4. Transfer characteristics**



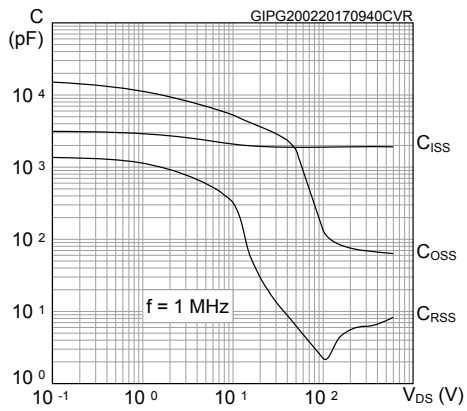
**Figure 5. Gate charge vs gate-source voltage**



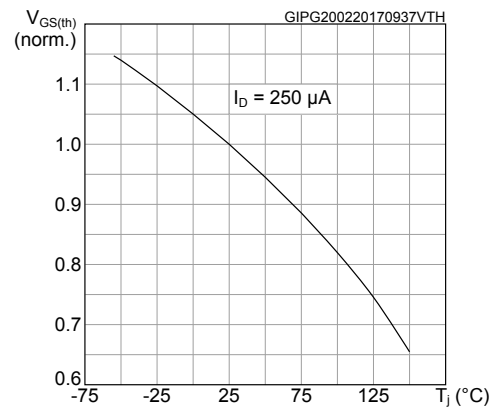
**Figure 6. Static drain-source on-resistance**



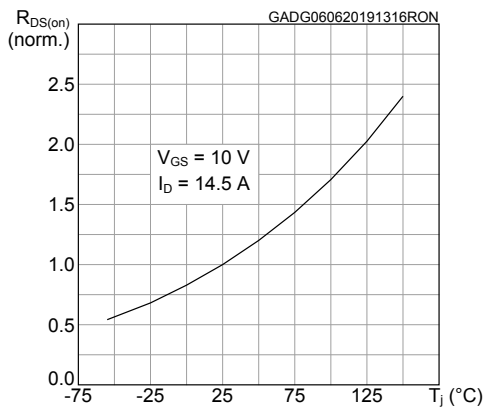
**Figure 7. Capacitance variations**



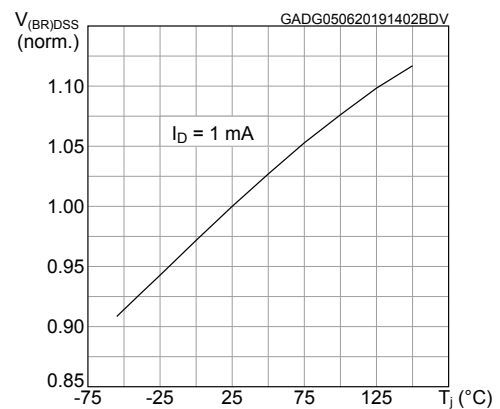
**Figure 8. Normalized gate threshold voltage vs temperature**



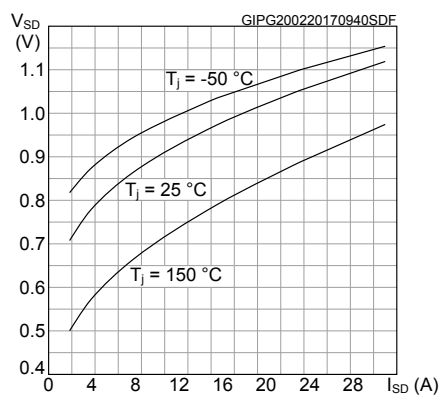
**Figure 9. Normalized on-resistance vs temperature**



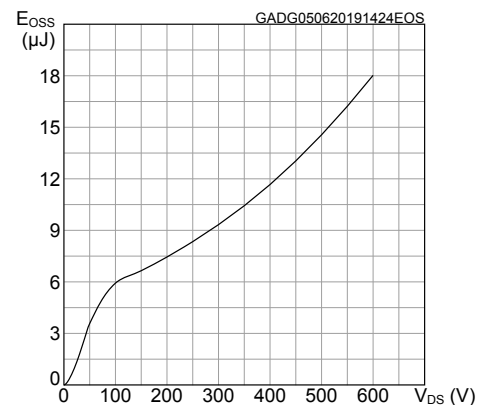
**Figure 10. Normalized  $V_{(BR)DSS}$  vs temperature**



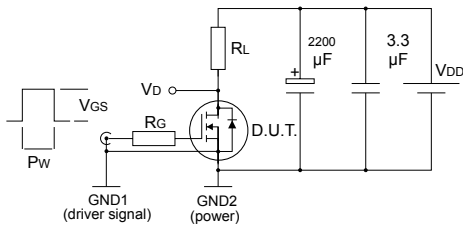
**Figure 11. Source-drain diode forward characteristics**



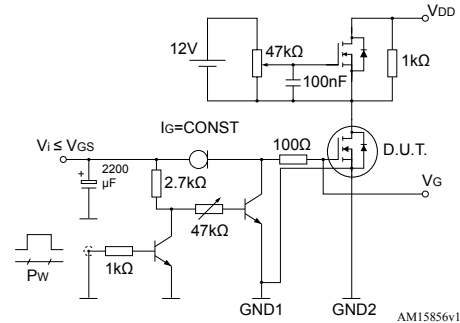
**Figure 12. Output capacitance stored energy**



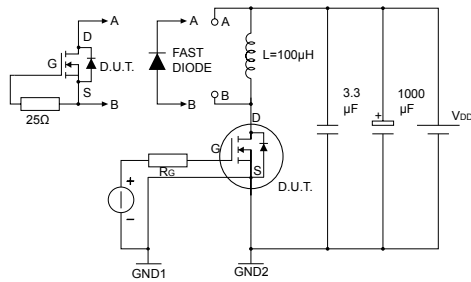
### 3 Test circuits

**Figure 13. Switching times test circuit for resistive load**


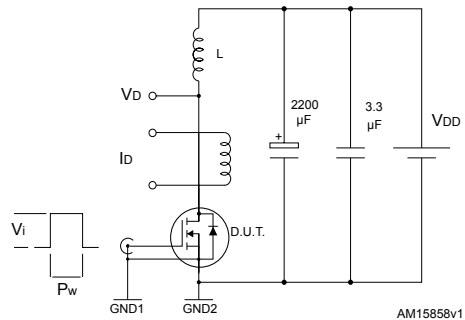
AM15855v1

**Figure 14. Test circuit for gate charge behavior**


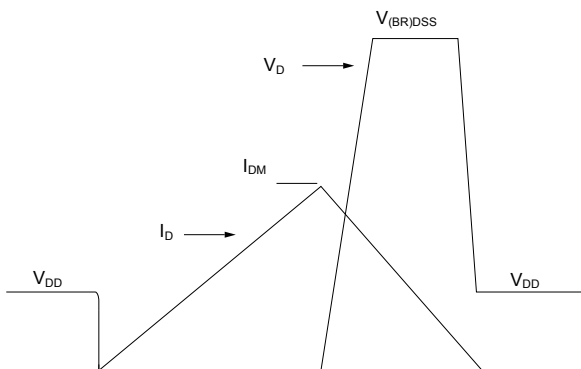
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**Figure 15. Test circuit for inductive load switching and diode recovery times**


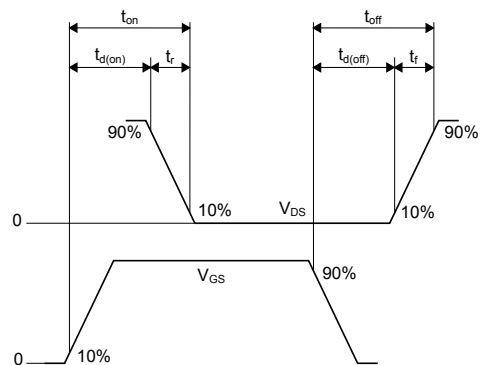
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**Figure 16. Unclamped inductive load test circuit**


AM15858v1

**Figure 17. Unclamped inductive waveform**


AM01472v1

**Figure 18. Switching time waveform**


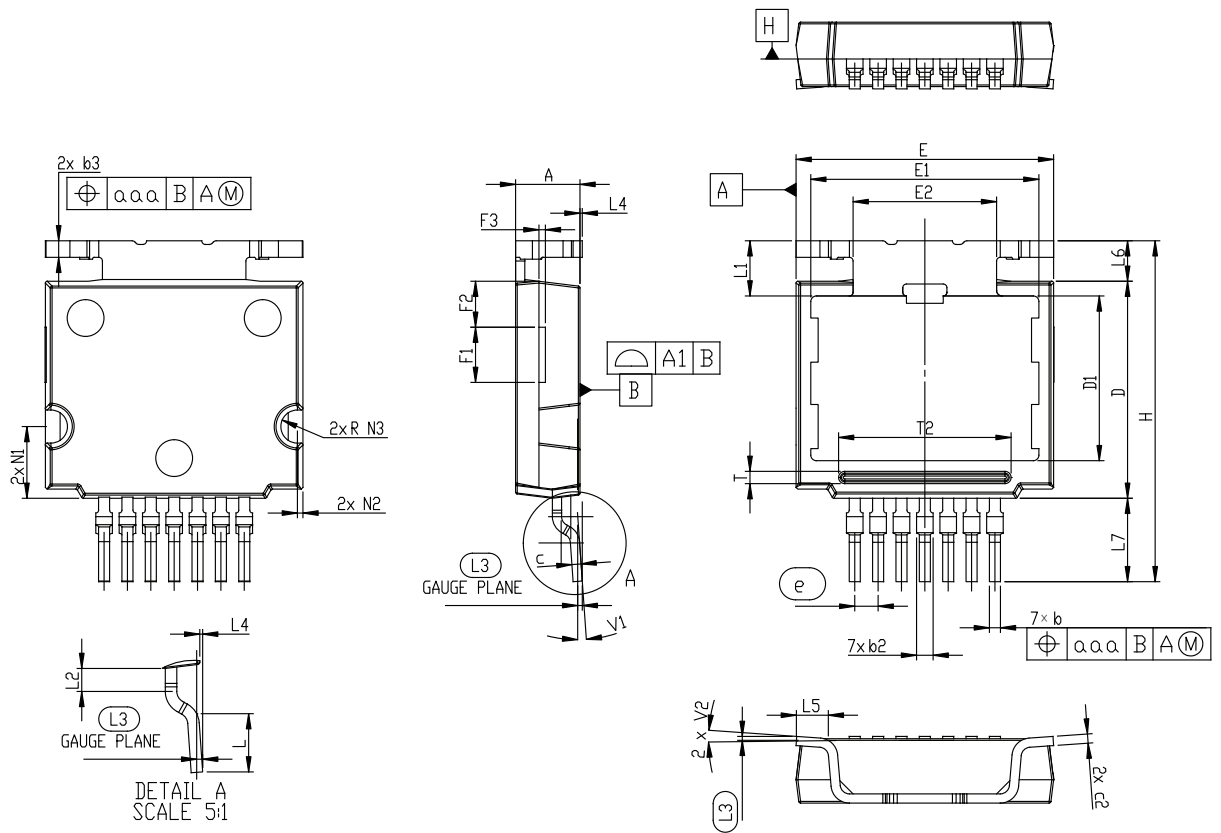
AM01473v1

## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 4.1 HU3PAK package information

Figure 19. HU3PAK package outline



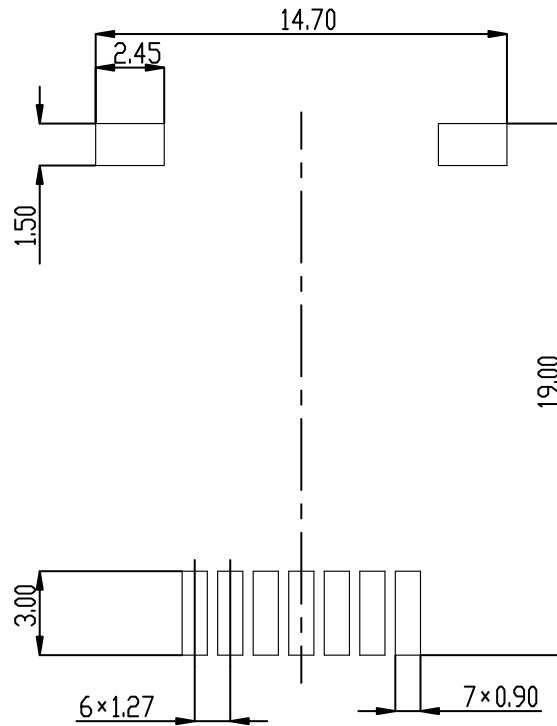
DM00674007\_2



**Table 8. HU3PAK package mechanical data**

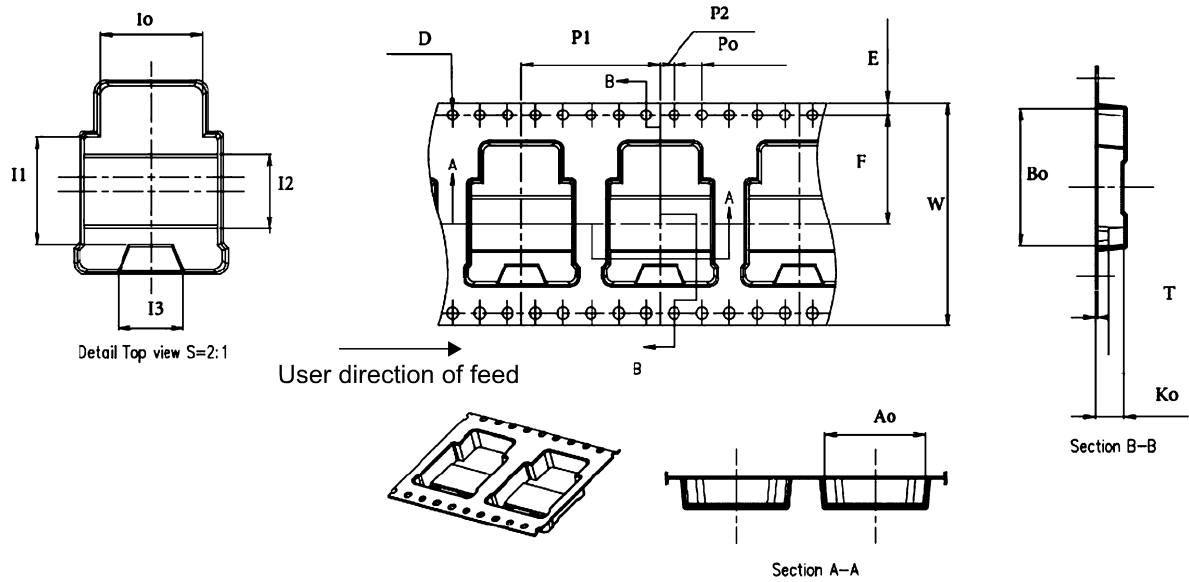
Ref.	Dimensions		
	mm		
	Min.	Typ.	Max.
A	3.40	3.50	3.60
A1		0.05	
b	0.50	0.60	0.70
b2	0.50	0.70	1.00
b3	0.80	0.90	1.00
c	0.40	0.50	0.60
c2	0.40	0.50	0.60
D	11.70	11.80	11.90
D1	8.80	8.955	9.10
E	13.90	14.00	14.10
E1	12.30	12.40	12.50
E2	7.75	7.80	7.85
e		1.27	
H	18.00	18.58	19.00
aaa		0.10	
L	2.40	2.52	2.60
L1		3.05	
L2	0.90	1.00	1.10
L3		0.26	
L4	0.075	0.125	0.175
L5	1.83	1.93	2.03
L6	2.14	2.24	2.34
L7	4.44	4.54	4.64
F1	2.90	3.00	3.10
F2	2.40	2.50	2.60
F3	0.25	0.35	0.45
N1	3.80	3.90	4.00
N2	0.25	0.30	0.45
N3	0.80	0.90	1.00
T	0.50	0.67	0.70
T2	9.18	9.38	9.43
V1		0°	8°
V2		0°	8°

Figure 20. HU3PAK recommended footprint (dimensions in mm)



## 4.2 HU3PAK packing information

Figure 21. HU3PAK carrier tape outline



DM00345054\_3

Table 9. HU3PAK tape mechanical data

Dimension	Value
	mm
A0	14.40 ±0.10
B0	19.70
D	1.50 ±0.10
E	1.75 ±0.10
F	15.65 ±0.10
I0	11.00
I1	11.60 ±0.10
I2	8.00
I3	7.00
K0	4.20
P0	4.00 ±0.10
P1	20.00 ±0.10
P2	2.00 ±0.10
T	0.40 ±0.50
W	32.00 ±0.30

Figure 22. HU3PAK reel outline

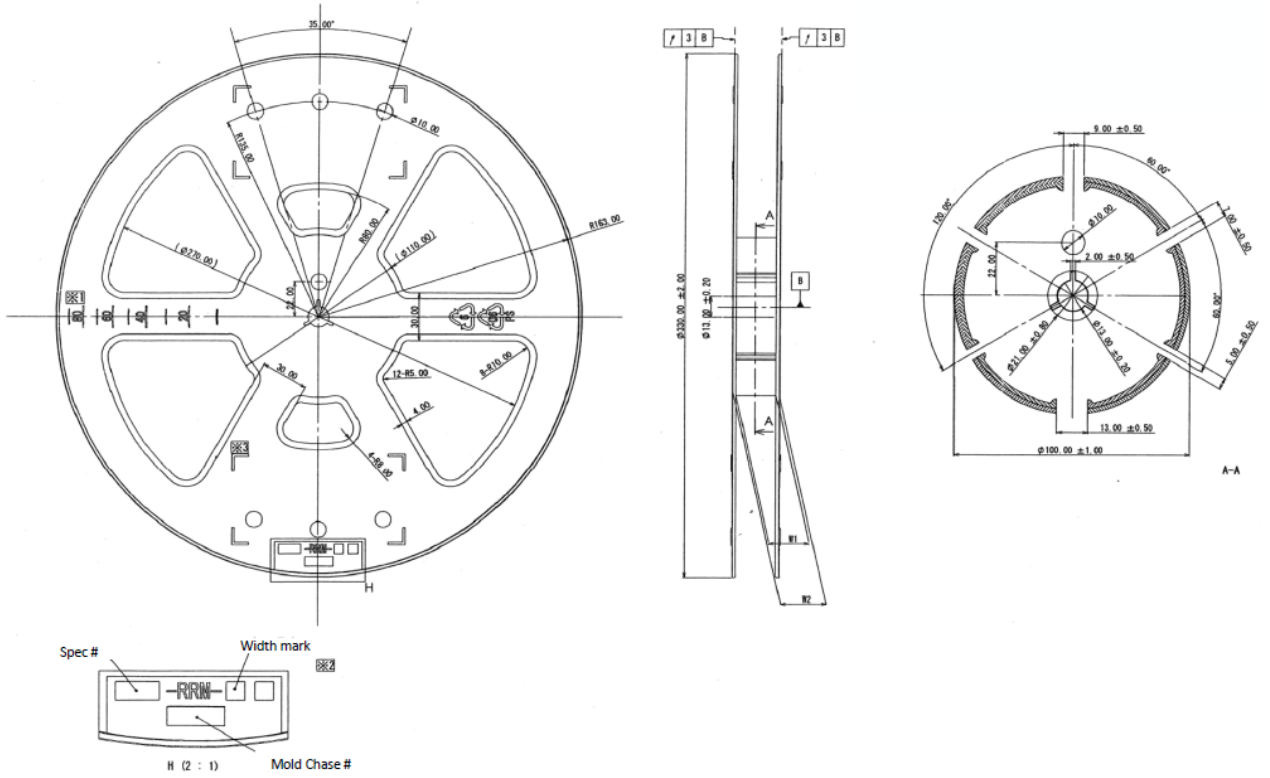


Table 10. HU3PAK reel mechanical data

Dimension	Value
	mm
Reel width	32.0
Reel inner width	33.4 ± 1.0
Reel outer width	37.4 ± 1.0

## Revision history

**Table 11. Document revision history**

Date	Revision	Changes
05-Jun-2019	1	Initial release.
06-Oct-2021	2	Modified <i>Features</i> on cover page. Modified <i>Table 1. Absolute maximum ratings</i> and <i>Table 4. On/off-state</i> . Modified <i>Section 4 Package information</i> . Minor text changes.
11-Nov-2021	3	Modified <i>Table 1. Absolute maximum ratings</i> . Modified <i>Table 8. HU3PAK package mechanical data</i> . Minor text changes.

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[STP25N10F7](#) [MJD32CT4-A](#)