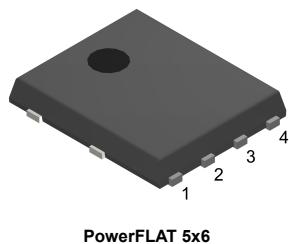
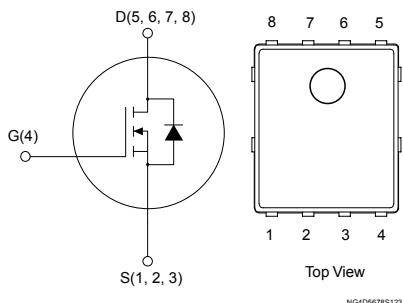


## N-channel 80 V, 5.2 mΩ typ., 100 A, STripFET F7 Power MOSFET in a PowerFLAT 5x6 package


**PowerFLAT 5x6**


NG4D5678S123

### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>	P <sub>TOT</sub>
STL100N8F7	80 V	6.1 mΩ	100 A	120 W

- Among the lowest R<sub>DS(on)</sub> on the market
- Excellent FoM (figure of merit)
- Low C<sub>rss</sub>/C<sub>iss</sub> ratio for EMI immunity
- High avalanche ruggedness

### Applications

- Switching applications

### Description

This N-channel Power MOSFET utilizes STripFET F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.



#### Product status link

[STL100N8F7](#)

#### Product summary

Order code	STL100N8F7
Marking	100N8F7
Package	PowerFLAT 5x6
Packing	Tape and reel

## 1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	80	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D$ <sup>(1)</sup>	Drain current (continuous) at $T_C = 25^\circ\text{C}$	100	A
$I_D$ <sup>(1)</sup>	Drain current (continuous) at $T_C = 100^\circ\text{C}$	71	A
$I_{DM}$ <sup>(2) (1)</sup>	Drain current (pulsed)	400	A
$I_D$ <sup>(3)</sup>	Drain current (continuous) at $T_{pcb} = 25^\circ\text{C}$	20	A
$I_D$ <sup>(3)</sup>	Drain current (continuous) at $T_{pcb} = 100^\circ\text{C}$	14	A
$I_{DM}$ <sup>(3) (2)</sup>	Drain current (pulsed)	80	A
$P_{TOT}$ <sup>(1)</sup>	Total power dissipation at $T_C = 25^\circ\text{C}$	120	W
$P_{TOT}$ <sup>(3)</sup>	Total power dissipation at $T_{pcb} = 25^\circ\text{C}$	4.8	W
$E_{AS}$ <sup>(4)</sup>	Single pulse avalanche energy	220	mJ
$T_J$	Operating junction temperature range	$-55 \text{ to } 175$	$^\circ\text{C}$
$T_{stg}$	Storage temperature range		$^\circ\text{C}$

1. This value is rated according to  $R_{thj-c}$ .
2. Pulse width limited by safe operating area.
3. This value is rated according to  $R_{thj-pcb}$ .
4. Starting  $T_J=25^\circ\text{C}$ ,  $I_D=25\text{ A}$ ,  $V_{DD}=40\text{ V}$

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	1.25	$^\circ\text{C/W}$
$R_{thj-pcb}$ <sup>(1)</sup>	Thermal resistance junction-pcb	31.3	$^\circ\text{C/W}$

1. When mounted on FR-4 board of 1inch<sup>2</sup>, 2oz Cu,  $t < 10\text{ s}$ .

## 2 Electrical characteristics

( $T_C = 25^\circ\text{C}$  unless otherwise specified)

**Table 3. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage	$V_{GS} = 0$ , $I_D = 250 \mu\text{A}$	80			V
$I_{\text{DSS}}$	Zero gate voltage drain current	$V_{GS} = 0$ , $V_{DS} = 80 \text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0$ , $V_{DS} = 80 \text{ V}$ , $T_C = 125^\circ\text{C}$ <sup>(1)</sup>			10	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0$ , $V_{GS} = \pm 20 \text{ V}$			$\pm 100$	nA
$V_{GS(\text{th})}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250 \mu\text{A}$	2.5		4.5	V
$R_{DS(\text{on})}$	Static drain-source on-resistance	$V_{GS} = 10 \text{ V}$ , $I_D = 10 \text{ A}$		5.2	6.1	$\text{m}\Omega$

1. Defined by design, not subject to production test.

**Table 4. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{GS} = 0$ , $V_{DS} = 40 \text{ V}$ , $f = 1 \text{ MHz}$	-	3435	-	pF
$C_{oss}$	Output capacitance		-	653	-	pF
$C_{rss}$	Reverse transfer capacitance		-	57	-	pF
$Q_g$	Total gate charge	$V_{DD} = 40 \text{ V}$ , $I_D = 20 \text{ A}$ ,	-	46.8	-	nC
$Q_{gs}$	Gate-source charge	$V_{GS} = 0$ to $10 \text{ V}$	-	23.4	-	nC
$Q_{gd}$	Gate-drain charge	(see Figure 13. Test circuit for gate charge behavior)	-	11.2	-	nC

**Table 5. Switching times**

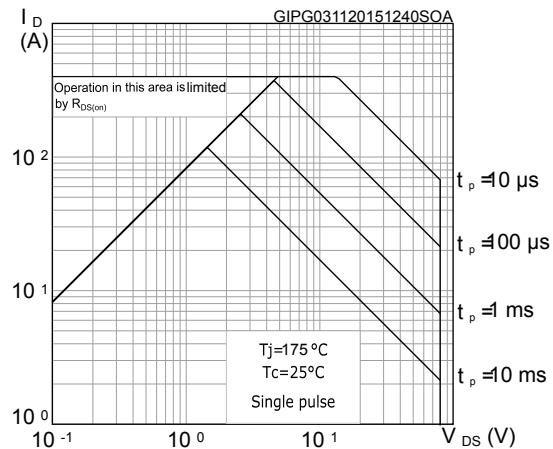
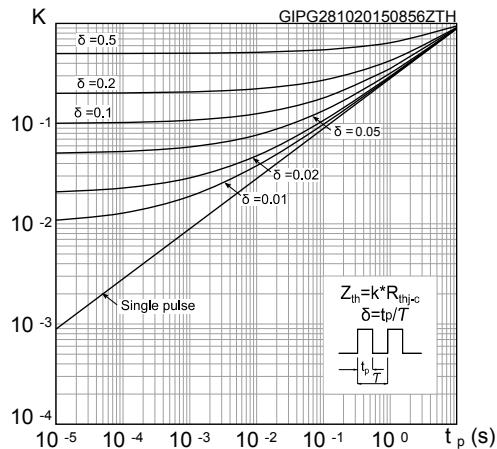
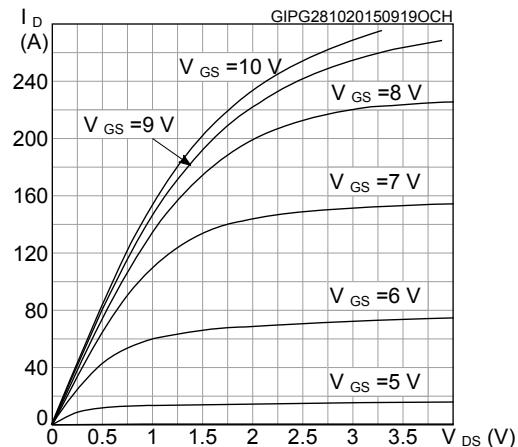
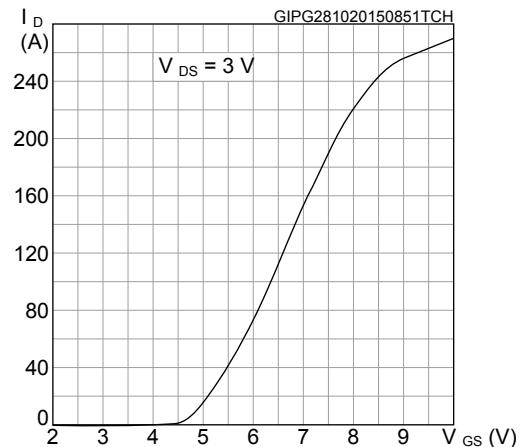
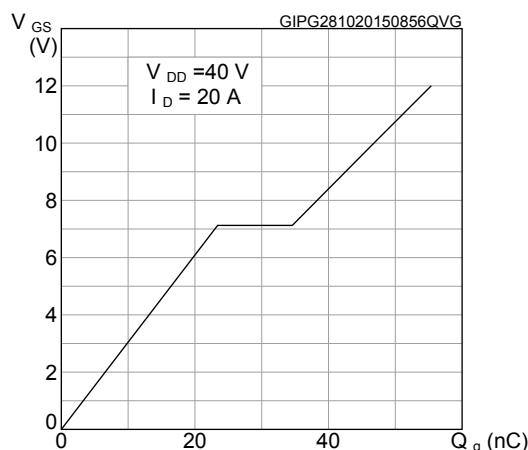
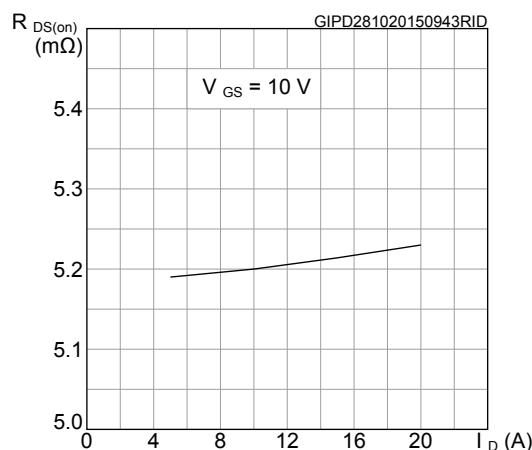
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(\text{on})}$	Turn-on delay time	$V_{DD} = 40 \text{ V}$ , $I_D = 10 \text{ A}$ , $R_G = 4.7 \Omega$ , $V_{GS} = 10 \text{ V}$	-	49	-	ns
$t_r$	Rise time	(see Figure 12. Test circuit for resistive load switching times and Figure 17. Switching time waveform)	-	95	-	ns
$t_{d(\text{off})}$	Turn-off delay time		-	60	-	ns
$t_f$	Fall time		-	32	-	ns

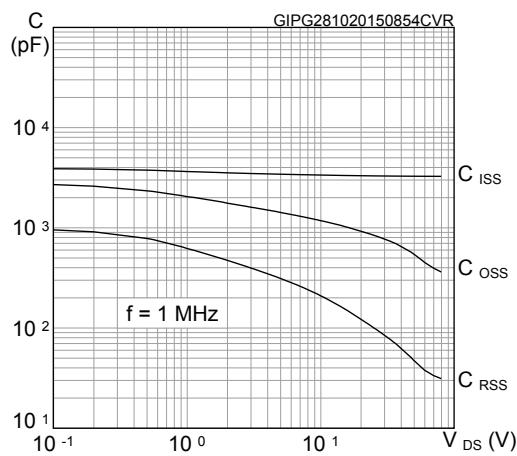
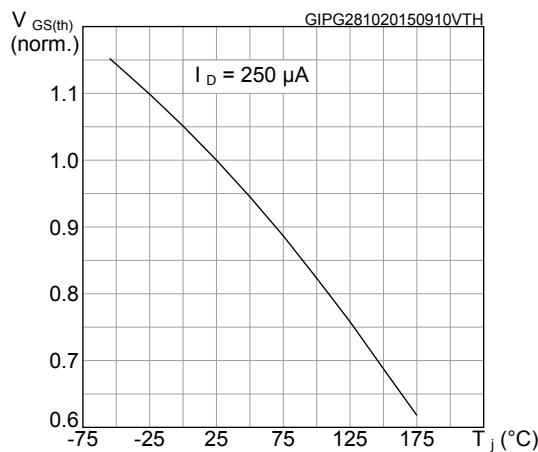
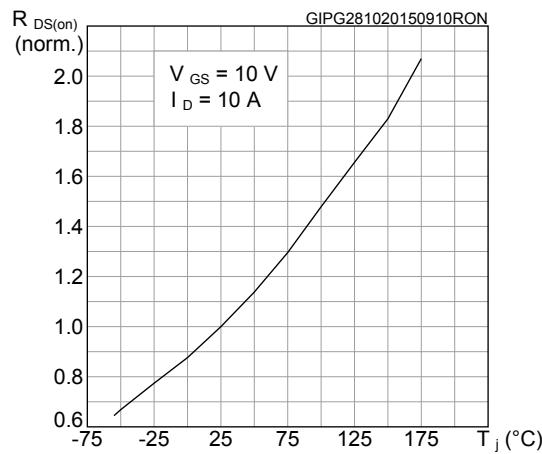
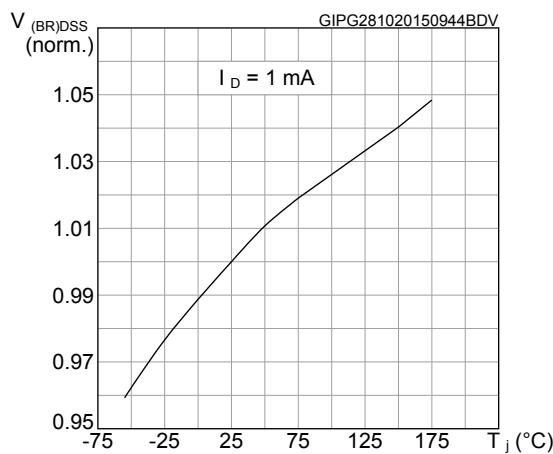
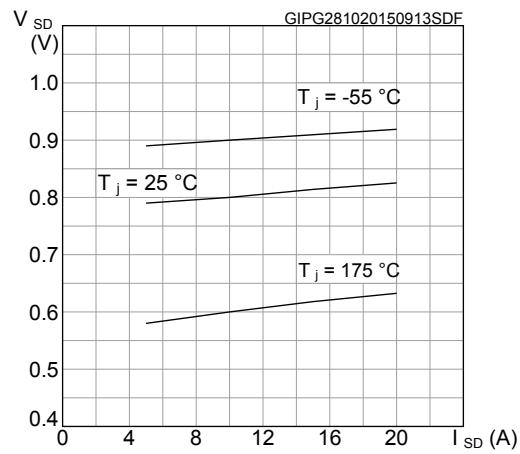
**Table 6. Source-drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>SD</sub> <sup>(1)</sup>	Forward on voltage	V <sub>GS</sub> = 0, I <sub>SD</sub> = 20 A	-		1.2	V
t <sub>rr</sub>	Reverse recovery time	I <sub>SD</sub> = 20 A, di/dt = 100 A/μs,	-	48.6		ns
Q <sub>rr</sub>	Reverse recovery charge	V <sub>DD</sub> = 60 V (see <a href="#">Figure 14. Test circuit for inductive load switching and diode recovery times.</a> )	-	58.6		nC
I <sub>RRM</sub>	Reverse recovery current		-	2.4		A

1. Pulsed: pulse duration = 300 μs, duty cycle 1.5%

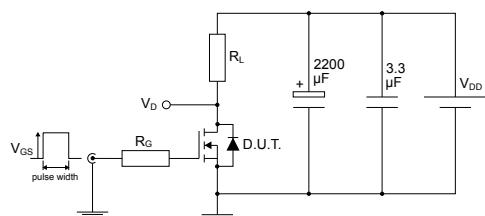
## 2.1 Electrical characteristics (curves)

**Figure 1. Safe operating area**

**Figure 2. Thermal impedance**

**Figure 3. Output characteristics**

**Figure 4. Transfer characteristics**

**Figure 5. Gate charge vs gate-source voltage**

**Figure 6. Static drain-source on-resistance**


**Figure 7. Capacitance variations**

**Figure 8. Normalized gate threshold voltage vs temperature**

**Figure 9. Normalized on-resistance vs temperature**

**Figure 10. Normalized V\_(BR)DSS vs temperature**

**Figure 11. Source-drain diode forward characteristics**


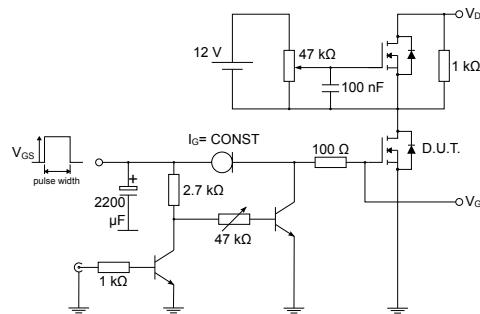
### 3 Test circuits

**Figure 12.** Test circuit for resistive load switching times



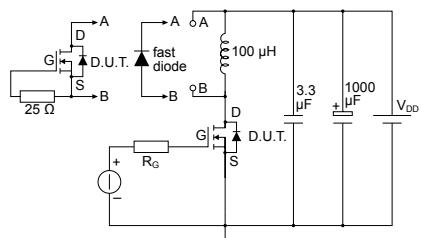
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**Figure 13.** Test circuit for gate charge behavior



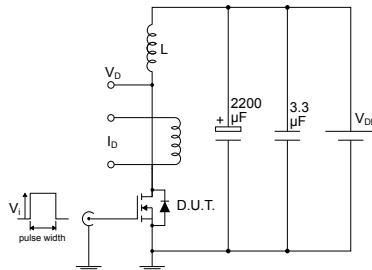
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**Figure 14.** Test circuit for inductive load switching and diode recovery times



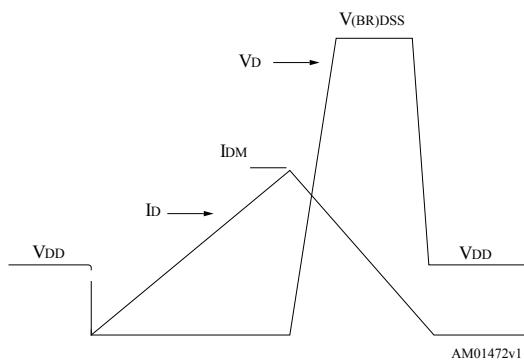
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**Figure 15.** Unclamped inductive load test circuit



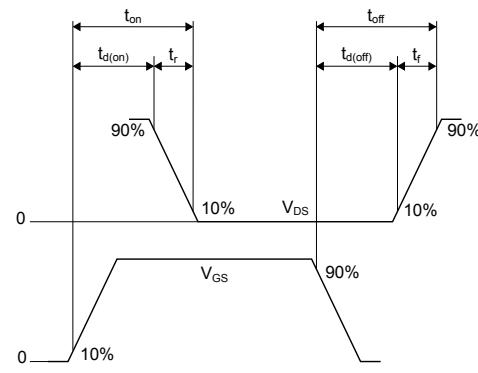
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**Figure 16.** Unclamped inductive waveform



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**Figure 17.** Switching time waveform



AM01473v1

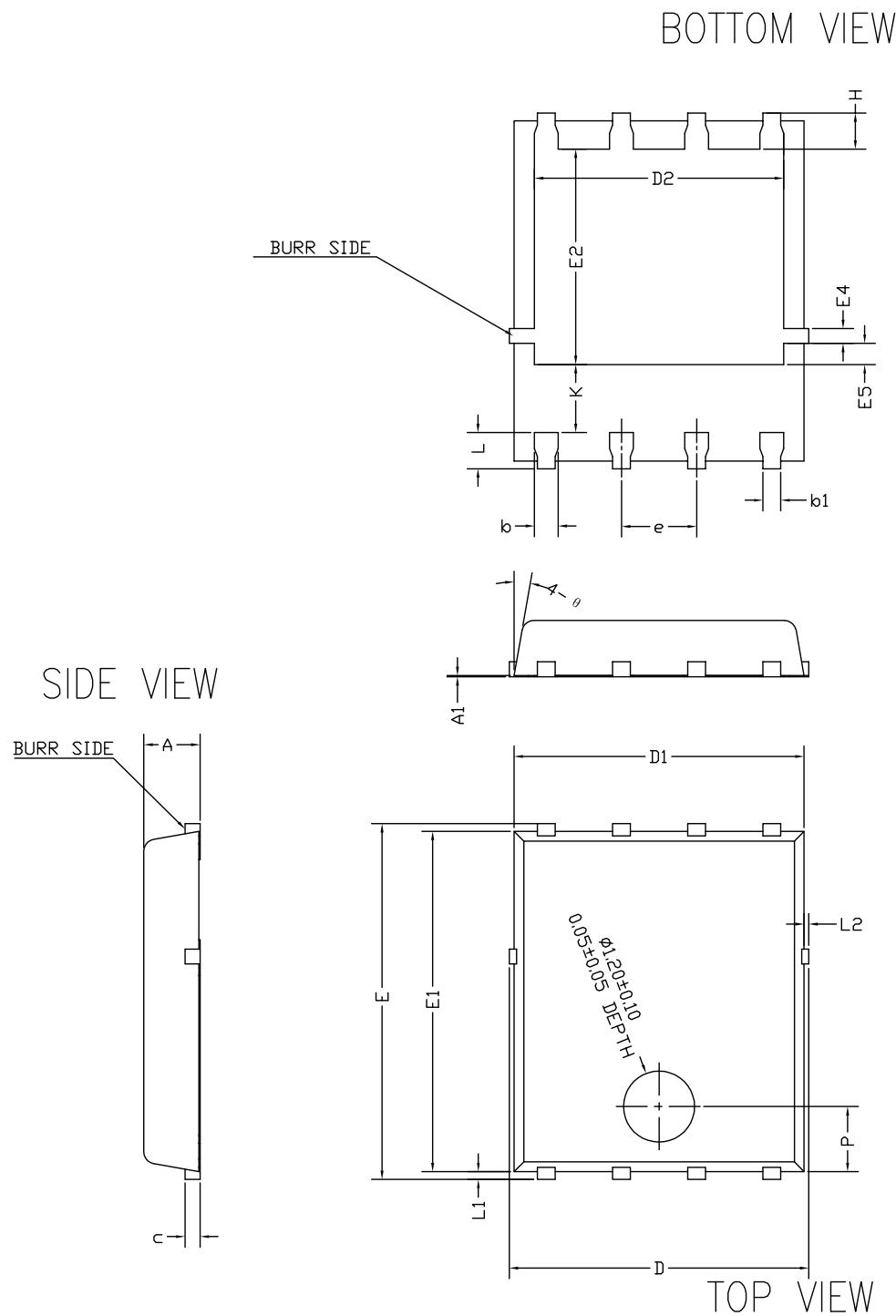
## 4

## Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

## 4.1 PowerFLAT 5x6 type C SUBCON package information

Figure 18. PowerFLAT 5x6 type C SUBCON package outline



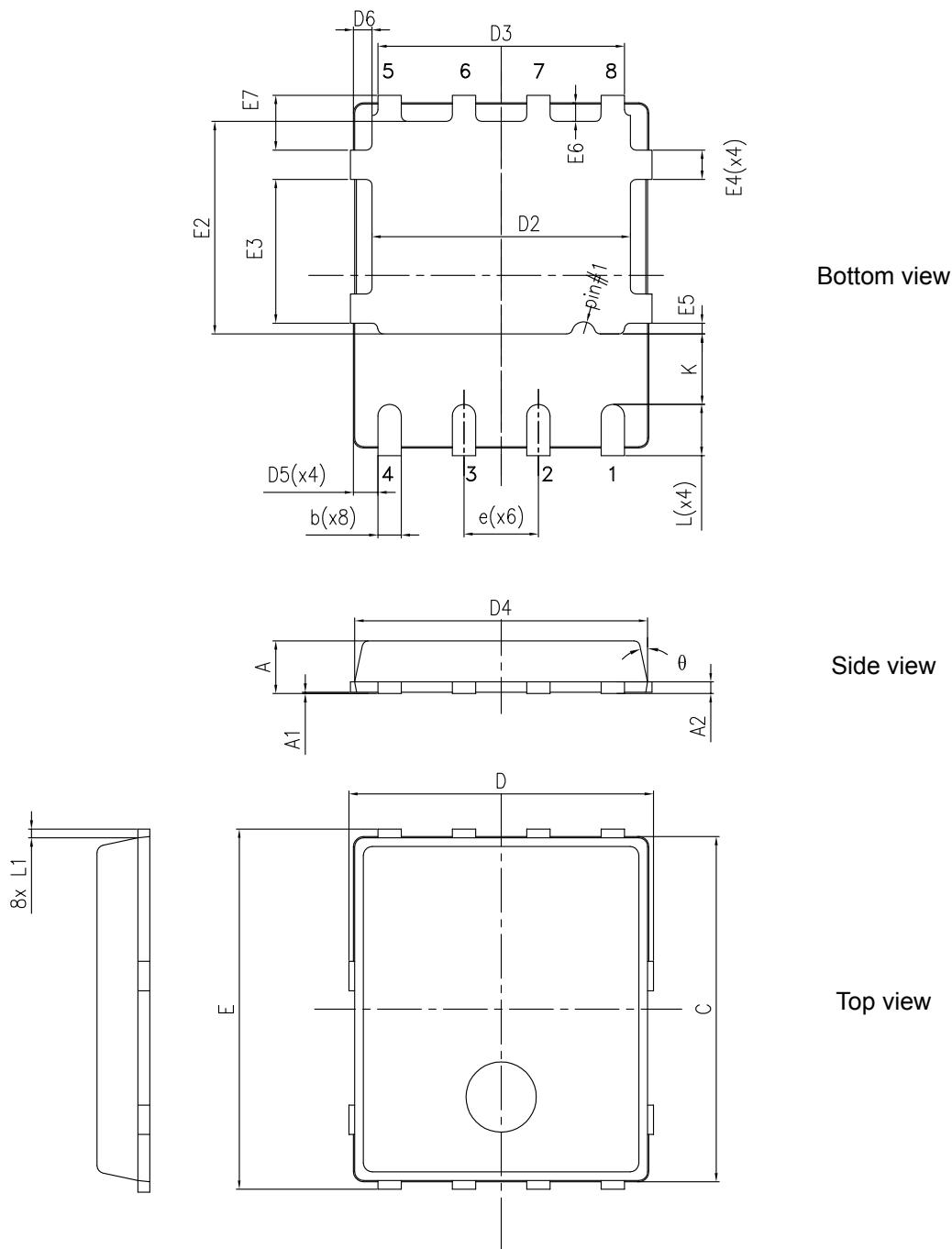
8472137\_SUBCON\_998G\_REV4

**Table 7. PowerFLAT 5x6 type C SUBCON package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	0.90	0.95	1.00
A1		0.02	
b	0.35	0.40	0.45
b1		0.30	
c	0.21	0.25	0.34
D			5.10
D1	4.80	4.90	5.00
D2	4.01	4.21	4.31
e	1.17	1.27	1.37
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.54	3.64	3.74
E4	0.15	0.25	0.35
E5	0.26	0.36	0.46
H	0.51	0.61	0.71
K	0.95		
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
L2			0.10
P	1.00	1.10	1.20
θ	8°	10°	12°

## 4.2 PowerFLAT 5x6 type C package information

Figure 19. PowerFLAT 5x6 type C package outline

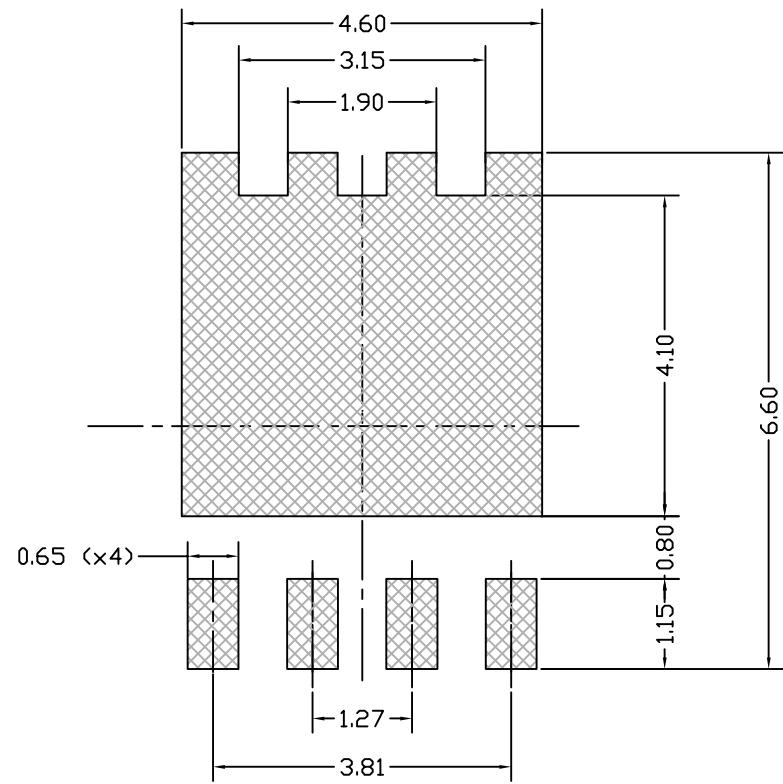


8231817\_typeC\_Rev18

**Table 8. PowerFLAT 5x6 type C package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.80	6.00	6.20
D	5.00	5.20	5.40
D2	4.15		4.45
D3	4.05	4.20	4.35
D4	4.80	5.00	5.20
D5	0.25	0.40	0.55
D6	0.15	0.30	0.45
e		1.27	
E	5.95	6.15	6.35
E2	3.50		3.70
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28
E6	0.20	0.325	0.45
E7	0.75	0.90	1.05
K	1.05		1.35
L	0.725		1.025
L1	0.05	0.15	0.25
θ	0°		12°

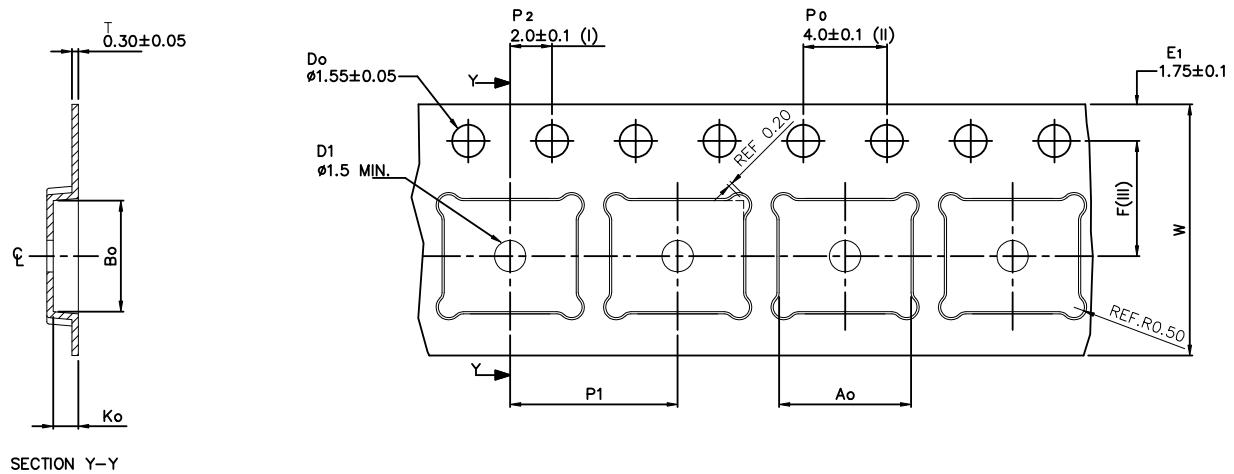
**Figure 20. PowerFLAT 5x6 recommended footprint (dimensions are in mm)**



8231817\_FOOTPRINT\_simp\_Rev\_18

## 4.3 PowerFLAT 5x6 packing information

**Figure 21.** PowerFLAT 5x6 tape (dimensions are in mm)



SECTION Y-Y

$A_o$	$6.30 \pm 0.1$
$B_o$	$5.30 \pm 0.1$
$K_o$	$1.20 \pm 0.1$
$F$	$5.50 \pm 0.1$
$P_1$	$8.00 \pm 0.1$
$W$	$12.00 \pm 0.3$

(I) Measured from centreline of sprocket hole to centreline of pocket.

Base and bulk quantity 3000 pcs  
All dimensions are in millimeters

(II) Cumulative tolerance of 10 sprocket holes is  $\pm 0.20$ .

(III) Measured from centreline of sprocket hole to centreline of pocket

8234350\_Tape\_rev\_C

**Figure 22.** PowerFLAT 5x6 package orientation in carrier tape

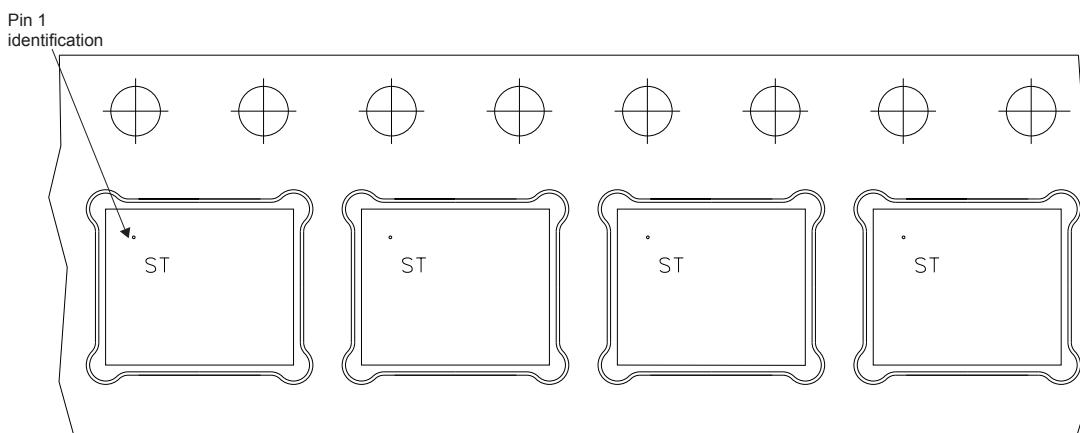
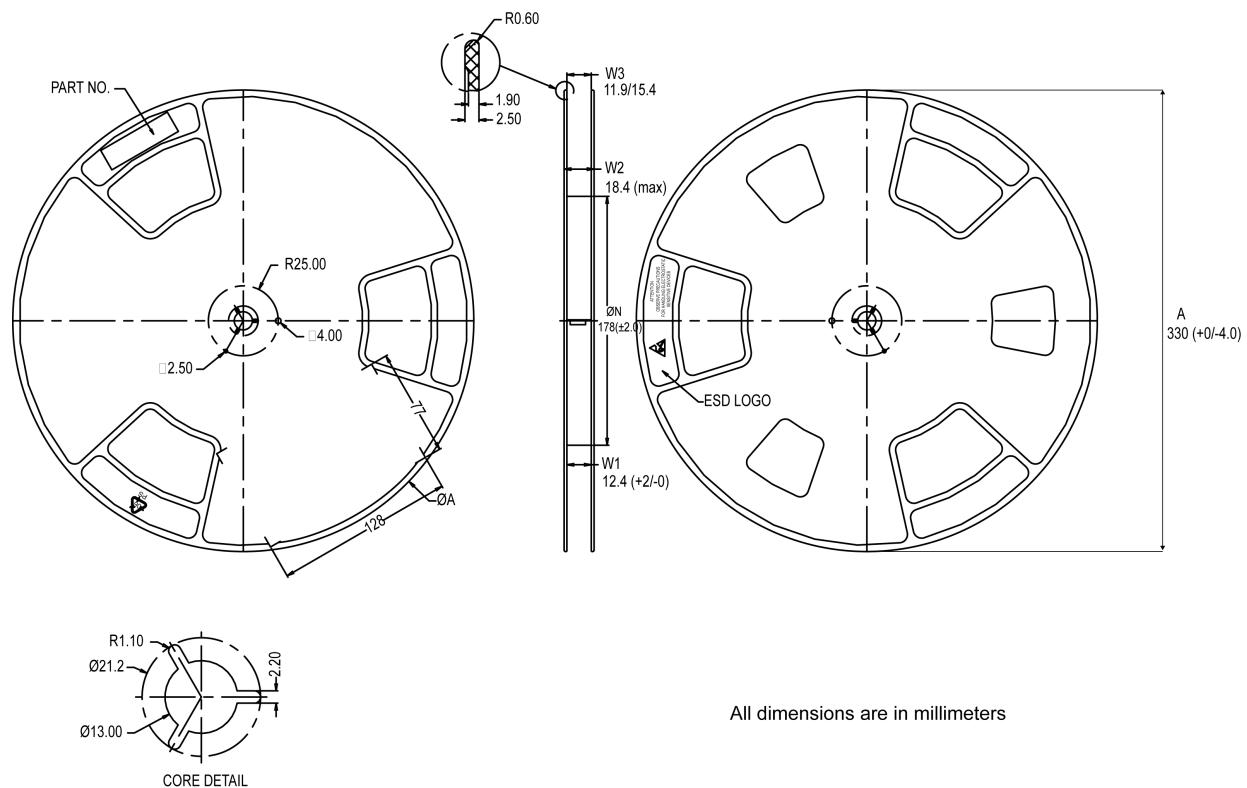


Figure 23. PowerFLAT 5x6 reel



8234350\_Reel\_rev\_C

## Revision history

**Table 9. Document revision history**

Date	Revision	Changes
21-Oct-2014	1	Initial release.
03-Nov-2015	2	Modified: Table 2: "Absolute maximum ratings" , Table 5: "Dynamic", Table 6: "Switching times" and Table 7: "Source drain diode". Added: Section 4.1: "Electrical characteristics (curves)". Minor text changes
03-Dec-2015	3	Document status promoted from preliminary to production data.
27-Nov-2019	4	Added <a href="#">Section 4.1 PowerFLAT 5x6 type C SUBCON package information</a> . Updated <a href="#">Section 4.2 PowerFLAT 5x6 type C package information</a> . Minor text changes.

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