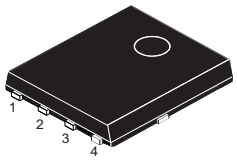
STL105NS3LLH7

N-channel 30 V, 0.0033 Ω typ., 27 A STripFET™ H7 Power MOSFET plus monolithic Schottky in a PowerFLAT™ 5x6

Datasheet - production data



PowerFLAT™5x6

Features

Order code	V_{DS}	$R_{DS(on)}$ max	I_D
STL105NS3LLH7	30 V	0.0039 Ω	27 A

- Very low on-resistance
- Very low Q_g
- Avalanche high ruggedness
- Embedded Schottky diode

Applications

- Switching applications

Description

This device exhibits low on-state resistance and capacitance for improved conduction and switching performance.

Figure 1. Internal schematic diagram

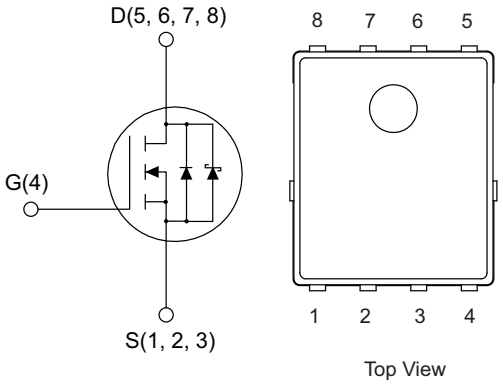


Table 1. Device summary

Order code	Marking	Package	Packaging
STL105NS3LLH7	105NS3LL	PowerFLAT™ 5x6	Tape and reel

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	30	V
V_{GS}	Gate-source voltage	± 20	V
I_D(1)	Drain current (continuous) at T_C = 25 °C	105	A
I_D(1)	Drain current (continuous) at T_C = 100 °C	65	A
I_{DM}(1)(2)	Drain current (pulsed)	420	A
I_D(3)	Drain current (continuous) at T_{pcb} = 25 °C	27	A
I_D(3)	Drain current (continuous) at T_{pcb} = 100 °C	16	A
I_{DM}(2)(3)	Drain current (pulsed)	108	A
P_{TOT}(1)	Total dissipation at T_C = 25 °C	62.5	W
P_{TOT}(2)	Total dissipation at T_{pcb} = 25 °C	4	W
T_{stg}	Storage temperature	-55 to 150	°C
T_j	Operating junction temperature		

1. This value is rated according to $R_{thj\text{-}c}$
2. Pulse width limited by safe operating area.
3. This value is rated according to $R_{thj\text{-}pcb}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}pcb}$(1)	Thermal resistance junction-pcb max	31.3	°C/W
$R_{thj\text{-}case}$	Thermal resistance junction-case max	2	°C/W

1. When mounted on FR-4 board of 1 inch², 2oz Cu, t < 10 sec

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0 V	30			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V V_{DS} = 24 V			500	µA
I_{GSS}	Gate-body leakage current	V_{GS} = ± 20 V, V_{DS} = 0 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 1 mA	1.2			V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 13.5 A		0.0033	0.0039	Ω
		V_{GS} = 4.5 V, I_D = 13.5 A		0.0044	0.0055	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0 V	-	2110	-	pF
C_{oss}	Output capacitance		-	640	-	pF
C_{rss}	Reverse transfer capacitance		-	42	-	pF
Q_g	Total gate charge	V_{DD} = 15 V, I_D = 27 A, V_{GS} = 4.5 V (see *Figure 11*)	-	13.7	-	nC
Q_{gs}	Gate-source charge		-	7.5	-	nC
Q_{gd}	Gate-drain charge		-	3.3	-	nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 15 V, I_D = 13.5 A, R_G = 4.7 Ω, V_{GS} = 4.5 V	-	26.4	-	ns
t_r	Rise time		-	10.4	-	ns
$t_{d(off)}$	Turn-off delay time		-	31.8	-	ns
t_f	Fall time		-	12.5	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		27	A
I_{SDM} (1)	Source-drain current (pulsed)		-		108	A
V_{SD} (2)	Forward on voltage	I_{SD} = 2 A, V_{GS} = 0 V	-	0.4	0.7	V
t_{rr}	Reverse recovery time	I_D = 2 A, di/dt = 100 A/µs V_{DD} = 20 V	-	35.2		ns
Q_{rr}	Reverse recovery charge		-	26.4		nC
I_{RRM}	Reverse recovery current		-	1.5		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

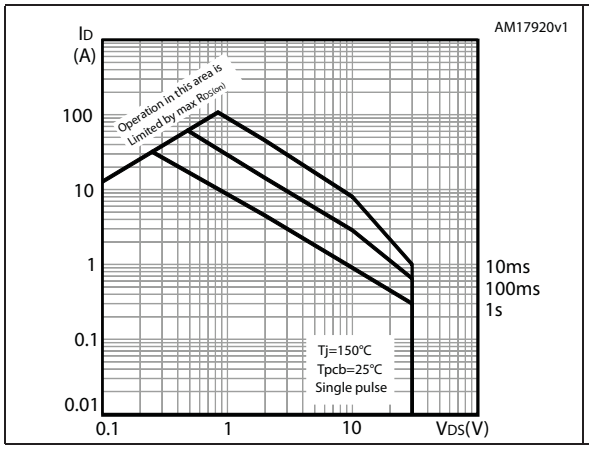


Figure 3. Thermal impedance

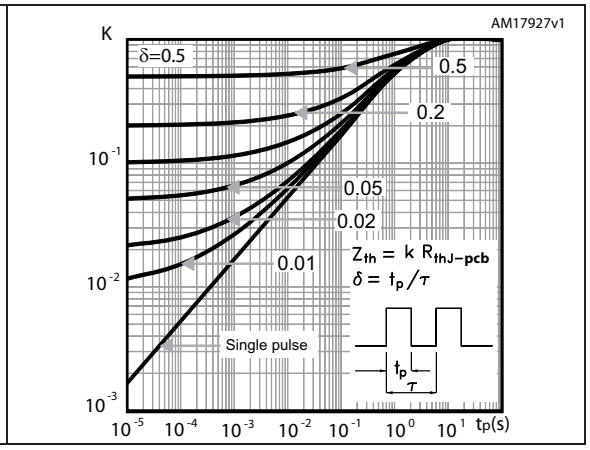


Figure 4. Output characteristics

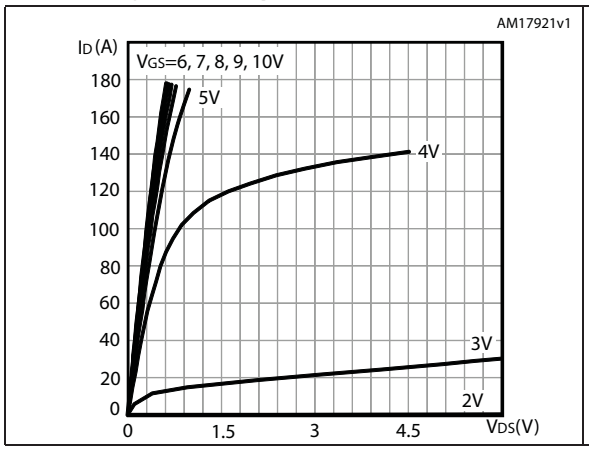


Figure 5. Transfer characteristics

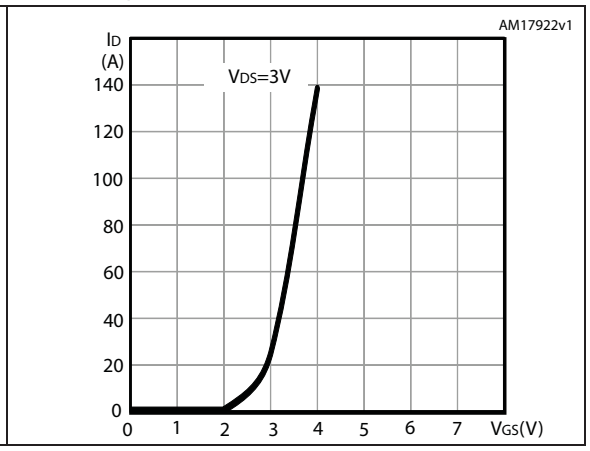


Figure 6. Gate charge vs gate-source voltage

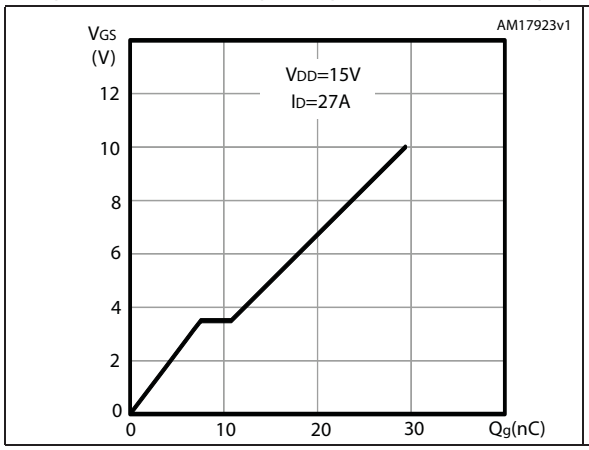


Figure 7. Static drain-source on-resistance

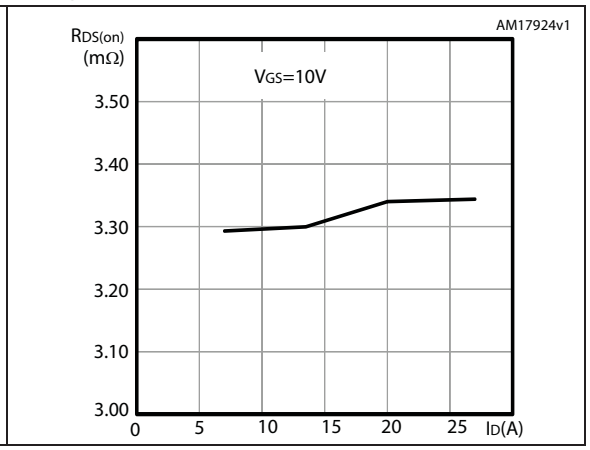


Figure 8. Capacitance variations

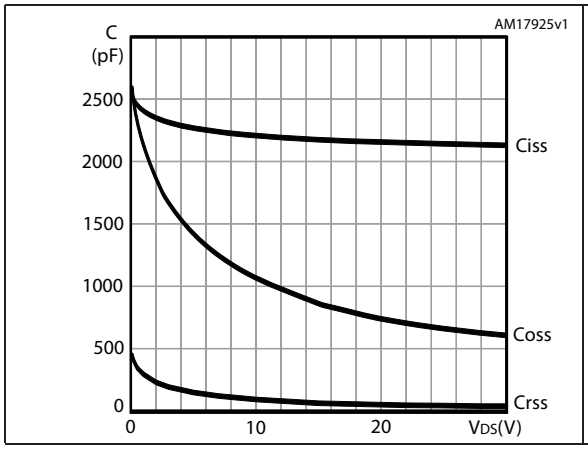
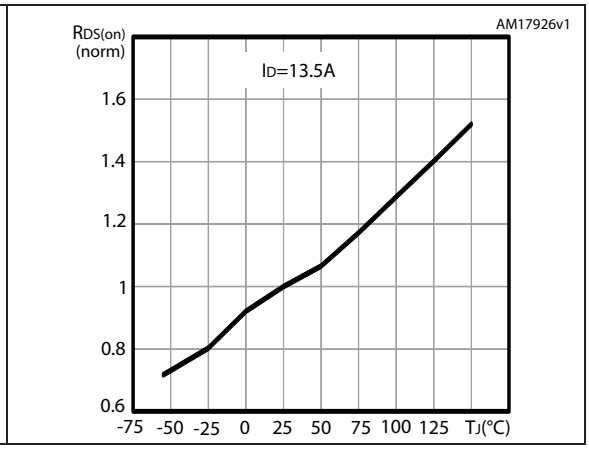


Figure 9. Normalized on-resistance vs temperature



3 Test circuits

Figure 10. Switching times test circuit for resistive load

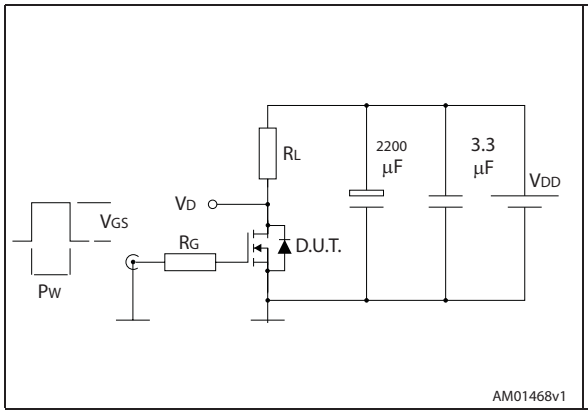


Figure 11. Gate charge test circuit

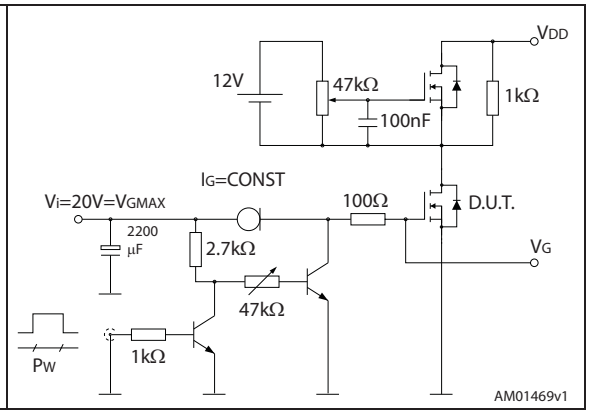


Figure 12. Test circuit for inductive load switching and diode recovery times

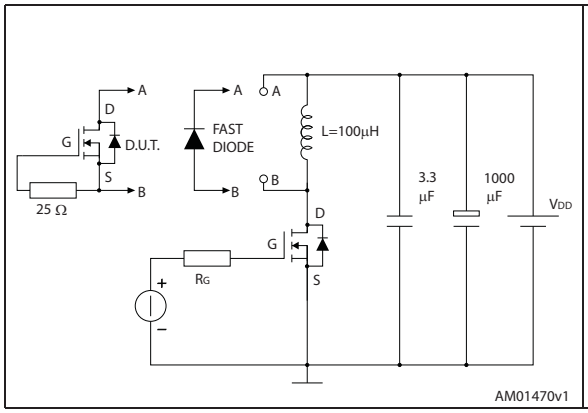


Figure 13. Unclamped inductive load test circuit

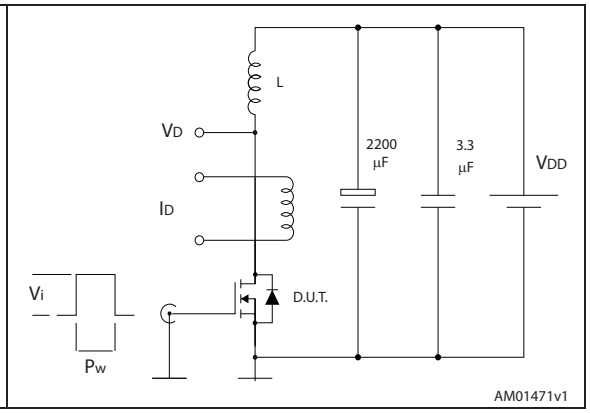


Figure 14. Unclamped inductive waveform

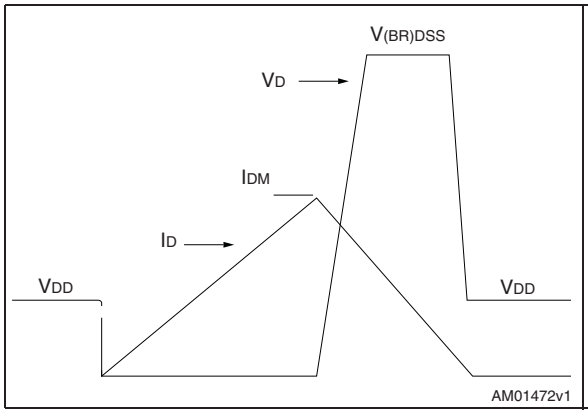
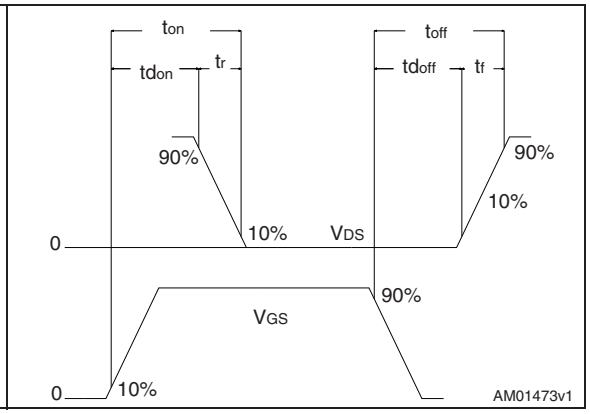


Figure 15. Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 16. PowerFLAT™ 5x6 type F outline

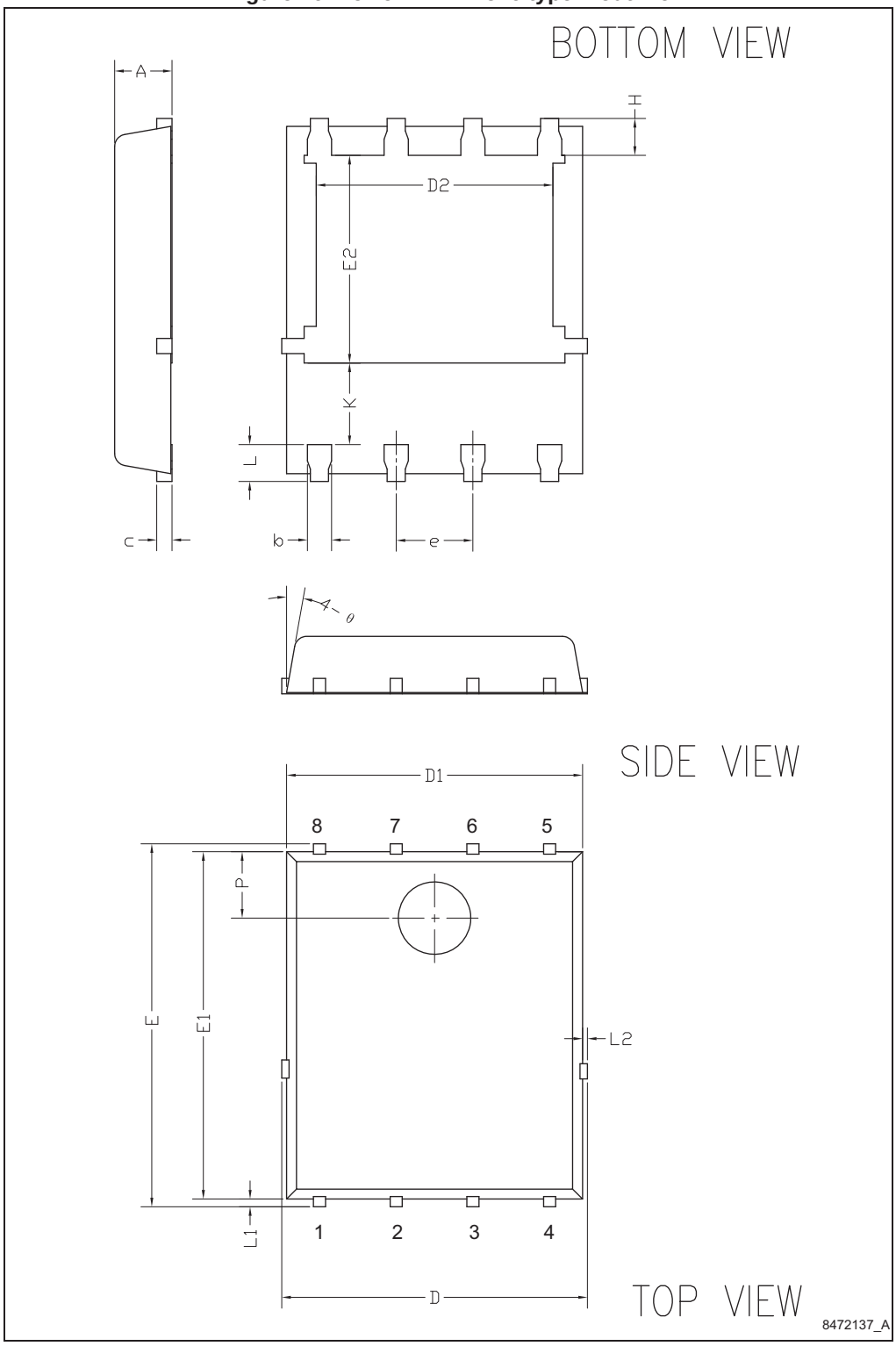
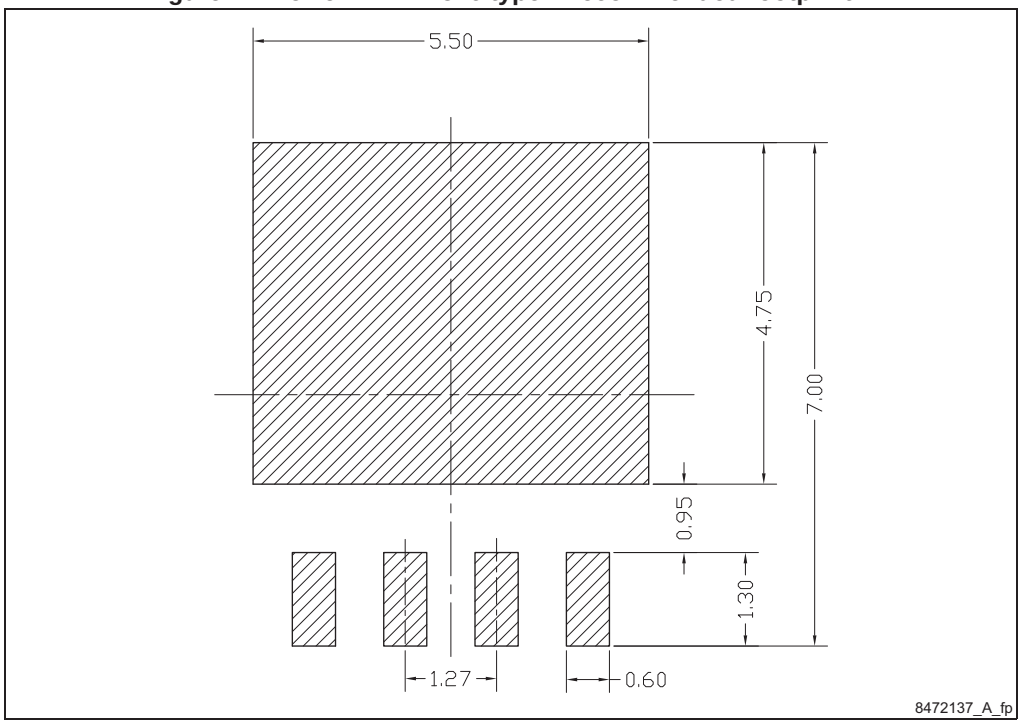


Table 8. PowerFLAT™ 5x6 type F package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.90	0.95	1.00
b	0.35	0.40	0.45
c	0.21	0.25	0.34
D			5.10
D1	4.80	4.90	5.00
D2	3.91	4.01	4.11
e	1.17	1.27	1.37
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.34	3.44	3.54
H	0.51	0.61	0.71
K	1.10		
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
L2			0.10
P	1.00	1.10	1.20
Θ	8°	10°	12°

Figure 17. PowerFLAT™ 5x6 type F recommended footprint(a)



a. All dimensions are in mm.

5 Packing information

Figure 18. PowerFLAT™ 5x6 tape(b)

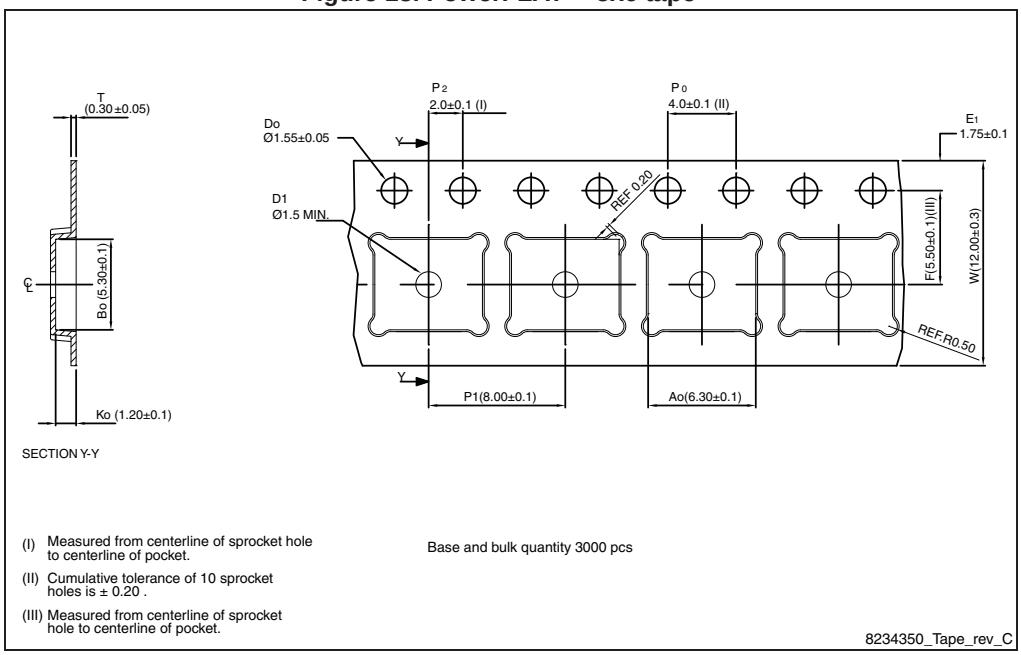
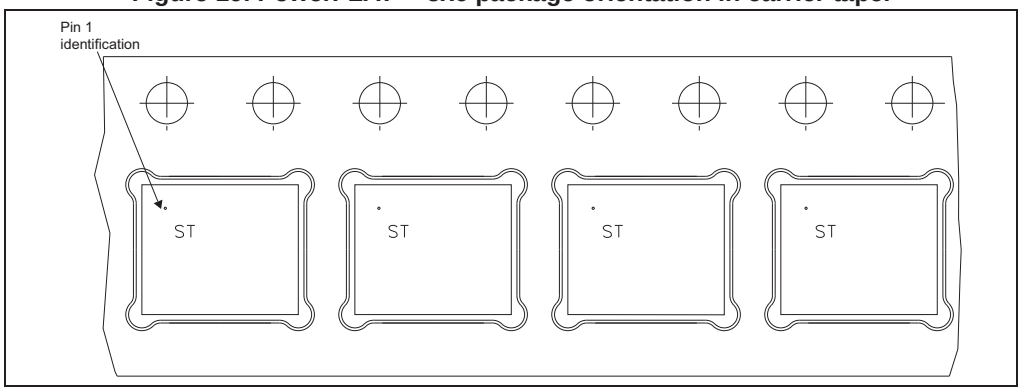
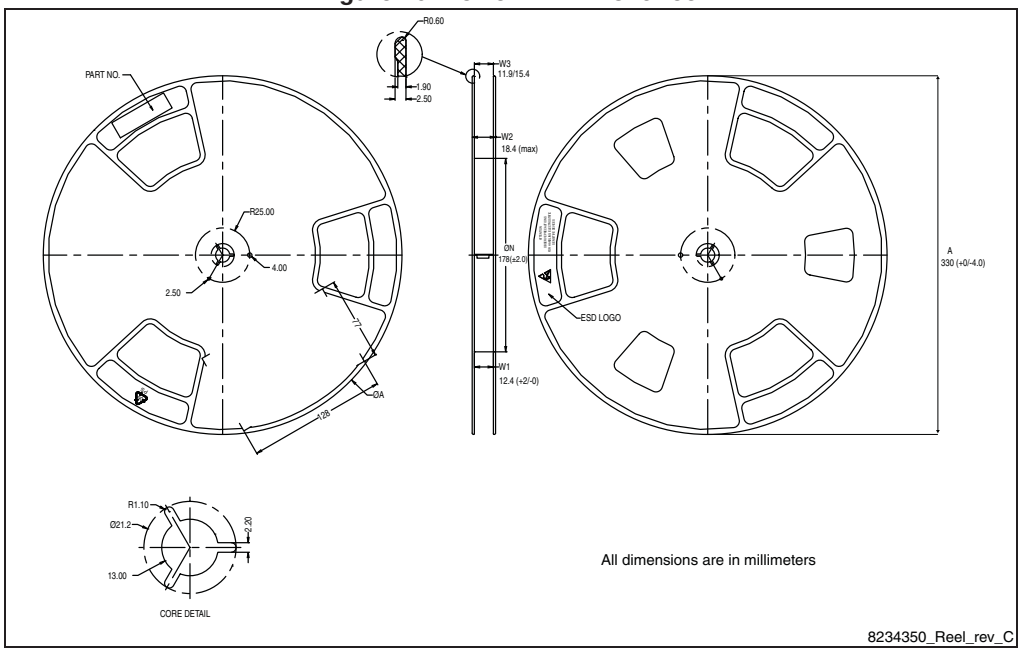


Figure 19. PowerFLAT™ 5x6 package orientation in carrier tape.



b. All dimensions are in millimeters.

Figure 20. PowerFLAT™ 5x6 reel



6 Revision history

Table 9. Document revision history

Date	Revision	Changes
07-May-2013	1	First release.
11-Jun-2013	2	– Changed: *Description* – Minor text changes
22-Nov-2013	3	– Modified: I_D (at T_C = 100 °C) and I_D (at T_{pcb} = 100 °C) in *Table 2* – Modified: P_{TOT} and T_J values in *Table 2* – Modified: $R_{DS(on)}$ values in *Table 4* – Modified: the entire typical values in *Table 5*, *6* and *7* – Added:*Section 2.1: Electrical characteristics (curves)* – Minor text changes
13-Apr-2015	4	– Document status promoted from preliminary to production data. – Minor text changes.

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