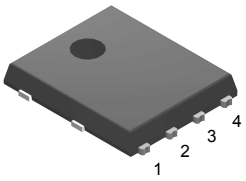
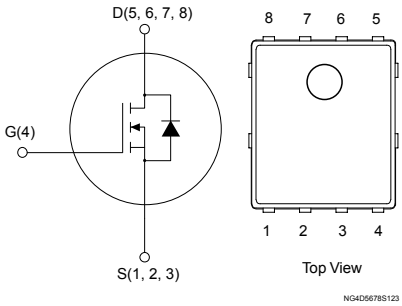
STL120N4LF6AG

Datasheet

Automotive-grade N-channel 40 V, 3.0 mΩ typ., 55 A STripFET F6 Power MOSFET in a PowerFLAT 5x6 package



PowerFLAT 5x6



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STL120N4LF6AG	40 V	3.6 mΩ	55 A	96 W

- AEC-Q101 qualified
- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss
- Wettable flank package

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the STripFET F6 technology with a new trench gate structure. The resulting Power MOSFET exhibits very low $R_{DS(on)}$ in all packages.

Product status link
STL120N4LF6AG

Product summary	
Order code	STL120N4LF6AG
Marking	120N4LF6
Package	PowerFLAT 5x6
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	40	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (continuous) at T_C = 25 °C	55	A
	Drain current (continuous) at T_C = 100 °C	55	
I_{DM} (2)	Drain current (pulsed)	220	A
P_{TOT}	Total power dissipation at T_C = 25 °C	96	W
T_{stg}	Storage temperature range	- 55 to 175	°C
T_J	Operating junction temperature range		°C

1. *Drain current is limited by package, the current capability of the silicon is 120 A at 25 °C.*
2. *Pulse width is limited by safe operating area.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	1.56	°C/W
R_{thJB} (1)	Thermal resistance, junction-to-board	31.3	°C/W

1. *When mounted on 1 inch² 2 Oz. Cu board, t ≤ 10 s.*

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AV}	Avalanche current, repetitive or not repetitive (pulse width limited by maximum junction temperature)	26	A
E_{AS}	Single pulse avalanche energy (T_J = 25 °C, I_C = I_{AV}, V_{DD} = 25 V)	200	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 250 µA	40			V
I_{DSS}	Zero gate voltage Drain current	V_{GS} = 0 V, V_{DS} = 40 V			1	µA
		V_{GS} = 0 V, V_{DS} = 40 V, T_J = 125 °C(1)			10	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	1		3	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 13 A		3.0	3.6	mΩ
		V_{GS} = 5 V, I_D = 13 A		3.2	4.5	

1. *Defined by design, not subject to production test.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0 V	-	4260	-	pF
C_{oss}	Output capacitance		-	647	-	pF
C_{rss}	Reverse transfer capacitance		-	373	-	pF
Q_g	Total gate charge	V_{DD} = 20 V, I_D = 26 A, V_{GS} = 10 V (see Figure 13. Test circuit for gate charge behavior)	-	80	-	nC
Q_{gs}	Gate-source charge		-	15	-	nC
Q_{gd}	Gate-drain charge		-	15	-	nC
R_G	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	-	1.5	-	Ω

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 20 V, I_D = 13 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 12. Test circuit for resistive load switching times and Figure 17. Switching time waveform)	-	20	-	ns
t_r	Rise time		-	70	-	ns
$t_{d(off)}$	Turn-off-delay time		-	40	-	ns
t_f	Fall time		-	20	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} (1)	Source-drain current		-		26	A
I_{SDM} (2)	Source-drain current (pulsed)		-		104	A
V_{SD} (3)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 13 A	-		1.1	V
t_{rr}	Reverse recovery time	I_{SD} = 26 A, di/dt = 100 A/µs, V_{DD} = 25 V (see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	40		ns
Q_{rr}	Reverse recovery charge		-	5.6		nC
I_{RRM}	Reverse recovery current		-	2.8		A

1. *This value is rated according to R_{thJB}.*
2. *Pulse width is limited by safe operating area.*
3. *Pulse test: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

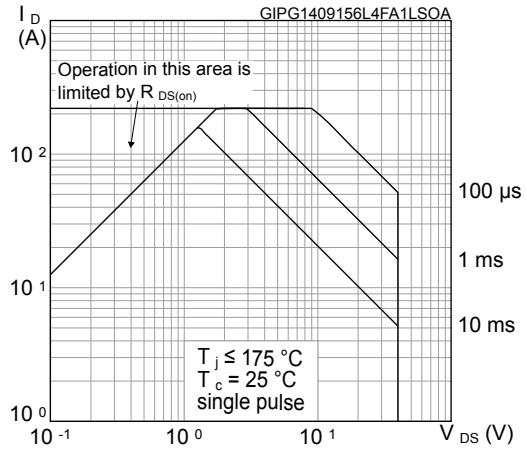


Figure 2. Thermal impedance

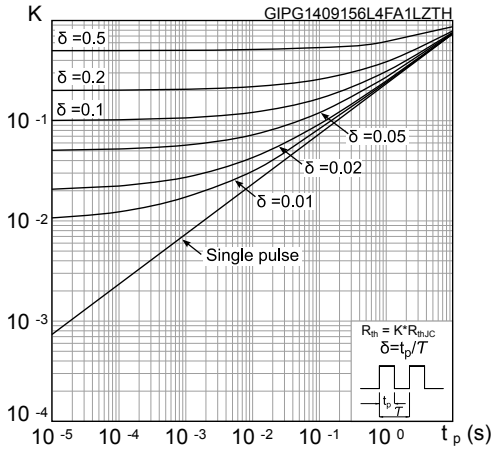


Figure 3. Output characteristics

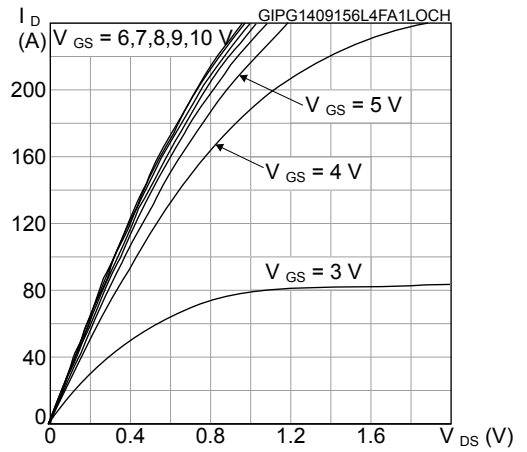


Figure 4. Transfer characteristics

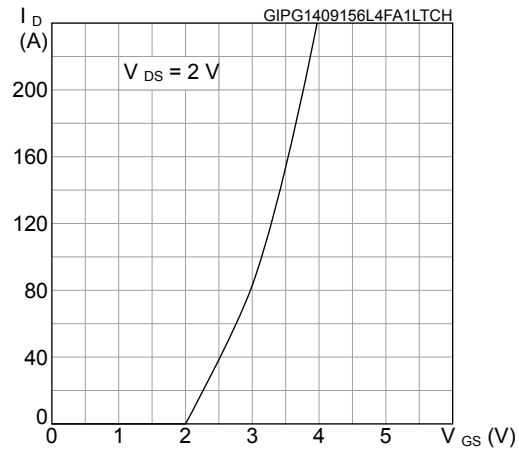


Figure 5. Gate charge vs gate-source voltage

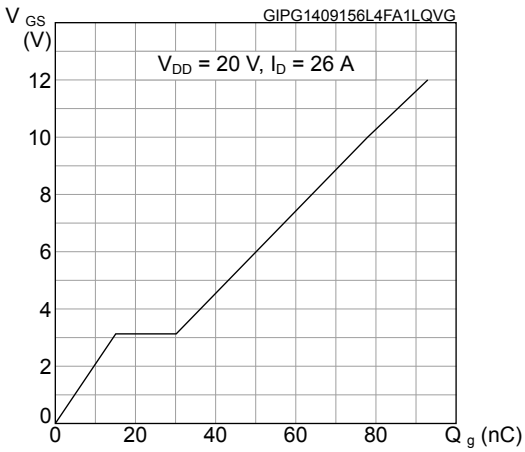


Figure 6. Static drain-source on-resistance

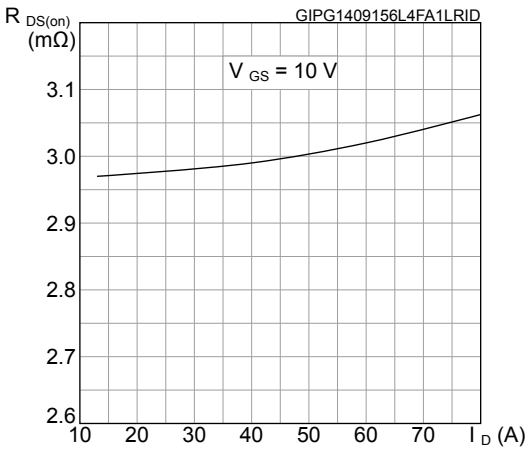


Figure 7. Capacitance variations

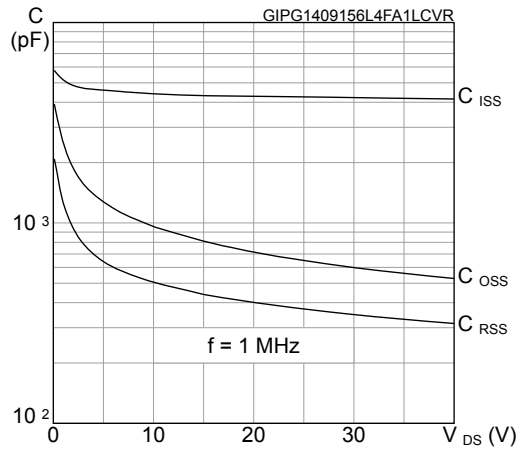


Figure 8. Normalized gate threshold voltage vs temperature

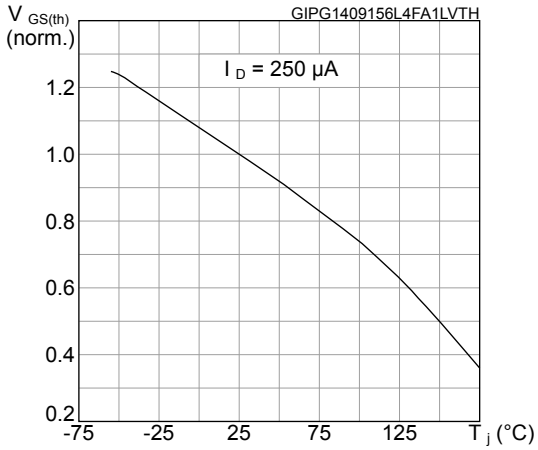


Figure 9. Normalized on-resistance vs temperature

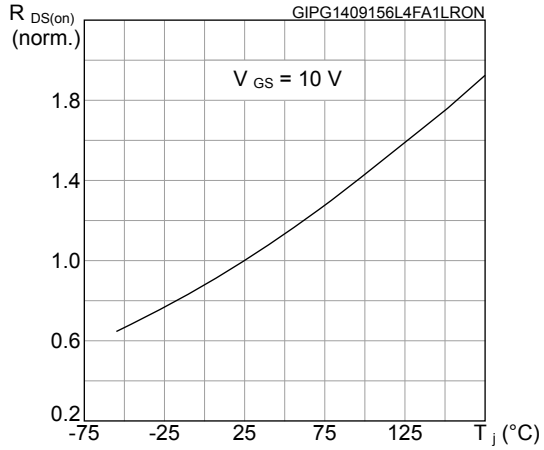


Figure 10. Normalized $V_{(BR)DSS}$ vs temperature

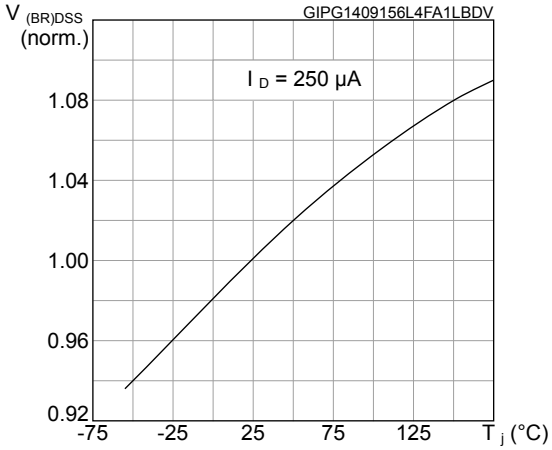
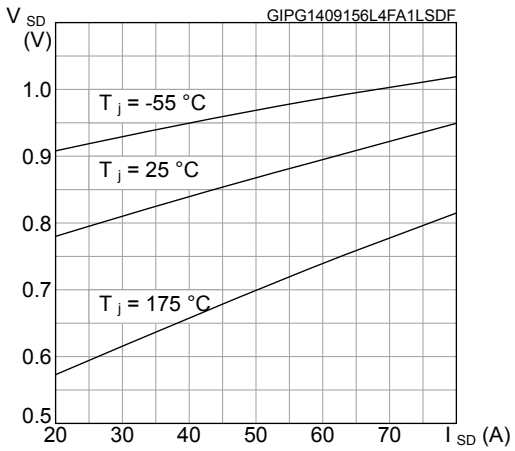


Figure 11. Source-drain diode forward characteristics



3 Test circuits

Figure 12. Test circuit for resistive load switching times

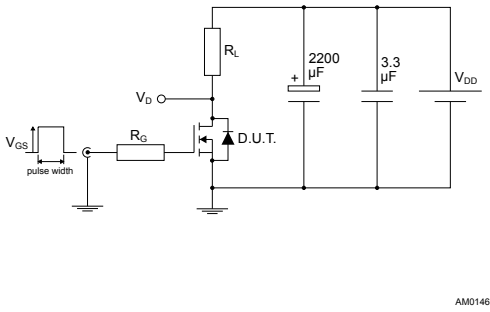


Figure 13. Test circuit for gate charge behavior

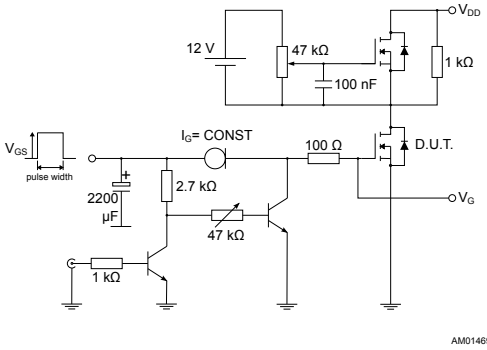


Figure 14. Test circuit for inductive load switching and diode recovery times

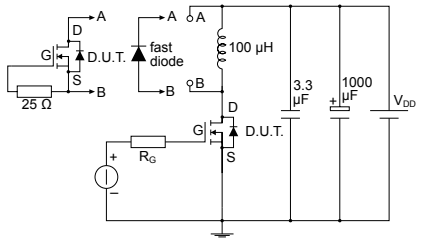


Figure 15. Unclamped inductive load test circuit

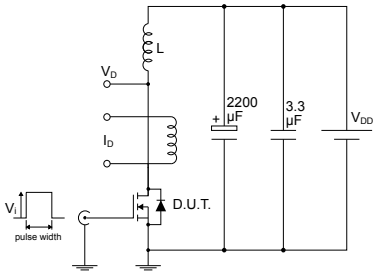


Figure 16. Unclamped inductive waveform

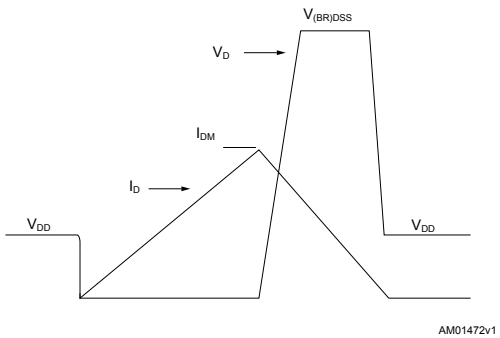
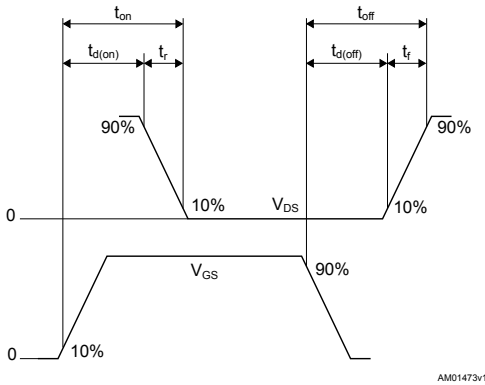


Figure 17. Switching time waveform

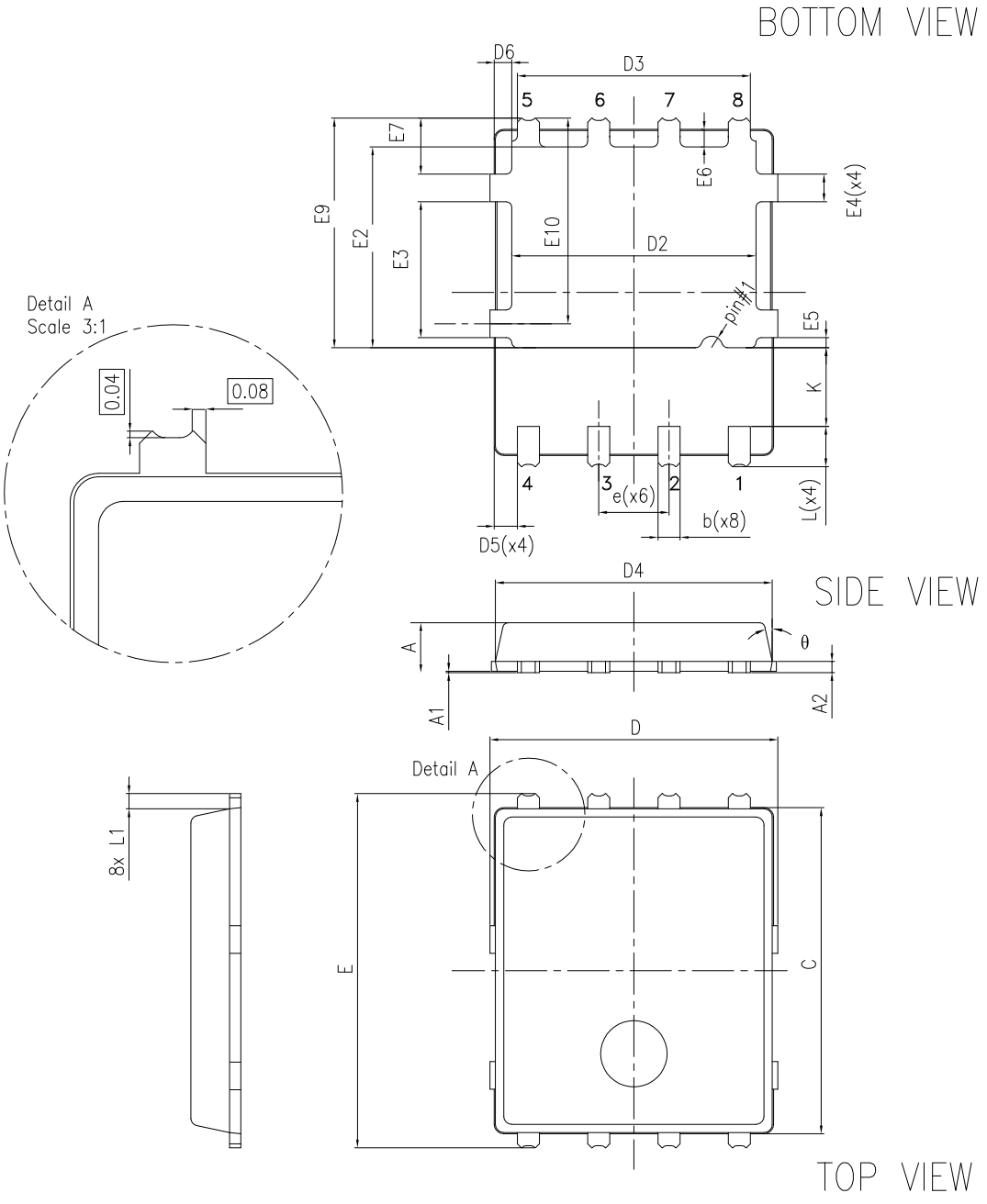


4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 PowerFLAT 5x6 WF type R package information

Figure 18. PowerFLAT 5x6 WF type R package outline

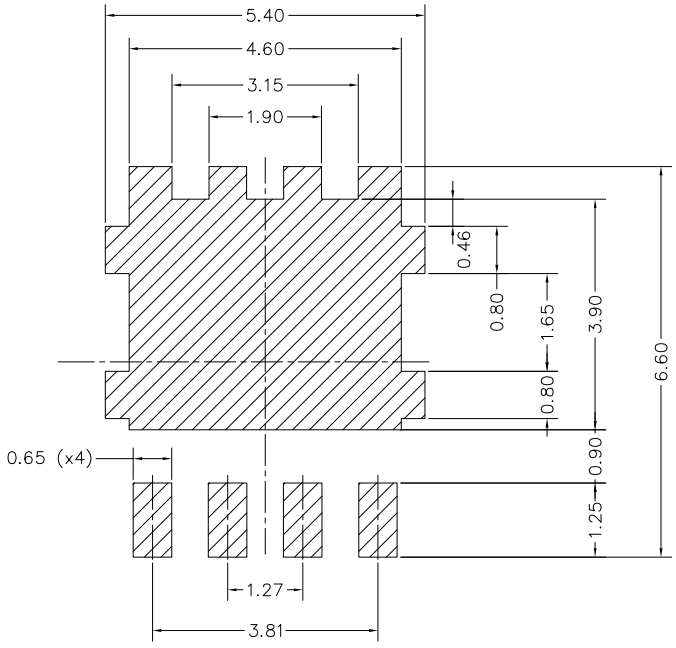


8231817_R_WF_Rev_20

Table 8. **PowerFLAT 5x6 WF type R mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.80	6.00	6.10
D	5.00	5.20	5.40
D2	4.15		4.45
D3	4.05	4.20	4.35
D4	4.80	5.00	5.10
D5	0.25	0.4	0.55
D6	0.15	0.3	0.45
e		1.27	
E	6.20	6.40	6.60
E2	3.50		3.70
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28
E6	0.20	0.325	0.45
E7	0.85	1.00	1.15
E9	4.00	4.20	4.40
E10	3.55	3.70	3.85
K	1.275		1.575
L	0.725	0.825	0.925
L1	0.175	0.275	0.375
Θ	0°		12°

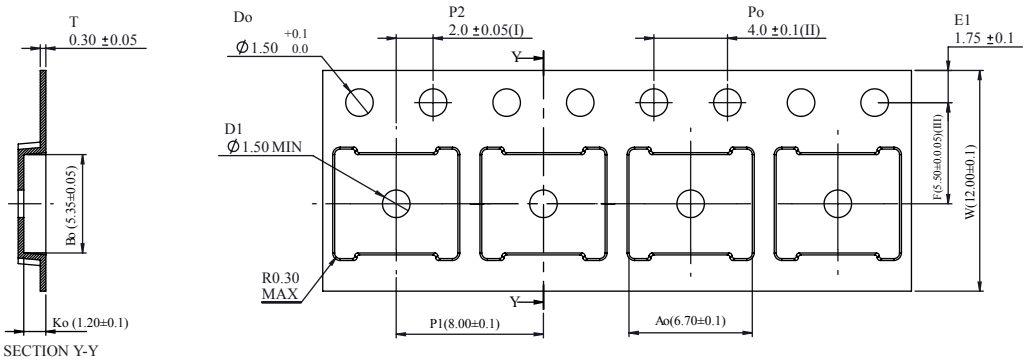
Figure 19. PowerFLAT 5x6 recommended footprint (dimensions are in mm)



8231817_FOOTPRINT_rev20

4.2 PowerFLAT 5x6 WF packing information

Figure 20. PowerFLAT 5x6 WF tape (dimensions are in mm)



(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
(III) Measured from centreline of sprocket hole to centreline of pocket.

Base and bulk qua ntity 3000 pcs

8234350_TapeWF_rev_C

Figure 21. PowerFLAT 5x6 package orientation in carrier tape

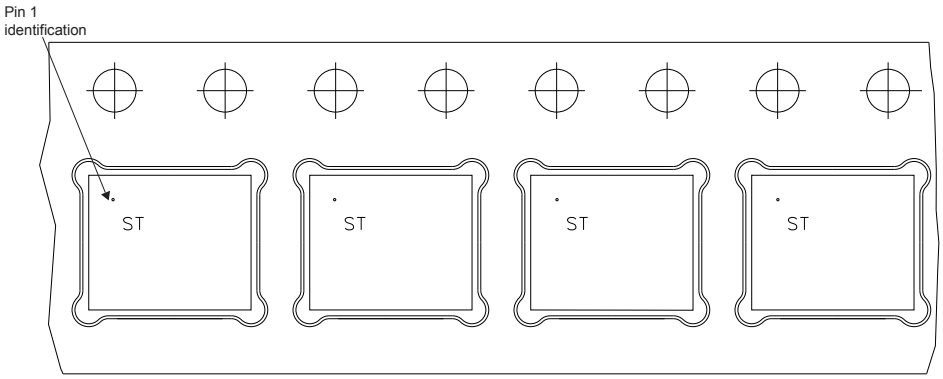
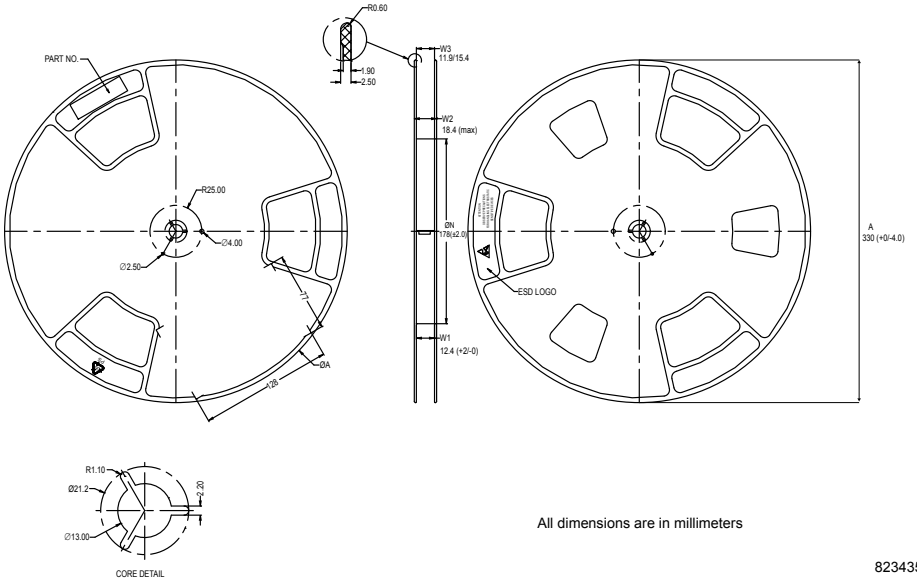


Figure 22. **PowerFLAT 5x6 reel (dimensions are in mm)**



Revision history

Table 9. **Document revision history**

Date	Revision	Changes
25-Sep-2015	1	First release.
15-Apr-2016	2	Updated title, description and features in cover page. Updated *Table 2: "Absolute maximum ratings"* and *Table 5: "On/off states"*. Minor text changes.
18-Jun-2021	3	Updated Table 1. Absolute maximum ratings. Minor text changes.

Contents

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