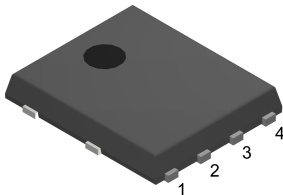
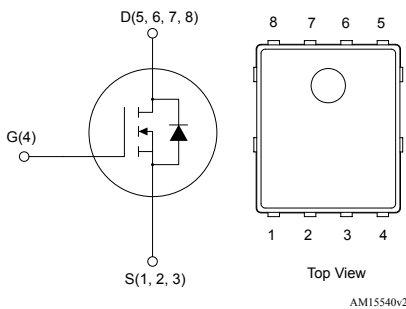


N-channel 30 V, 1.4 mΩ typ., 35 A SStripFET F5 Power MOSFET in a PowerFLAT 5x6 package


PowerFLAT 5x6


Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STL150N3LLH5	30 V	1.75 mΩ	35 A ⁽¹⁾

1. The value is rated according $R_{thj-pcb}$.

- Low on-resistance $R_{DS(on)}$
- High avalanche ruggedness
- Low gate drive power loss

Applications

- Switching applications

Description

This N-channel Power MOSFET is developed using the SStripFET F5 technology and has been optimized to achieve very low on-state resistance, contributing to a FoM that is among the best in its class.



Product status link

[STL150N3LLH5](#)

Product summary

Order code	STL150N3LLH5
Marking	150N3LH5
Package	PowerFLAT 5x6
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	30	V
V_{GS}	Gate-source voltage	± 22	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	195	A
	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	122	
$I_D^{(2)}$	Drain current (continuous) at $T_{pcb} = 25\text{ }^\circ\text{C}$	35	A
	Drain current (continuous) at $T_{pcb} = 100\text{ }^\circ\text{C}$	21.8	
$I_{DM}^{(3)}$	Drain current (pulsed)	140	A
$P_{TOT}^{(1)}$	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	114	W
$P_{TOT}^{(2)}$	Total power dissipation at $T_{pcb} = 25\text{ }^\circ\text{C}$	4	W
T_{stg}	Storage temperature range	-55 to 150	$^\circ\text{C}$
T_J	Operating junction temperature range		

1. This value is rated according to R_{thj-c} .
2. This value is rated according to $R_{thj-pcb}$.
3. Pulse width is limited by safe operating area.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	1.1	$^\circ\text{C/W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	31.3	

1. When mounted on a 1-inch² FR-4 board, 2oz Cu, $t < 10\text{ s}$.

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AV}	Not-repetitive avalanche current (pulse width limited by T_J max)	17	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$, $I_D = I_{AV}$, $V_{DD} = 24\text{ V}$)	300	mJ

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	30			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 30\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 30\text{ V}$, $T_C = 125\text{ °C}$			10	μA
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 22\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	1	1.55	2.2	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 17.5\text{ A}$		1.4	1.75	m Ω
		$V_{GS} = 4.5\text{ V}$, $I_D = 17.5\text{ A}$		1.9	2.4	m Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	5800	-	pF
C_{oss}	Output capacitance		-	1147	-	
C_{rSS}	Reverse transfer capacitance		-	127	-	
Q_g	Total gate charge	$V_{DD} = 15\text{ V}$, $I_D = 35\text{ A}$, $V_{GS} = 4.5\text{ V}$ (see Figure 13. Test circuit for gate charge behavior)	-	40	-	nC
Q_{gs}	Gate-source charge		-	13.4	-	
Q_{gd}	Gate-drain charge		-	14.9	-	
R_g	Gate input resistance	$f = 1\text{ MHz}$, gate DC Bias = 0 V, test signal level = 20 mV, $I_D = 0\text{ V}$	-	1.1	-	Ω

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 15\text{ V}$, $I_D = 17.5\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	17.2	-	ns
t_r	Rise time		-	30.8	-	
$t_{d(off)}$	Turn-off delay time	(see Figure 12. Test circuit for resistive load switching times and Figure 17. Switching time waveform)	-	65.8	-	
t_f	Fall time		-	47.8	-	

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		35	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		140	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 35\text{ A}$	-		1.1	V
t_{rr}	Reverse recovery time	$I_{SD} = 35\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 25\text{ V}$	-	43.8		ns
Q_{rr}	Reverse recovery charge	(see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	46		nC
I_{RRM}	Reverse recovery current		-	2.1		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

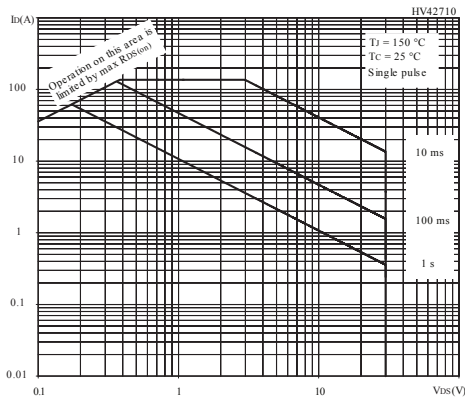


Figure 2. Thermal impedance

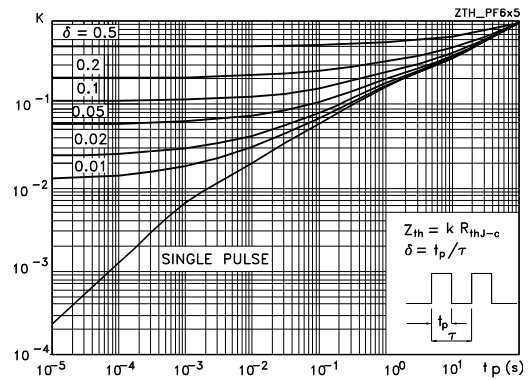


Figure 3. Output characteristics

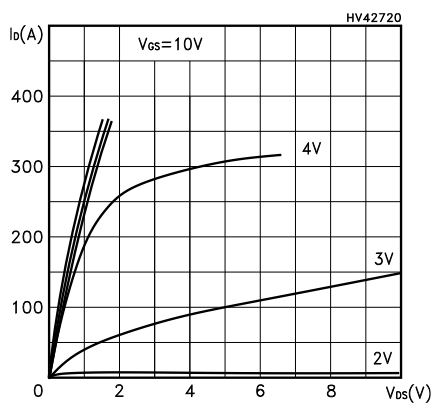


Figure 4. Transfer characteristics

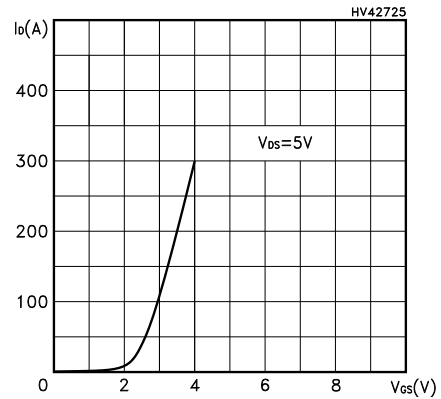


Figure 5. Normalized $B_{V_{DS}}$ vs temperature

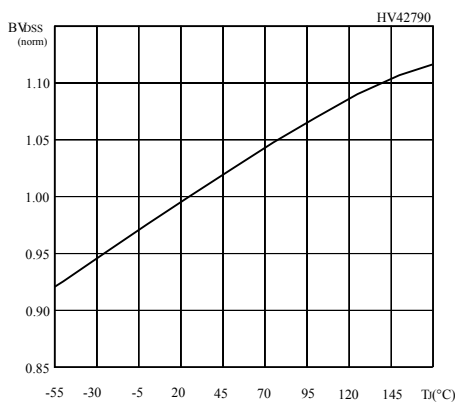


Figure 6. Static drain-source on-resistance

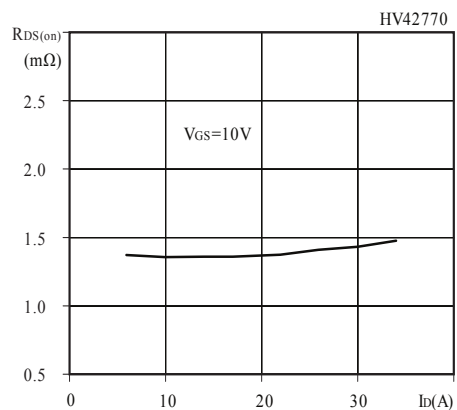


Figure 7. Gate charge vs gate-source voltage

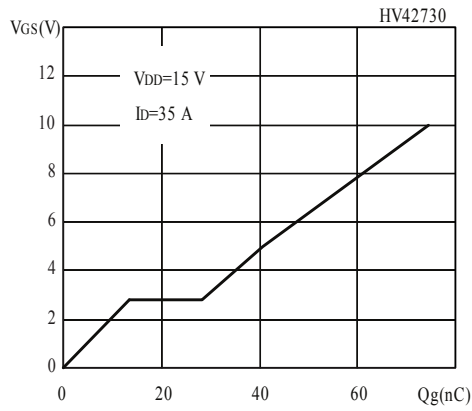


Figure 8. Capacitance variations

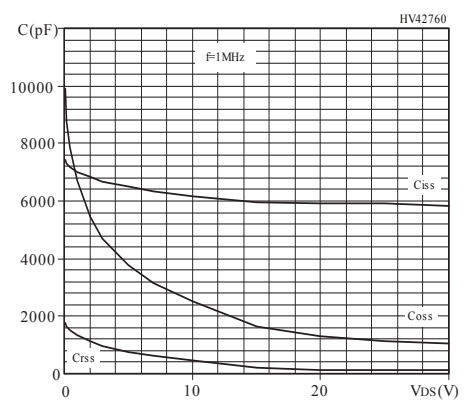


Figure 9. Normalized gate threshold voltage vs temperature

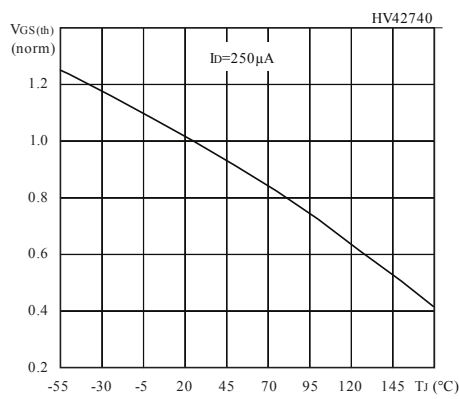


Figure 10. Normalized on-resistance vs temperature

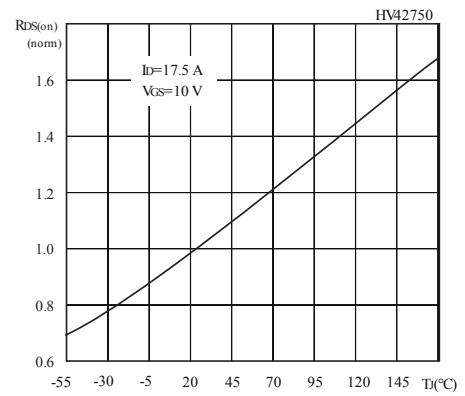
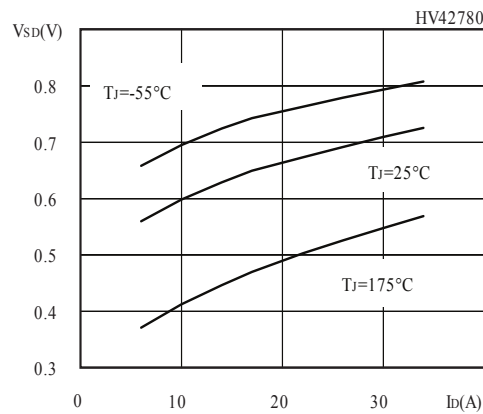
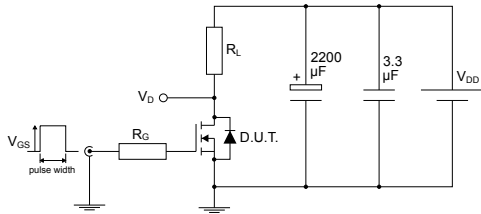


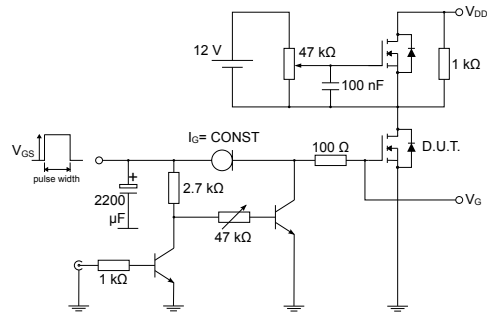
Figure 11. Source-drain diode forward characteristics



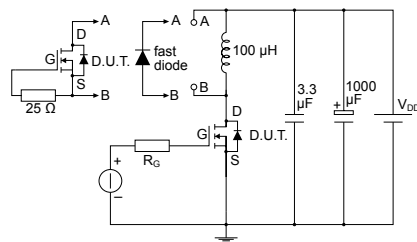
3 Test circuits

Figure 12. Test circuit for resistive load switching times


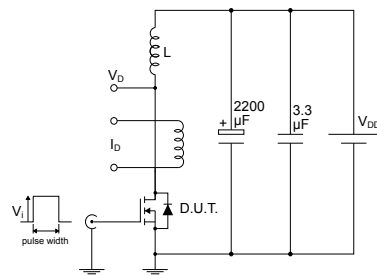
AM01468v1

Figure 13. Test circuit for gate charge behavior


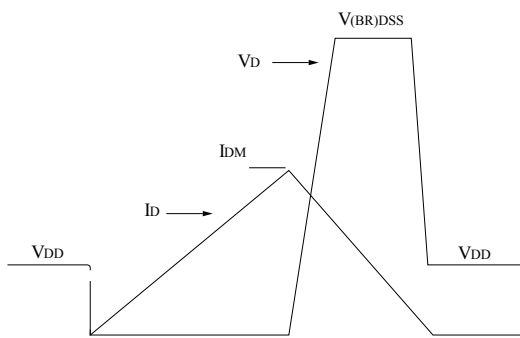
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Figure 14. Test circuit for inductive load switching and diode recovery times


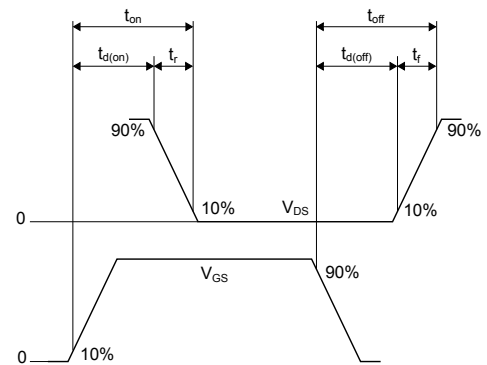
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Figure 15. Unclamped inductive load test circuit


AM01471v1

Figure 16. Unclamped inductive waveform


AM01472v1

Figure 17. Switching time waveform


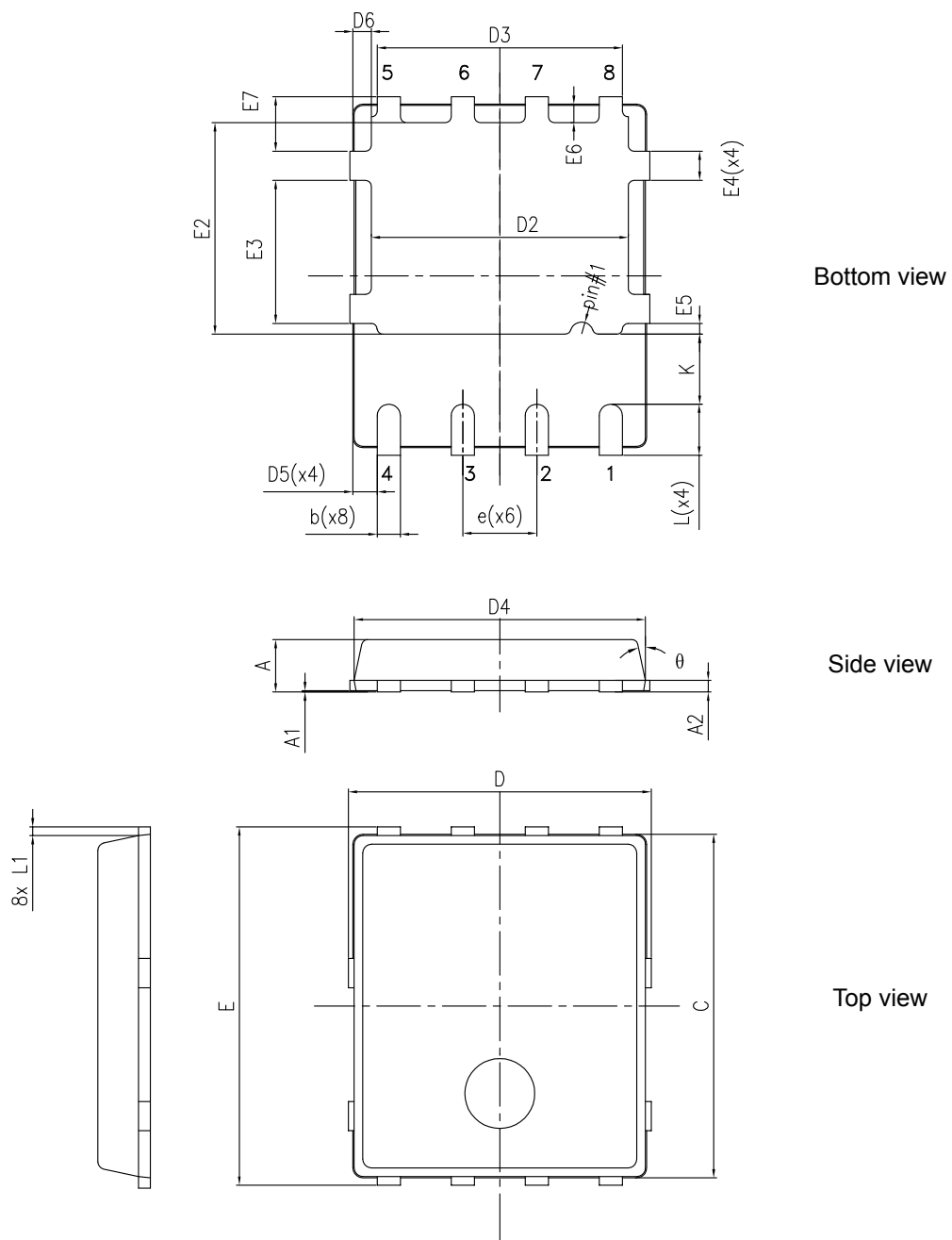
AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 PowerFLAT 5x6 type C package information

Figure 18. PowerFLAT 5x6 type C package outline



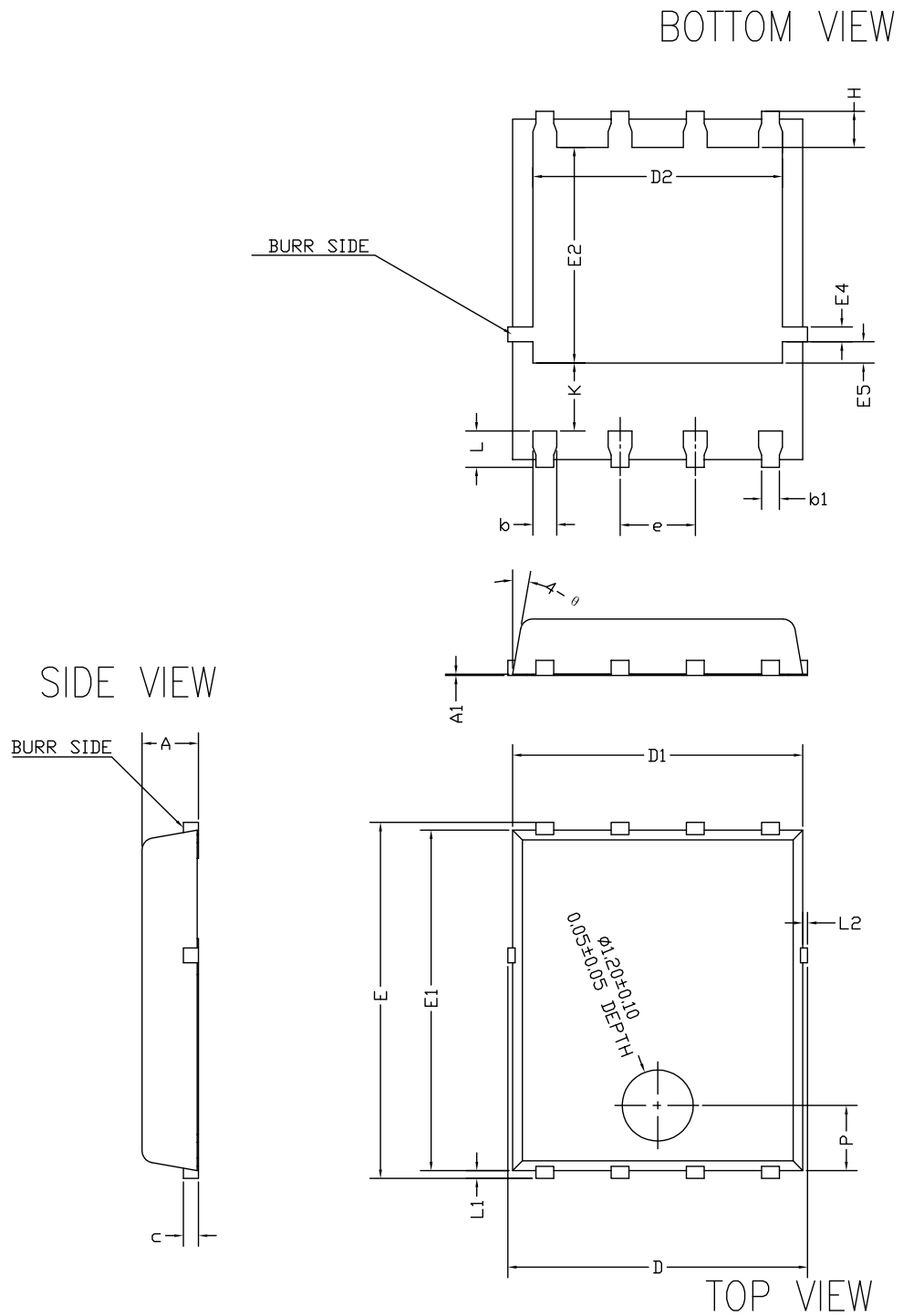
8231817_typeC_Rev20

Table 8. PowerFLAT 5x6 type C package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.80	6.00	6.20
D	5.00	5.20	5.40
D2	4.15		4.45
D3	4.05	4.20	4.35
D4	4.80	5.00	5.20
D5	0.25	0.40	0.55
D6	0.15	0.30	0.45
e		1.27	
E	5.95	6.15	6.35
E2	3.50		3.70
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28
E6	0.20	0.325	0.45
E7	0.75	0.90	1.05
K	1.05		1.35
L	0.725		1.025
L1	0.05	0.15	0.25
θ	0°		12°

4.2 PowerFLAT 5x6 type C SUBCON package information

Figure 19. PowerFLAT 5x6 type C SUBCON package outline

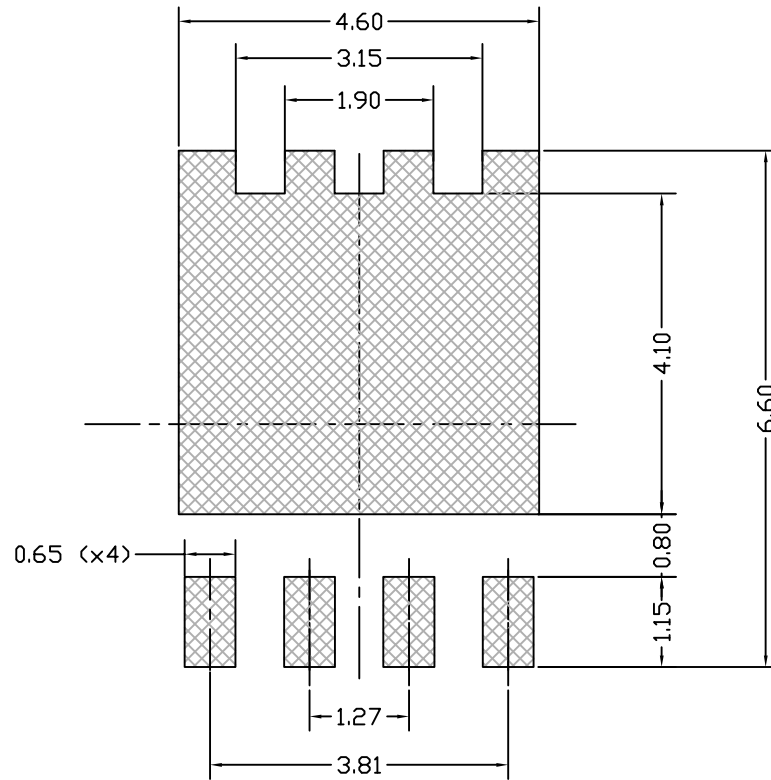


8472137_SUBCON_998G_REV4

Table 9. PowerFLAT 5x6 type C SUBCON package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.90	0.95	1.00
A1		0.02	
b	0.35	0.40	0.45
b1		0.30	
c	0.21	0.25	0.34
D			5.10
D1	4.80	4.90	5.00
D2	4.01	4.21	4.31
e	1.17	1.27	1.37
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.54	3.64	3.74
E4	0.15	0.25	0.35
E5	0.26	0.36	0.46
H	0.51	0.61	0.71
K	0.95		
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
L2			0.10
P	1.00	1.10	1.20
θ	8°	10°	12°

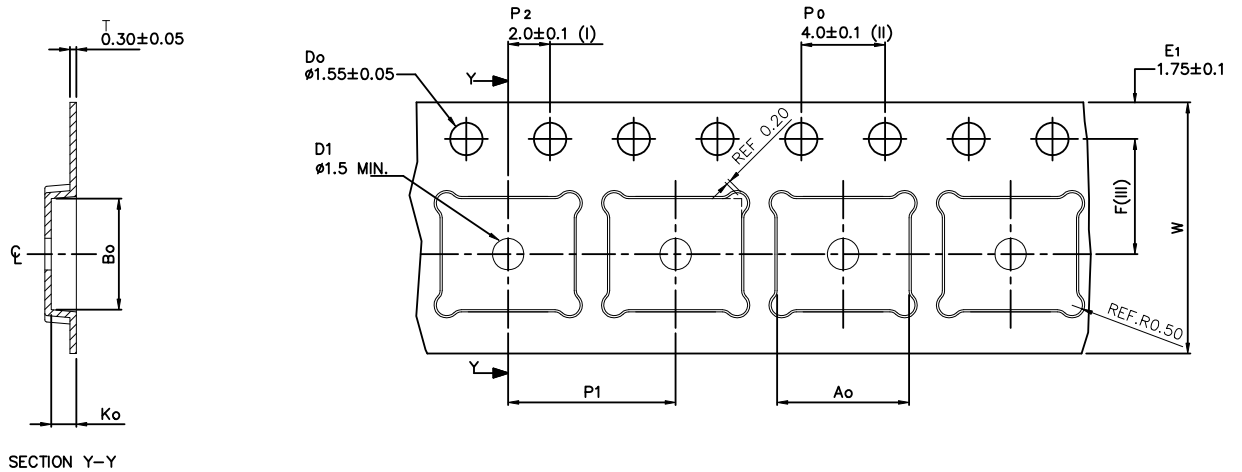
Figure 20. PowerFLAT 5x6 recommended footprint (dimensions are in mm)



8231817_FOOTPRINT_simp_Rev_20

4.3 PowerFLAT 5x6 packing information

Figure 21. PowerFLAT 5x6 tape (dimensions are in mm)



A ₀	6.30 +/- 0.1
B ₀	5.30 +/- 0.1
K ₀	1.20 +/- 0.1
F	5.50 +/- 0.1
P ₁	8.00 +/- 0.1
W	12.00 +/- 0.3

(I) Measured from centreline of sprocket hole to centreline of pocket.

(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .

(III) Measured from centreline of sprocket hole to centreline of pocket

Base and bulk quantity 3000 pcs
All dimensions are in millimeters

8234350_Tape_rev_C

Figure 22. PowerFLAT 5x6 package orientation in carrier tape

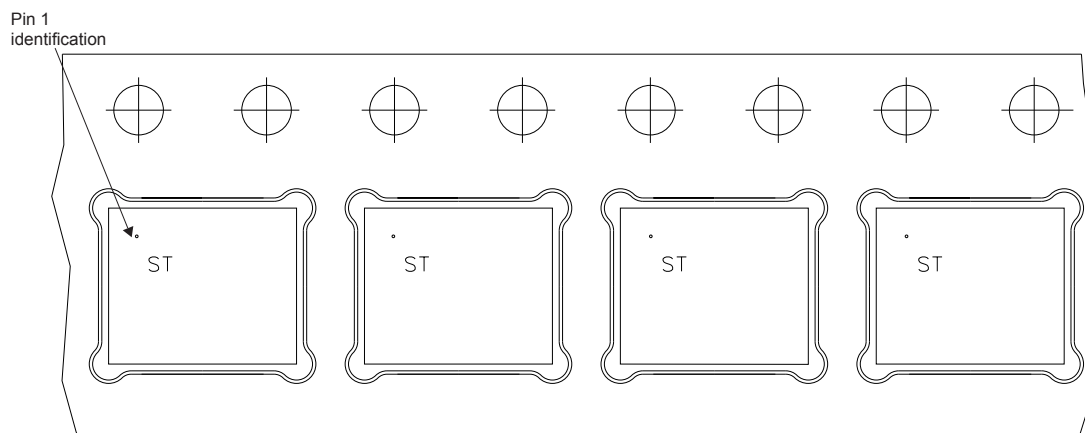
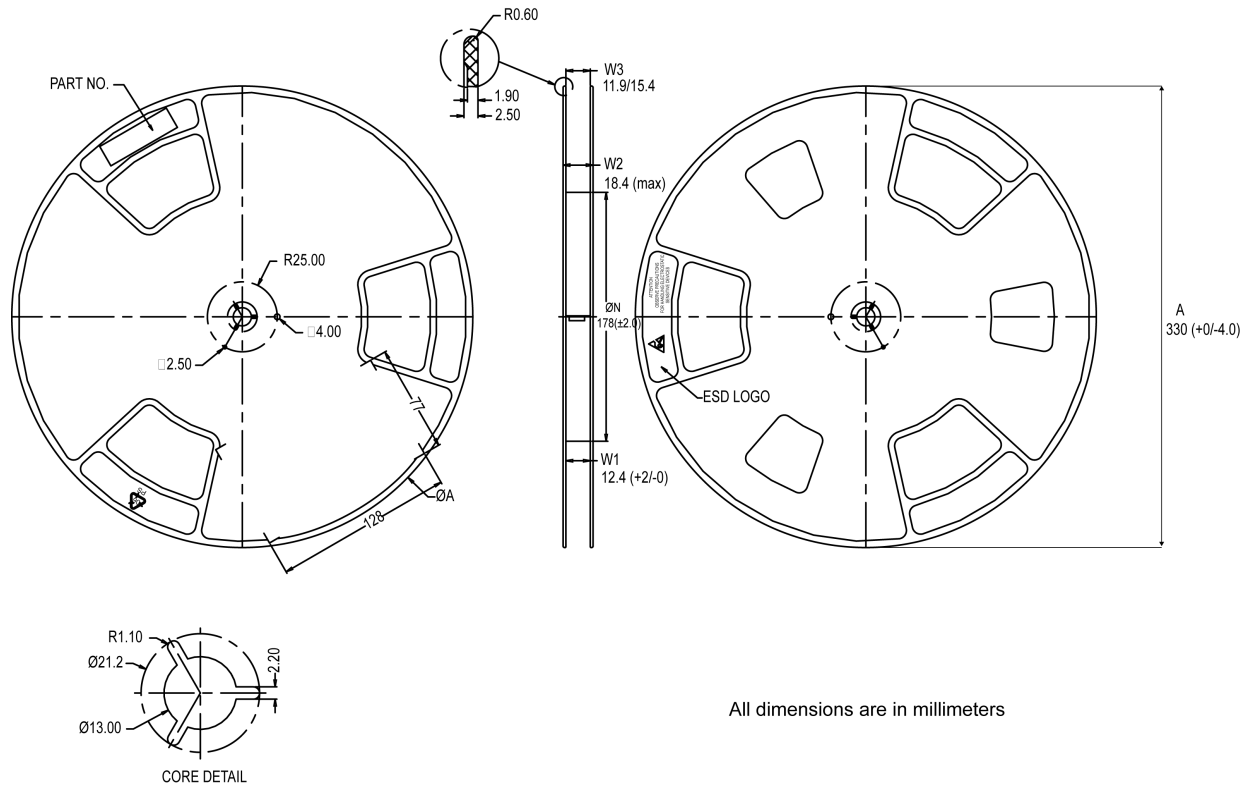


Figure 23. PowerFLAT 5x6 reel



All dimensions are in millimeters

8234350_Reel_rev_C

Revision history

Table 10. Document revision history

Date	Revision	Changes
22-Oct-2007	1	First release
01-Apr-2008	2	Document status promoted from preliminary data to datasheet
23-Sep-2008	3	V_{GS} value has been changed on <i>Table 2</i> and <i>Table 5</i>
24-Jan-2020	4	$V_{GS(th)}$ value has been changed on <i>Table 5</i>
12-Jun-2009	5	<i>Section 4: Package mechanical data</i> has been updated. Minor text changes.
05-Oct-2011	6	<ul style="list-style-type: none"> – Modified: <i>Figure 1</i> and marking in <i>Table 1</i> – Modified: I_D value in <i>Figure 11</i> – Updated: <i>Figure 13, 14, 15</i> and <i>16</i> – Updated: <i>Section 4: Package mechanical data</i>
12-Feb-2020	7	Updated Section 4 Package information . Minor text changes.

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