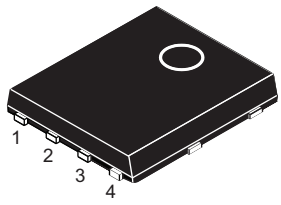
STL160N3LLH6

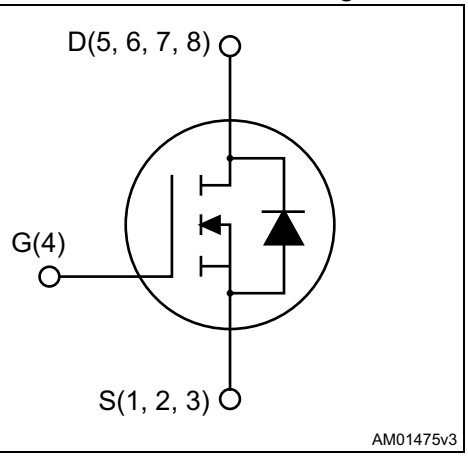
N-channel 30 V, 0.0011 Ω typ., 45 A STripFET™ H6 Power MOSFET in a PowerFLAT™ 5x6 package

Datasheet – production data



PowerFLAT™5x6

Figure 1. Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max	I_D
STL160N3LLH6	30 V	0.0013 Ω	45 A (1)

1. The value is rated according to $R_{thj\text{-}pcb}$

- Very low on-resistance
- Very low switching gate charge
- High avalanche ruggedness
- Low gate drive power loss

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the 6th generation of STripFET™ technology, with a new trench gate structure. The resulting Power MOSFET exhibits a very low $R_{DS(on)}$ in all packages.

Table 1. Device summary

Order code	Marking	Package	Packaging
STL160N3LLH6	160N3LH6	PowerFLAT™ 5x6	Tape and reel

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	30	V
V_{GS}	Gate-source voltage	± 20	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	240	A
I_D (1)	Drain current (continuous) at T_C = 100 °C	170	A
I_{DM} (1),(3)	Drain current (pulsed)	960	A
I_D (2)	Drain current (continuous) at T_{pcb} = 25 °C	45	A
I_D (2)	Drain current (continuous) at T_{pcb}=100 °C	32	A
I_{DM} (2),(3)	Drain current (pulsed)	180	A
P_{TOT} (1)	Total dissipation at T_C = 25 °C	136	W
P_{TOT} (2)	Total dissipation at T_{pcb} = 25 °C	4.8	W
T_j T_{stg}	Operating junction temperature Storage temperature	-55 to 175	°C

1. The value is rated according to $R_{thj\text{-}c}$.
2. The value is rated according to $R_{thj\text{-}pcb}$.
3. Pulse width limited by safe operating area.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	1.1	°C/W
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb	31.3	°C/W

1. When mounted on FR-4 board of 1inch², 2oz Cu, t < 10 sec.

Table 4. Avalanche data

Symbol	Parameter	Value	Unit
I_{AV}	Not-repetitive avalanche current (pulse width limited by T_j max)	35	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AV})	900	mJ

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified).

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS}= 0, I_D = 250 µA	30			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0, V_{DS} = 30 V			1	µA
		V_{DS} = 30 V at T_C = 125 °C			10	µA
I_{GSS}	Gate body leakage current	V_{DS} = 0, V_{GS} = ±20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 250 µA	1			V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS}= 10 V, I_D= 17.5 A		0.0011	0.0013	Ω
		V_{GS}= 4.5 V, I_D= 17.5 A		0.0016	0.0020	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{GS}=0, V_{DS} = 25 V, f=1 MHz	-	6375	-	pF
C_{oss}	Output capacitance		-	1230	-	pF
C_{rss}	Reverse transfer capacitance		-	675	-	pF
Q_g	Total gate charge	V_{DD}=15 V, I_D = 35 A V_{GS} =4.5 V *(see Figure 14)*	-	61.5	-	nC
Q_{gs}	Gate-source charge		-	20		nC
Q_{gd}	Gate-drain charge		-	24		nC
R_g	Gate input resistance	f = 1 MHz, gate DC Bias = 0, test signal level = 20 mV, I_D = 0	-	1.4	-	Ω

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD}=15 V, I_D= 17.5 A, R_G=4.7 Ω, V_{GS}=10 V *(see Figure 13)*	-	22.5	-	ns
t_r	Rise time		-	32	-	ns
$t_{d(off)}$	Turn-off delay time		-	107.5	-	ns
t_f	Fall time		-	54	-	ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		45	A
I_{SDM}(1)	Source-drain current (pulsed)		-		180	A
V_{SD}(2)	Forward on voltage	V_{GS}=0, I_{SD} = 35 A	-		1.1	V
t_{rr}	Reverse recovery time	I_{SD} = 35 A, di/dt = 100 A/µs, V_{DD}=25 V	-	37.2		ns
Q_{rr}	Reverse recovery charge		-	36		nC
I_{RRM}	Reverse recovery current		-	1.9		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration=300µs, duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

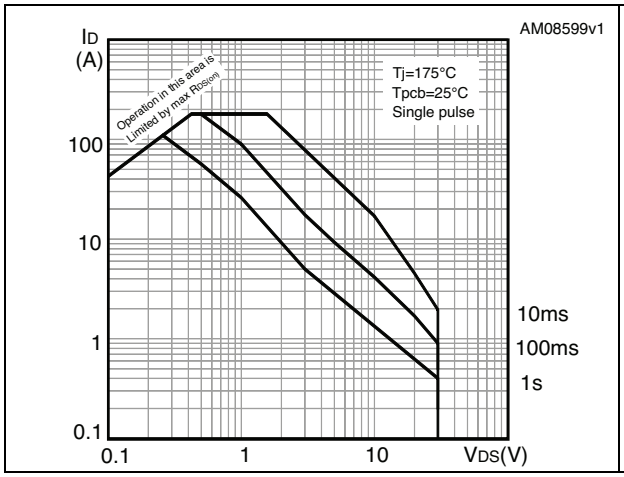


Figure 3. Thermal impedance

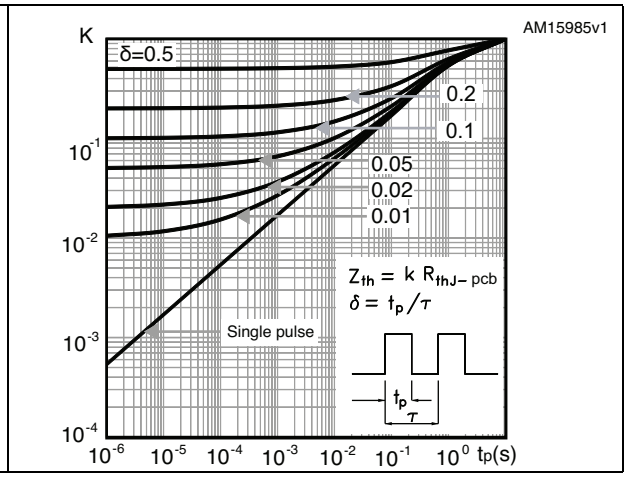


Figure 4. Output characteristics

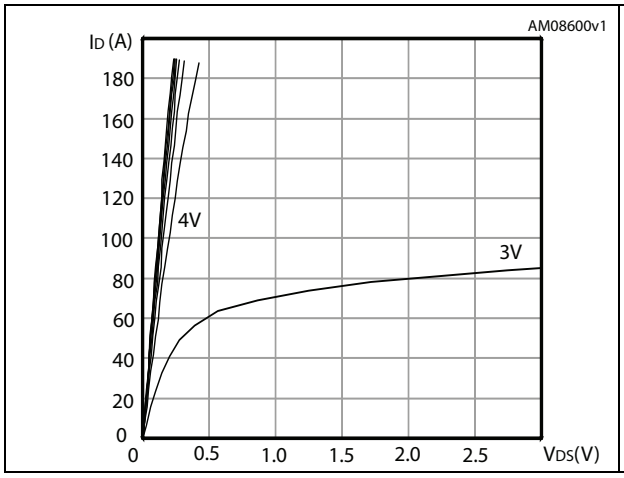


Figure 5. Transfer characteristics

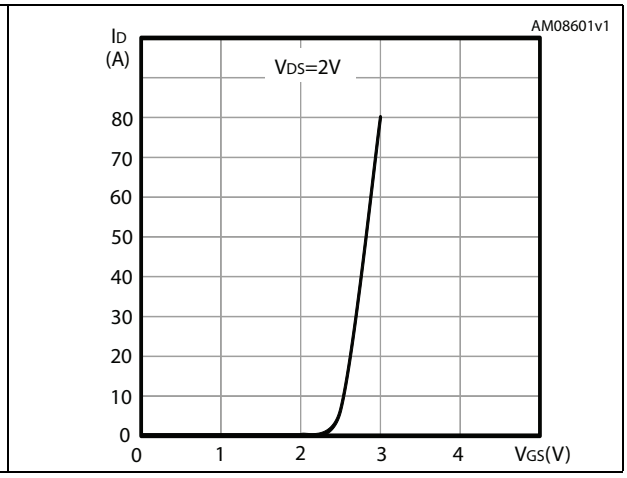


Figure 6. Normalized $V_{(BR)DSS}$ vs temperature

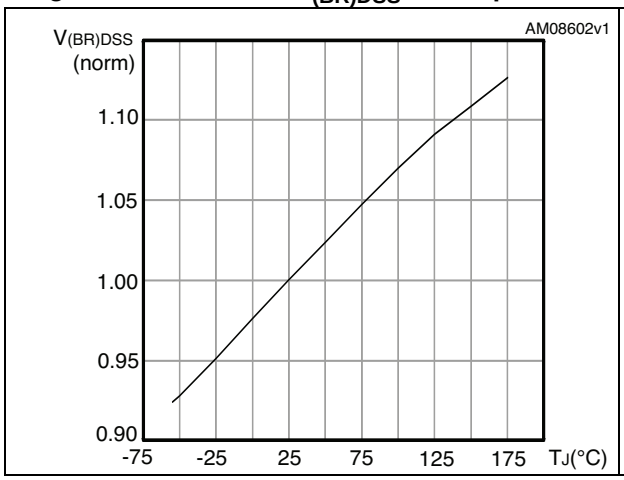


Figure 7. Static drain-source on-resistance

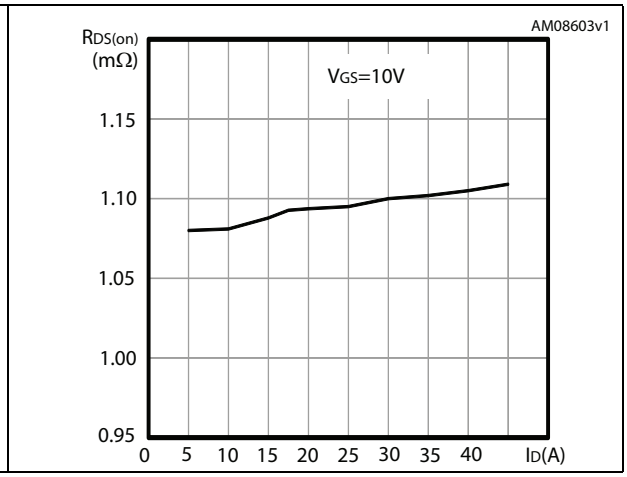


Figure 8. Gate charge vs gate-source voltage

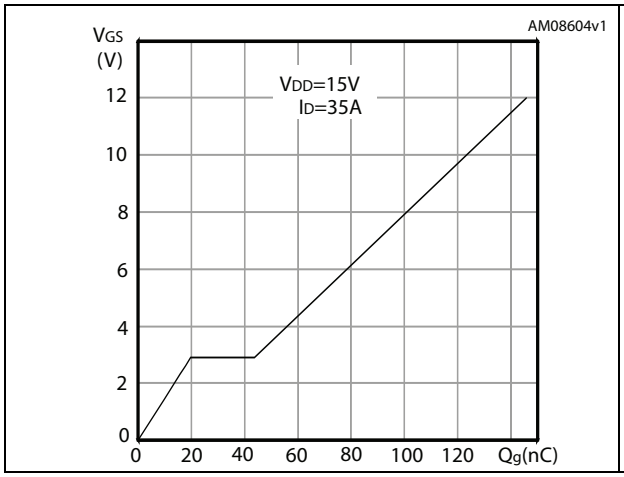


Figure 9. Capacitance variations

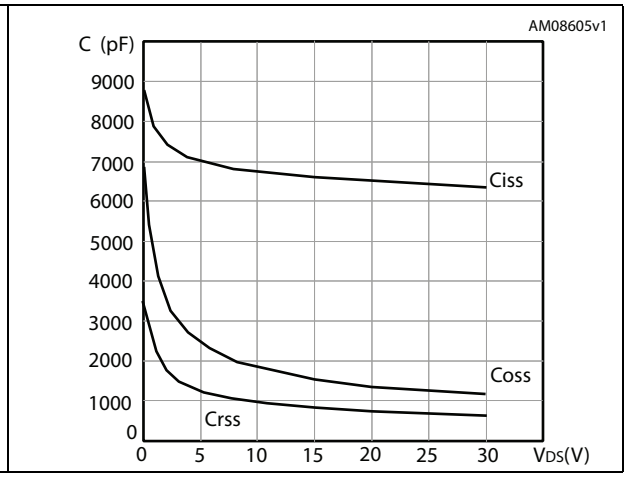


Figure 10. Normalized gate threshold voltage vs temperature

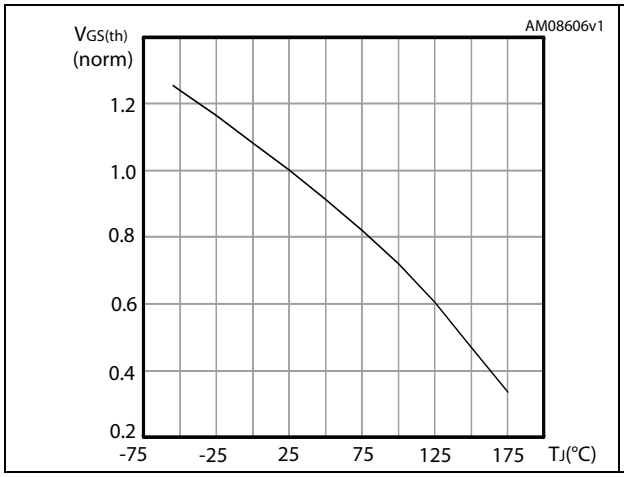


Figure 11. Normalized on-resistance vs temperature

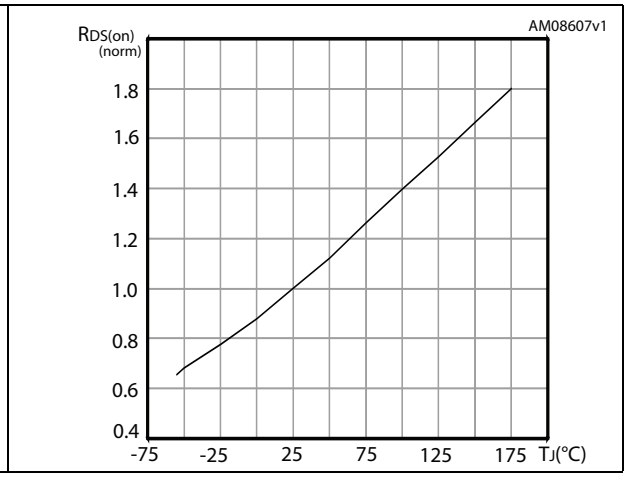
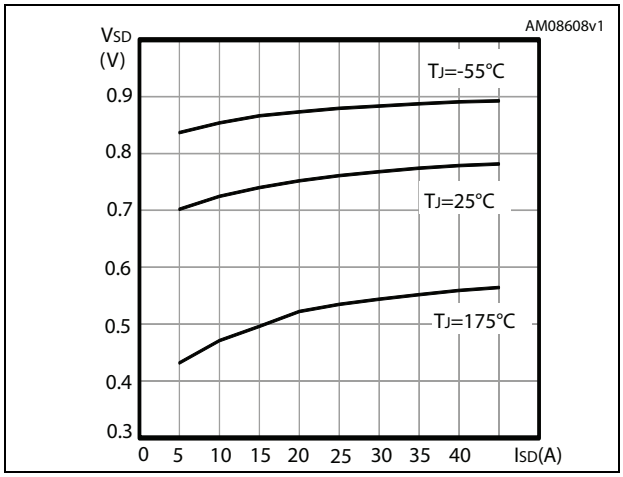


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

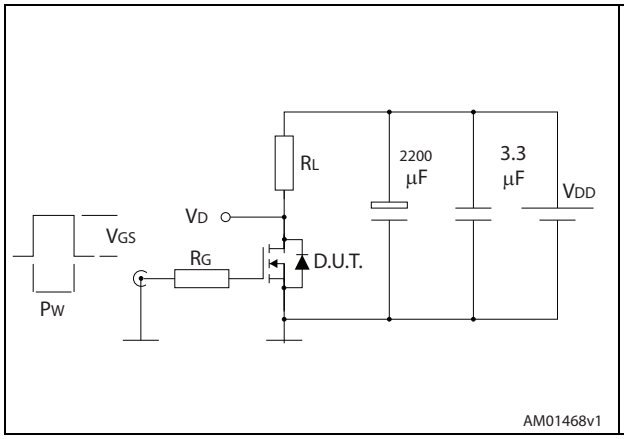


Figure 14. Gate charge test circuit

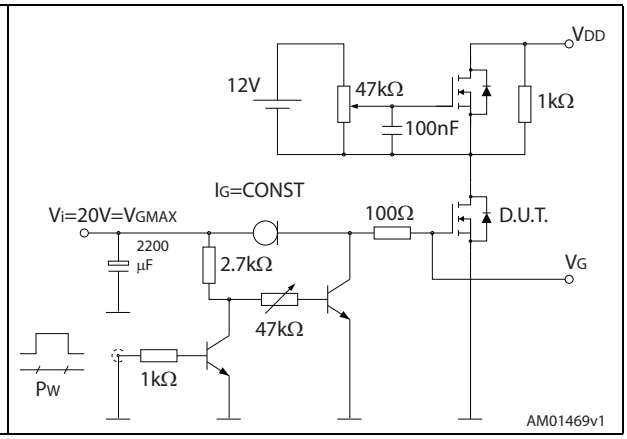


Figure 15. Test circuit for inductive load switching and diode recovery times

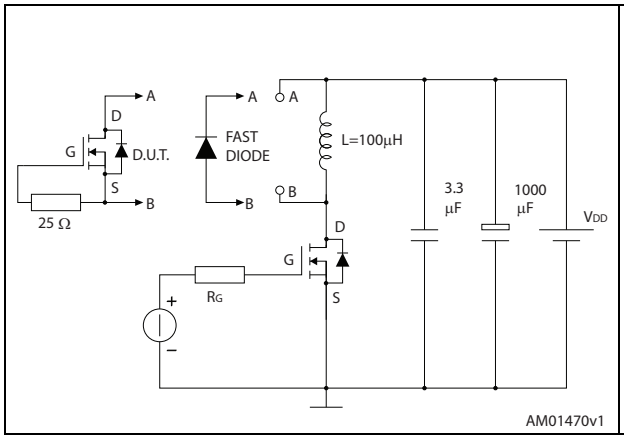


Figure 16. Unclamped inductive load test circuit

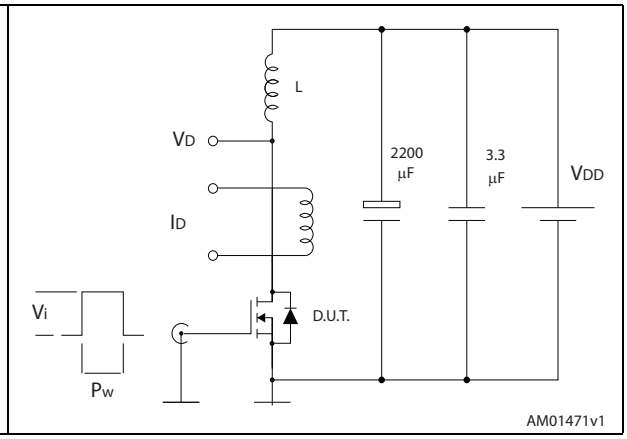


Figure 17. Unclamped inductive waveform

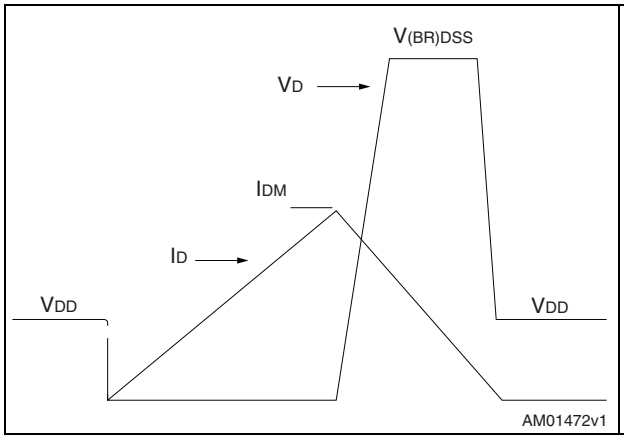
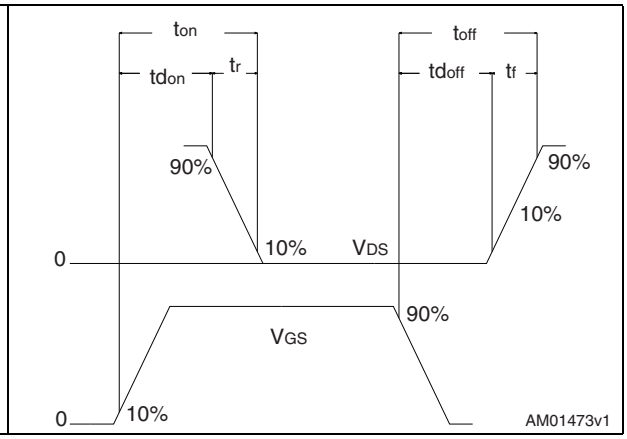


Figure 18. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.
ECOPACK® is an ST trademark.

Figure 19. PowerFLAT™ 5x6 type S-C mechanical data

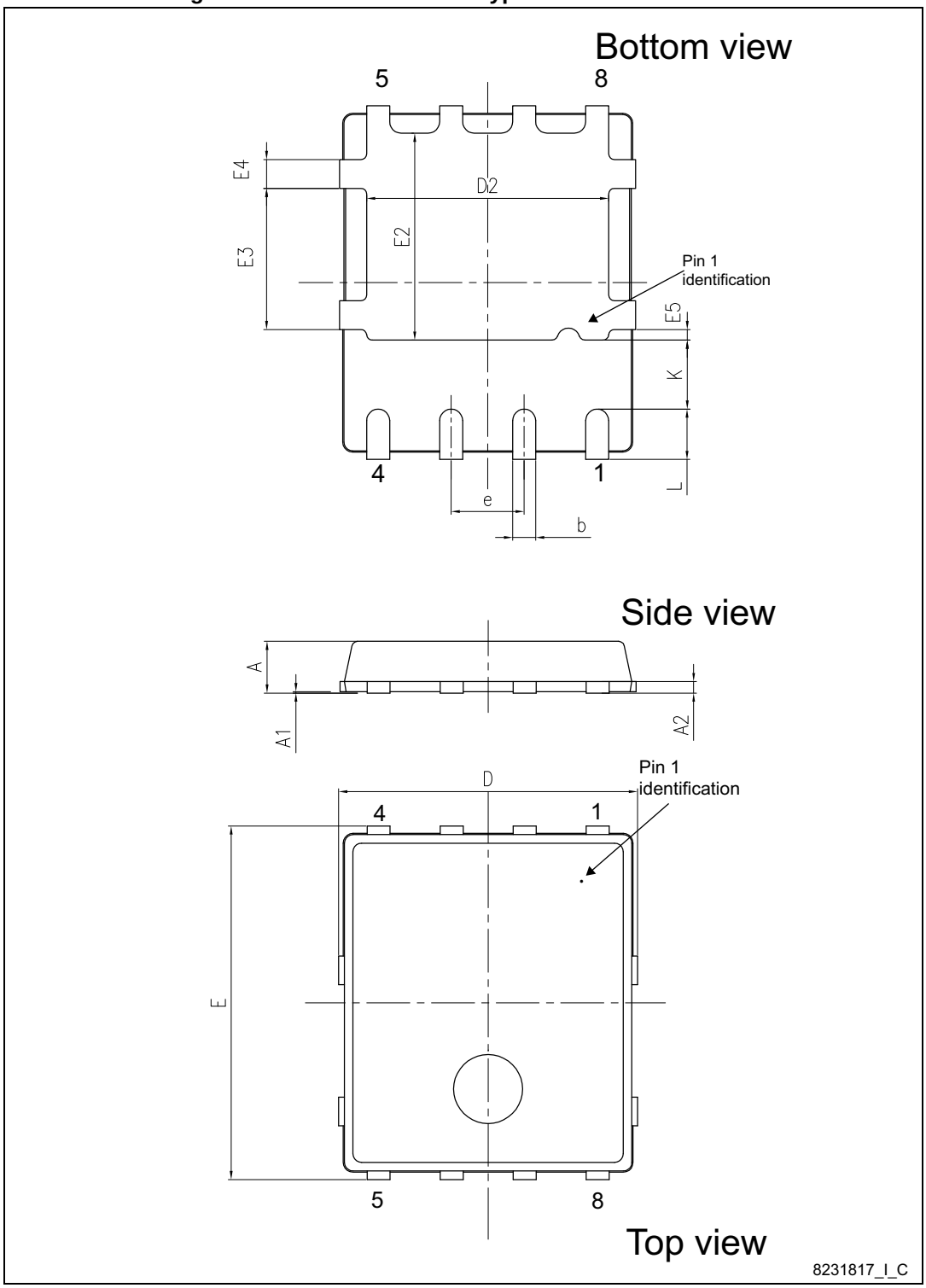
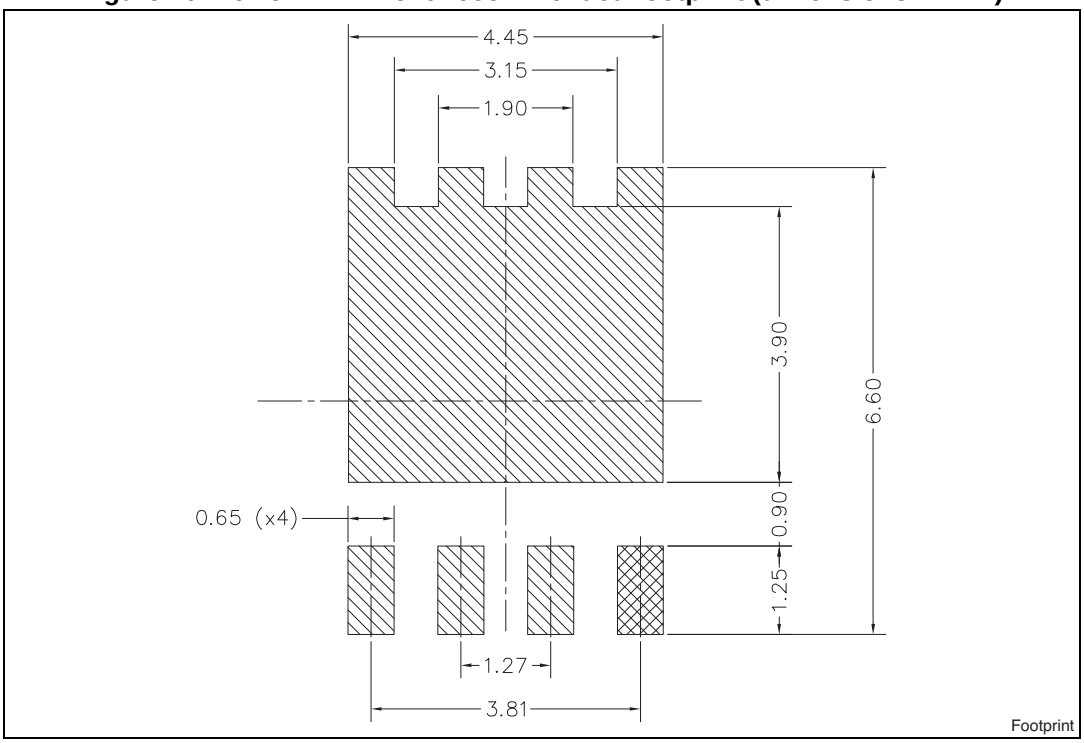


Table 9. PowerFLAT™ 5x6 type S-C mechanical data

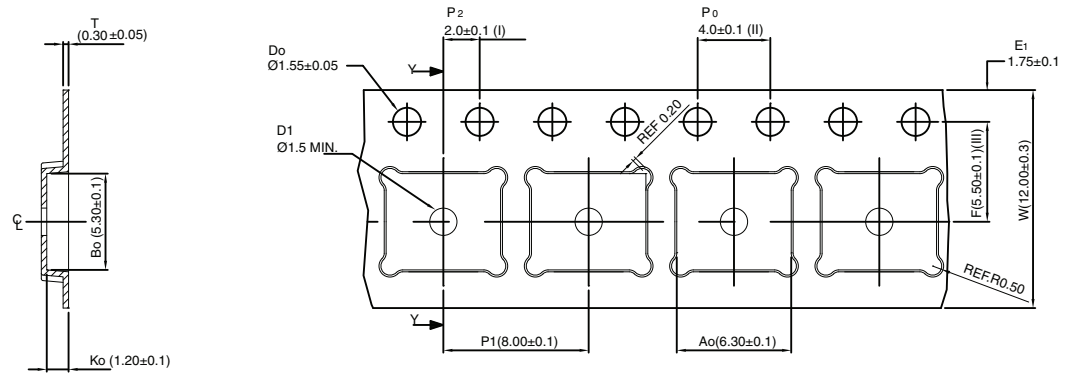
Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D		5.20	
E		6.15	
D2	4.11		4.31
E2	3.50		3.70
e		1.27	
e1		0.65	
L	0.715		1.015
K	1.05		1.35
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28

Figure 20. PowerFLAT™ 5x6 recommended footprint (dimensions in mm)



5 Packaging mechanical data

Figure 21. PowerFLAT™ 5x6 tape(a)



(I) Measured from centerline of sprocket hole to centerline of pocket.

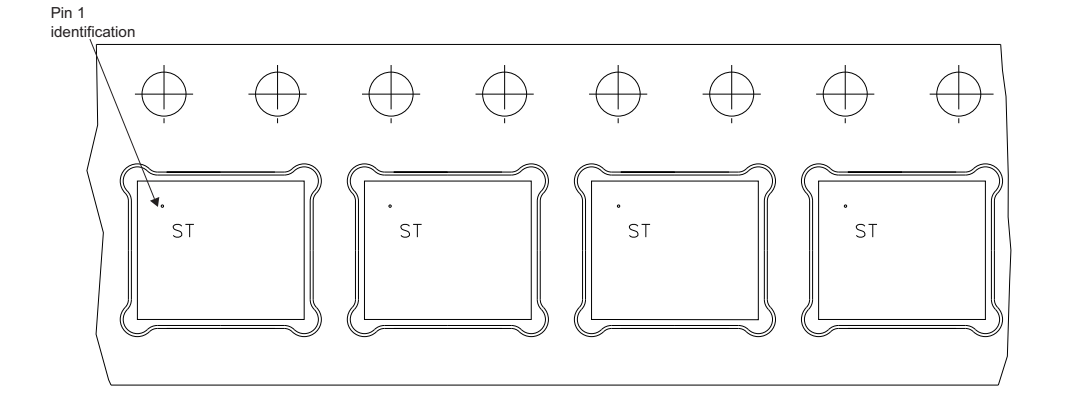
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .

(III) Measured from centerline of sprocket hole to centerline of pocket.

Base and bulk quantity 3000 pcs

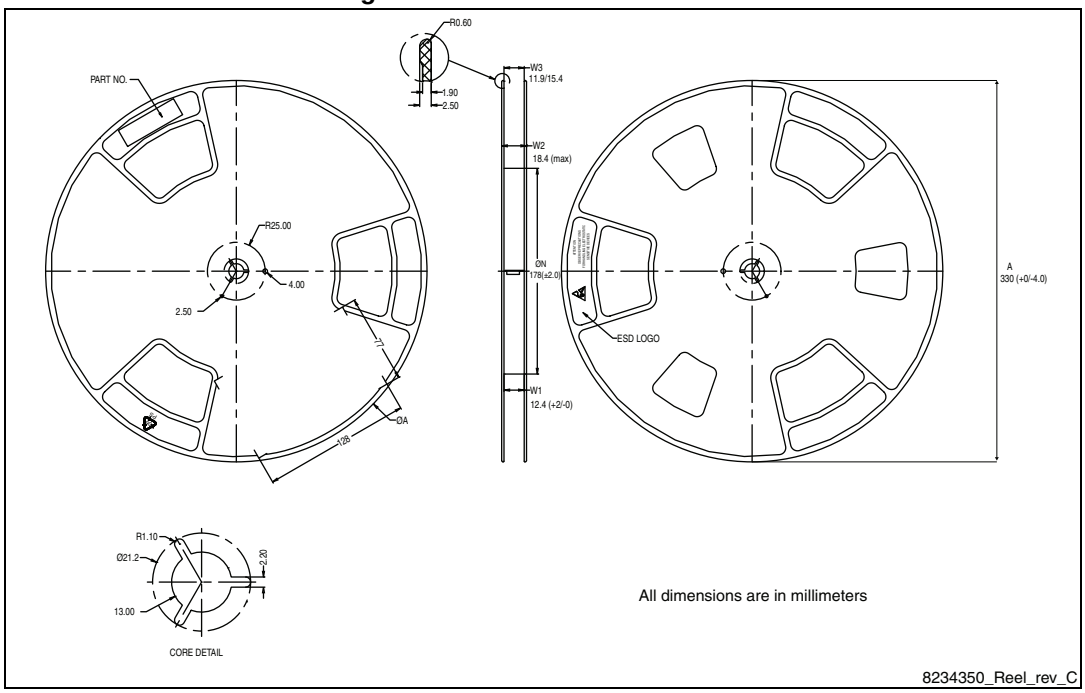
8234350_Tape_rev_C

Figure 22. PowerFLAT™ 5x6 package orientation in carrier tape



a. All dimensions are in millimeters.

Figure 23. PowerFLAT™ 5x6 reel



6 Revision history

Table 10. Document revision history

Date	Revision	Changes
10-Nov-2010	1	First release.
10-Nov-2011	2	*Section 4: Package mechanical data* has been updated. Minor text changes.
31-Jul-2013	3	– Modified: I_D in the title and in the *Features Table*, *Table 5*, *6* and *7* – Modified: values on the *Table 2*, $R_{thj\text{-}case}$ on the *Table 3*, max values for the I_{SD} and I_{SDM} on *Table 8* – Updated: *Section 4: Package mechanical data* – Inserted: *Section 5: Packaging mechanical data* – Modified: *Figure 13*, *14*, *15* and *16* – Minor text changes
09-Aug-2013	4	– Modified: drain current (continuous) at T_C = 100 °C value and drain current (continuous) at T_{pcb}=100 °C value – Modified: test conditions of $R_{DS(on)}$ – Modified: I_D in *Table 6* and *7* – Modified: I_{SD} in *Table 8* – Modified: *Figure 2*, *3*, *4*, *5*, *7*, *12*, *13*, *14*, *15* and *16* – Updated: *Section 4: Package mechanical data* – Minor text changes
24-Sep-2013	5	– Modified: marking in *Table 1* – Minor text changes
23-Sep-2014	6	– Modified: title – Modified: *Features* – Modified: *Description* – Updated: *Section 4: Package mechanical data* – Minor text changes

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