STL16N60M2



N-channel 600 V, 0.290 Ω typ., 8 A MDmesh™ M2 Power MOSFET in a PowerFLAT™ 5x6 HV package

Datasheet - production data

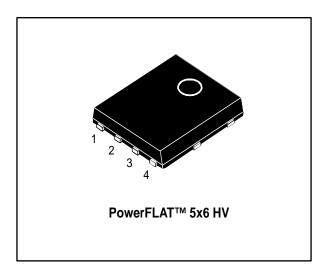
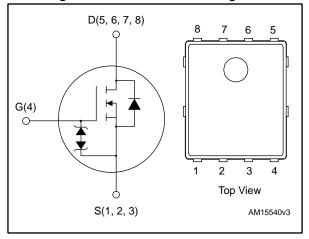


Figure 1: Internal schematic diagram



Features

Order code	V _{DS} @ T _{Jmax}	R _{DS(on)} max.	I _D
STL16N60M2 650 V		0.355 Ω	8 A

- Extremely low gate charge
- Excellent output capacitance (C_{OSS}) profile
- 100% avalanche tested
- Zener-protected

Applications

Switching applications

Description

This device is an N-channel Power MOSFET developed using MDmesh™ M2 technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance and optimized switching characteristics, rendering it suitable for the most demanding high efficiency converters.

Table 1: Device summary

Order code	Marking	Package	Packing	
STL16N60M2	16N60M2	PowerFLAT™ 5x6 HV	Tape and reel	

Contents STL16N60M2

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STL16N60M2 Electrical ratings

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{GS}	Gate-source voltage	± 25	V
I _D	Drain current (continuous) at T _C = 25 °C	8 ⁽¹⁾	Α
I _D	Drain current (continuous) at T _C = 100 °C	5	А
I _{DM} ⁽²⁾	Drain current (pulsed)	32	А
P _{TOT}	Total dissipation at T _C = 25 °C	52	W
dv/dt ⁽³⁾	Peak diode recovery voltage slope	15	V/ns
dv/dt ⁽⁴⁾	MOSFET dv/dt ruggedness	50	V/ns
T _{stg}	Storage temperature	- 55 to 150	°C
T _j	Max. operating junction temperature	150	

Notes:

Table 3: Thermal data

Symbol	Symbol Parameter		Unit
R _{thj-case}	Thermal resistance junction-case max	2.40	°C/W
R _{thj-pcb}	Thermal resistance junction-pcb max ⁽¹⁾	59	°C/W

Notes:

Table 4: Avalanche characteristics

Symbol	Symbol Parameter		Unit
I _{AR}	Avalanche current, repetetive or not repetetive (pulse width limited by T_{jmax})	2	Α
E _{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR} , V_{DD} = 50 V)	130	mJ

⁽¹⁾The value is limited by package.

 $[\]ensuremath{^{(2)}}\mbox{Pulse}$ width limited by safe operating area.

 $^{^{(3)}}I_{SD} \leq 8$ A, di/dt ≤ 400 A/µs; V_{DS peak} < V_{(BR)DSS}, V_{DD} = 80% V_{(BR)DSS}

 $^{^{(4)}}V_{DS} \le 480 \text{ V}$

⁽¹⁾When mounted on 1 inch² FR-4, 2 Oz copper board

Electrical characteristics STL16N60M2

2 Electrical characteristics

(T_C= 25 °C unless otherwise specified)

Table 5: On/off states

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0 \text{ V}, I_D = 1 \text{ mA}$	600			V
	Zoro goto voltago Droin	$V_{GS} = 0 \text{ V}, V_{DS} = 600 \text{ V}$			1	μΑ
I _{DSS}	Zero gate voltage Drain current	$V_{GS} = 0 \text{ V}, V_{DS} = 600 \text{ V},$ $T_{C} = 125 \text{ °C}$			100	μΑ
I _{GSS}	Gate-body leakage current	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 25 \text{ V}$			±10	μΑ
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	2	3	4	V
R _{DS(on)}	Static drain-source on- resistance	V _{GS} = 10 V, I _D = 4 A		0.290	0.355	Ω

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
C _{iss}	Input capacitance		1	704	ı	pF
Coss	Output capacitance	V _{DS} = 100 V, f = 1 MHz,	1	38	ı	pF
C _{rss}	Reverse transfer capacitance	$V_{GS} = 0 V$	-	1.2	-	pF
Coss eq. (1)	Equivalent output capacitance	$V_{DS} = 0 \text{ V to } 480 \text{ V},$ $V_{GS} = 0 \text{ V}$	-	140	-	pF
R _G	Intrinsic gate resistance	f = 1 MHz open drain	-	5.3	-	Ω
Q_g	Total gate charge	V _{DD} = 480 V, I _D = 12 A,	1	19	ı	nC
Q_{gs}	Gate-source charge	V _{GS} = 10 V (see <i>Figure 15</i> :	- 1	3.3	•	nC
Q_{gd}	Gate-drain charge	"Gate charge test circuit")	-	9.5	-	nC

Notes:

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t _{d(on)}	Turn-on delay time	$V_{DD} = 300 \text{ V}, I_D = 6 \text{ A}$	-	10.5	-	ns
t _r	Rise time	$R_G = 4.7 \Omega$, $V_{GS} = 10 V$ (see Figure 14: "Switching times	-	9.5	-	ns
t _{d(off)}	Turn-off-delay time	test circuit for resistive load"	1	58	ı	ns
t _f	Fall time	and Figure 19: "Switching time waveform")	-	18.5	-	ns

 $^{^{(1)}}C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 8: Source drain diode

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I _{SD}	Source-drain current		-		8	Α
I _{SDM} ⁽¹⁾	Source-drain current (pulsed)		-		32	А
V _{SD} ⁽²⁾	Forward on voltage	V _{GS} = 0 V, I _{SD} = 8 A	1		1.6	V
t _{rr}	Reverse recovery time		-	316		ns
Q _{rr}	Reverse recovery charge	I _{SD} = 12 A, di/dt = 100 A/μs, V _{DD} = 60 V (see <i>Figure 16: "Test circuit for inductive load switching and diode recovery times"</i>)		3.25		μC
I _{RRM}	Reverse recovery current			20.5		А
t _{rr}	Reverse recovery time		-	455		ns
Q _{rr}	Reverse recovery charge	I_{SD} = 12 A, di/dt = 100 A/ μ s, V_{DD} = 60 V, T_{j} = 150 °C (see Figure 16: "Test circuit for inductive load switching and diode		4.8		μC
I _{RRM}	Reverse recovery current	recovery times")	-	21		Α

Notes:

Table 9: Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1 \text{ mA}, I_{D} = 0 \text{ A}$	30	1	ı	V

⁽¹⁾Pulse width is limited by safe operating area

 $^{^{(2)}\}text{Pulse}$ test: pulse duration = 300 $\mu\text{s},$ duty cycle 1.5%

2.1 Electrical characteristics (curves)

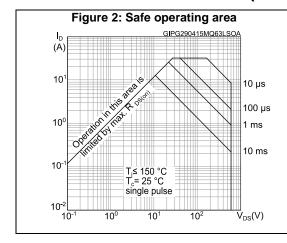


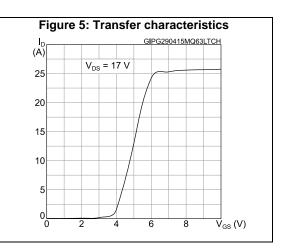
Figure 3: Thermal impedance

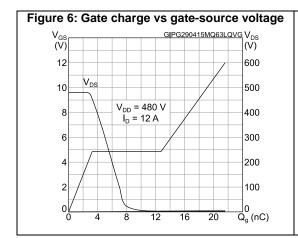
ZthPowerFlat $5x6_19$ 0.2

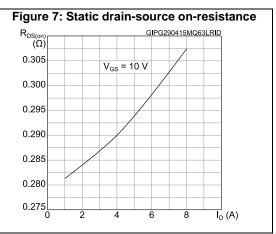
10⁻¹
0.1

0.05
0.02
0.01

Zth = k RthJ-c $\delta = t_p/\tau$ 10⁻³
10⁻⁶
10⁻⁵
10⁻⁴
10⁻³
10⁻¹







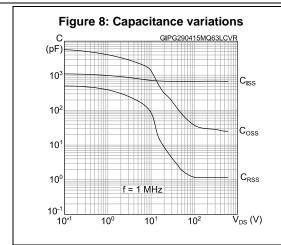
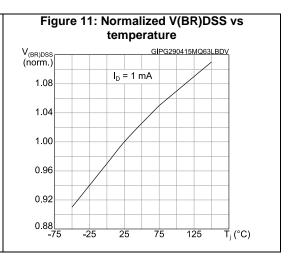
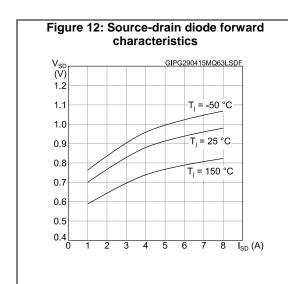
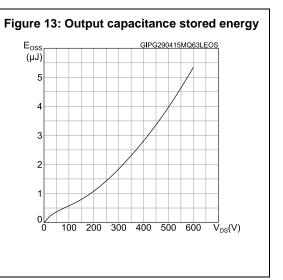


Figure 10: Normalized on-resistance vs temperature

R_{DS(on)} GIPG290415MQ63LRON
(norm.)
2.2
1.8
1.4
1.0
0.6
0.2
-75 -25 25 75 125 T_j (°C)

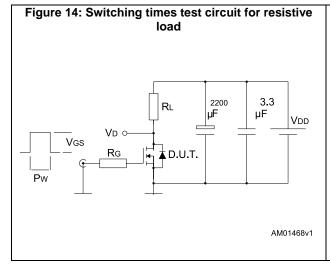






Test circuits STL16N60M2

3 **Test circuits**



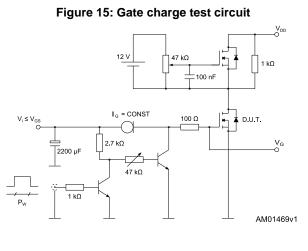


Figure 16: Test circuit for inductive load switching and diode recovery times

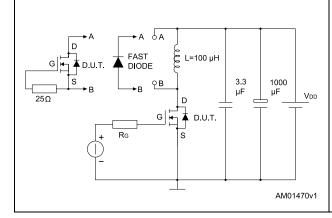
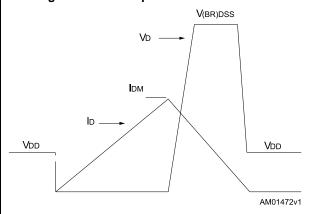
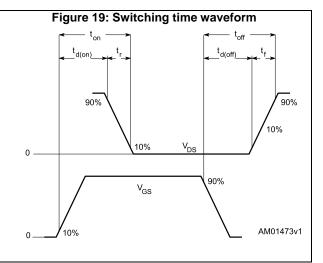


Figure 17: Unclamped inductive load test circuit 2200 Vdd AM01471v1

Figure 18: Unclamped inductive waveform





4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: **www.st.com**. ECOPACK® is an ST trademark.



4.1 PowerFLAT™ 5x6 HV package information

Figure 20: PowerFLAT™ 5x6 HV package outline

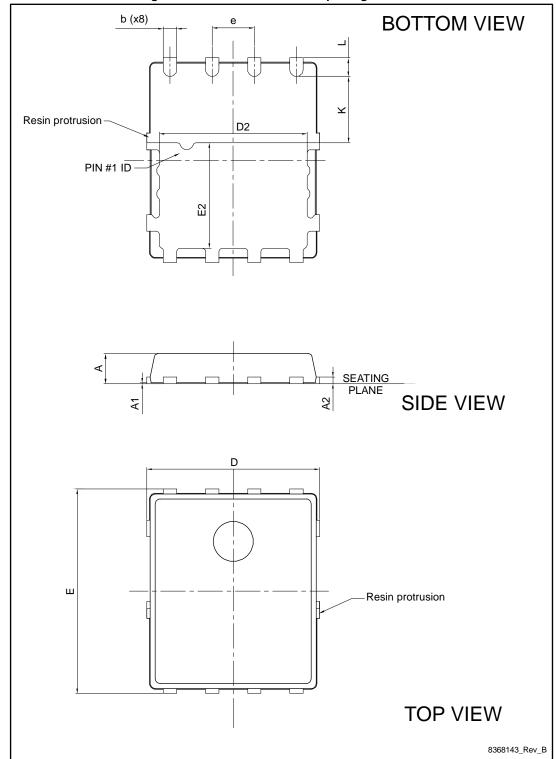
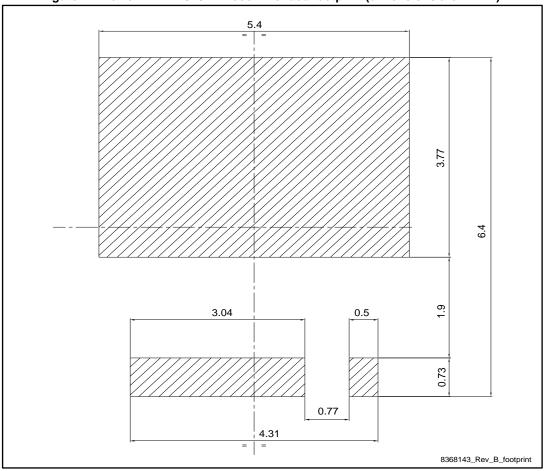


Table 10: PowerFLAT™ 5x6 HV mechanical data

Dim.	mm					
Dim.	Min.	Тур.	Max.			
Α	0.80		1.00			
A1	0.02		0.05			
A2		0.25				
b	0.30		0.50			
D	5.00	5.20	5.40			
Е	5.95	6.15	6.35			
D2	4.30	4.40	4.50			
E2	3.10	3.20	3.30			
е		1.27				
L	0.50	0.55	0.60			
K	1.90	2.00	2.10			

Figure 21: PowerFLAT™ 5x6 HV recommended footprint (dimensions are in mm)



4.2 Packing information

Figure 22: PowerFLAT™ 5x6 tape (dimensions are in mm)

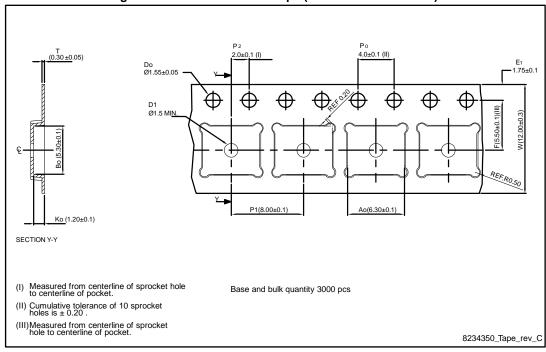
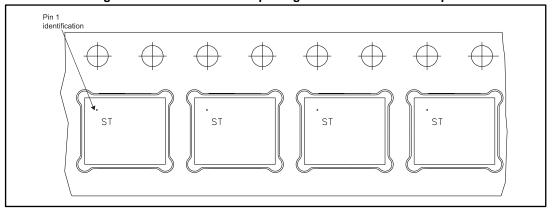


Figure 23: PowerFLAT™ 5x6 package orientation in carrier tape



8234350_Reel_rev_C

PART NO.

R25.00

R330 (+0)-4.0)

R1.10

R21.20

R2



Revision history STL16N60M2

5 Revision history

Table 11: Document revision history

Date	Revision	Changes
18-May-2015	1	First release.

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