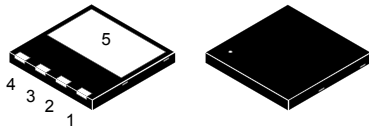
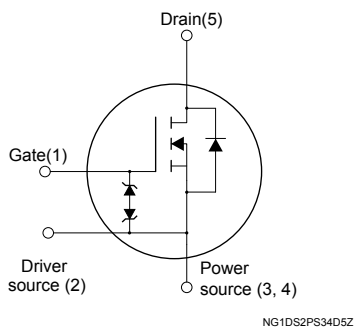


## N-channel 600 V, 0.280 $\Omega$ typ., 11 A, MDmesh DM2 Power MOSFET in a PowerFLAT 8x8 HV package


**PowerFLAT™ 8x8 HV**

**Product status link**
[STL19N60DM2](#)
**Product summary**

<b>Order code</b>	STL19N60DM2
<b>Marking</b>	19N60DM2
<b>Package</b>	PowerFLAT™ 8x8 HV
<b>Packing</b>	Tape and reel

### Features

Order code	$V_{DS}$	$R_{DS(on)}$ max.	$I_D$
STL19N60DM2	600 V	0.320 $\Omega$	11 A

- Fast-recovery body diode
- Extremely low gate charge and input capacitance
- Low on-resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected

### Applications

- Switching applications

### Description

This high-voltage N-channel Power MOSFET is part of the MDmesh DM2 fast-recovery diode series. It offers very low recovery charge ( $Q_{rr}$ ) and time ( $t_{rr}$ ) combined with low  $R_{DS(on)}$ , rendering it suitable for the most demanding high-efficiency converters and ideal for bridge topologies and ZVS phase-shift converters.

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	$\pm 25$	V
$I_D$	Drain current (continuous) at $T_{case} = 25\text{ }^\circ\text{C}$	11	A
	Drain current (continuous) at $T_{case} = 100\text{ }^\circ\text{C}$	6.8	
$I_{DM}^{(1)}$	Drain current (pulsed)	44	A
$P_{TOT}$	Total power dissipation at $T_{case} = 25\text{ }^\circ\text{C}$	90	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	40	V/ns
$dv/dt^{(3)}$	MOSFET $dv/dt$ ruggedness	50	
$T_{stg}$	Storage temperature range	-55 to 150	$^\circ\text{C}$
$T_j$	Operating junction temperature range		

- Pulse width is limited by safe operating area.
- $I_{SD} \leq 11\text{ A}$ ,  $di/dt=400\text{ A}/\mu\text{s}$ ,  $V_{DD} = 400\text{ V}$ ,  $V_{DS(peak)} < V_{(BR)DSS}$
- $V_{DS} \leq 480\text{ V}$

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	1.39	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	45	

- When mounted on an 1-inch<sup>2</sup> FR-4, 2oz Cu board

**Table 3. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}^{(1)}$	Avalanche current, repetitive or not repetitive	2.5	A
$E_{AS}^{(2)}$	Single pulse avalanche energy	380	mJ

- Pulse width is limited by  $T_{jmax}$ .
- Starting  $T_j = 25\text{ }^\circ\text{C}$ ,  $I_D = I_{AR}$ ,  $V_{DD} = 50\text{ V}$

## 2 Electrical characteristics

( $T_{\text{case}} = 25\text{ °C}$  unless otherwise specified)

**Table 4. Static**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage	$V_{\text{GS}} = 0\text{ V}$ , $I_{\text{D}} = 1\text{ mA}$	600			V
$I_{\text{DSS}}$	Zero gate voltage drain current	$V_{\text{GS}} = 0\text{ V}$ , $V_{\text{DS}} = 600\text{ V}$			1	$\mu\text{A}$
		$V_{\text{GS}} = 0\text{ V}$ , $V_{\text{DS}} = 600\text{ V}$ , $T_{\text{case}} = 125\text{ °C}^{(1)}$			100	
$I_{\text{GSS}}$	Gate-body leakage current	$V_{\text{DS}} = 0\text{ V}$ , $V_{\text{GS}} = \pm 25\text{ V}$			$\pm 5$	$\mu\text{A}$
$V_{\text{GS}(\text{th})}$	Gate threshold voltage	$V_{\text{DS}} = V_{\text{GS}}$ , $I_{\text{D}} = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{\text{DS}(\text{on})}$	Static drain-source on-resistance	$V_{\text{GS}} = 10\text{ V}$ , $I_{\text{D}} = 5.5\text{ A}$		0.280	0.320	$\Omega$

1. Defined by design, not subject to production test.

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{\text{iss}}$	Input capacitance	$V_{\text{DS}} = 100\text{ V}$ , $f = 1\text{ MHz}$ , $V_{\text{GS}} = 0\text{ V}$	-	800	-	pF
$C_{\text{oss}}$	Output capacitance		-	40	-	pF
$C_{\text{rss}}$	Reverse transfer capacitance		-	1.33	-	pF
$C_{\text{oss eq.}}^{(1)}$	Equivalent output capacitance	$V_{\text{DS}} = 0$ to $480\text{ V}$ , $f = 1\text{ MHz}$ , $V_{\text{GS}} = 0\text{ V}$	-	80	-	pF
$R_{\text{G}}$	Intrinsic gate resistance	$f = 1\text{ MHz}$ , $I_{\text{D}} = 0\text{ A}$	-	5.6	-	$\Omega$
$Q_{\text{g}}$	Total gate charge	$V_{\text{DD}} = 480\text{ V}$ , $I_{\text{D}} = 12\text{ A}$ , $V_{\text{GS}} = 0$ to $10\text{ V}$ (see Figure 14. Test circuit for gate charge behavior)	-	20	-	nC
$Q_{\text{gs}}$	Gate-source charge		-	5.2	-	nC
$Q_{\text{gd}}$	Gate-drain charge		-	8.5	-	nC

1.  $C_{\text{oss eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{\text{oss}}$  when  $V_{\text{DS}}$  increases from 0 to 80%  $V_{\text{DSS}}$

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{\text{d}(\text{on})}$	Turn-on delay time	$V_{\text{DD}} = 300\text{ V}$ , $I_{\text{D}} = 6\text{ A}$ , $R_{\text{G}} = 4.7\text{ }\Omega$ , $V_{\text{GS}} = 10\text{ V}$ (see Figure 13. Switching times test circuit for resistive load and Figure 18. Switching time waveform)	-	13.5	-	ns
$t_{\text{r}}$	Rise time		-	8	-	ns
$t_{\text{d}(\text{off})}$	Turn-off delay time		-	9.5	-	ns
$t_{\text{f}}$	Fall time		-	32.5	-	ns

**Table 7. Source-drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		11	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		44	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$ , $I_{SD} = 11\text{ A}$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 12\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 60\text{ V}$ (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	125		ns
$Q_{rr}$	Reverse recovery charge		-	0.675		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	11		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 12\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 60\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$ (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	190		ns
$Q_{rr}$	Reverse recovery charge		-	1.225		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	13		A

1. Pulse width is limited by safe operating area.
2. Pulse test: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

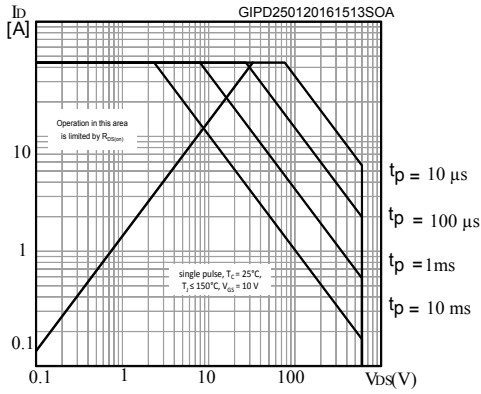


Figure 2. Thermal impedance

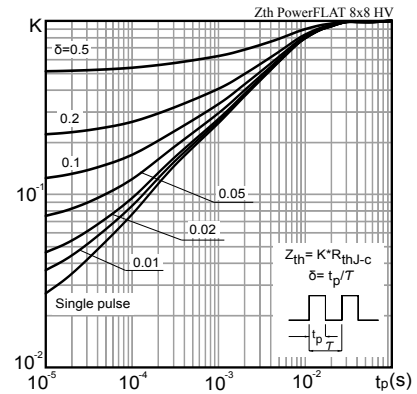


Figure 3. Output characteristics

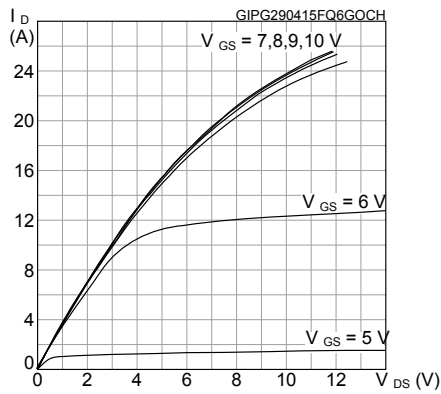


Figure 4. Transfer characteristics

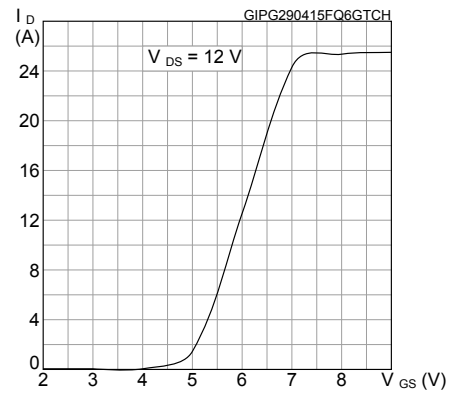


Figure 5. Gate charge vs gate-source voltage

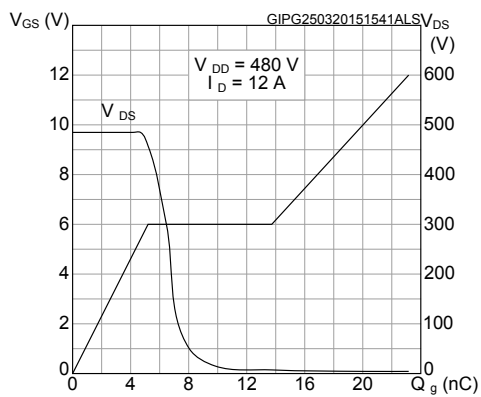


Figure 6. Static drain-source on-resistance

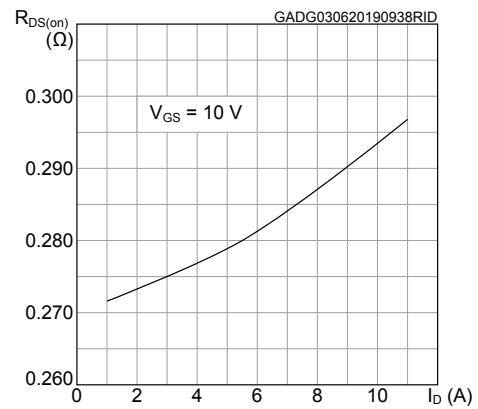


Figure 7. Capacitance variations

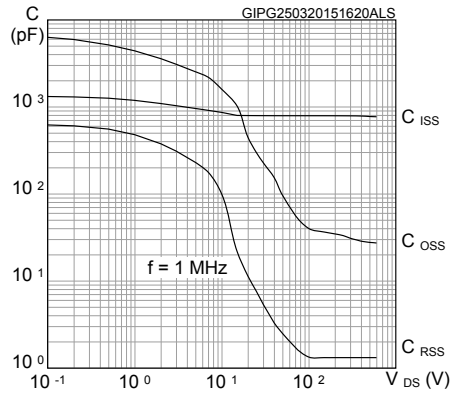


Figure 8. Normalized gate threshold voltage vs temperature

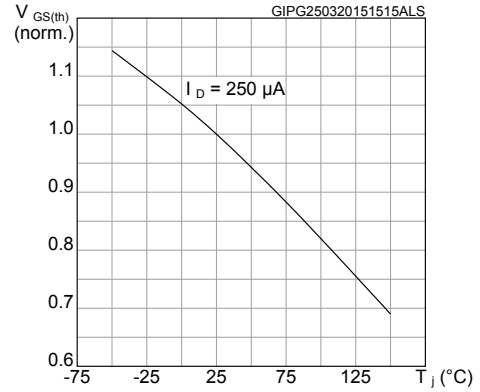


Figure 9. Normalized on-resistance vs temperature

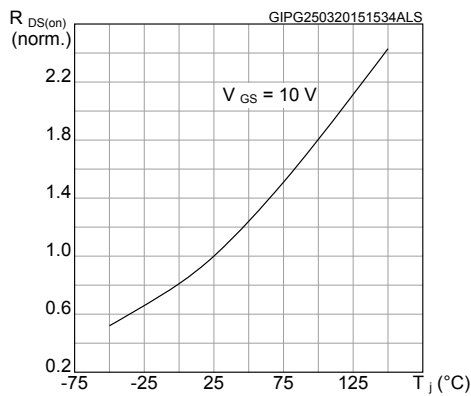


Figure 10. Normalized V<sub>(BR)DSS</sub> vs temperature

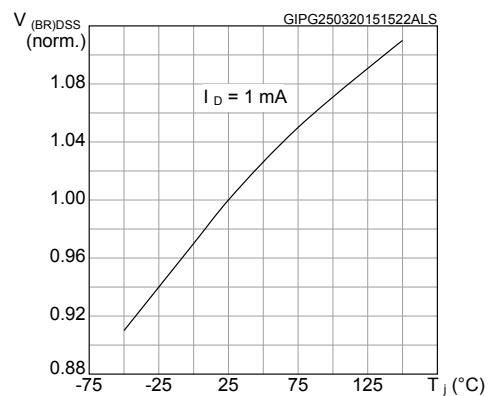


Figure 11. Source-drain diode forward characteristics

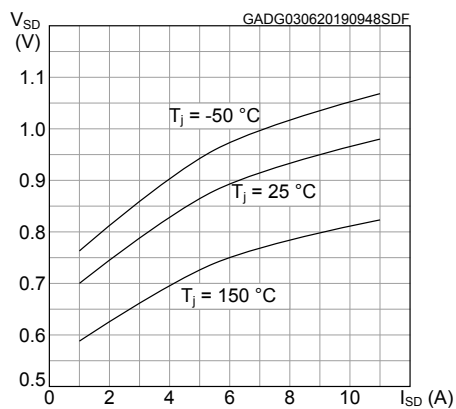
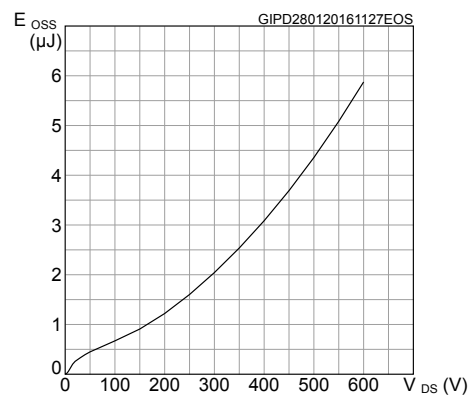
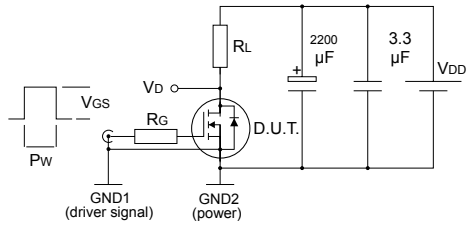


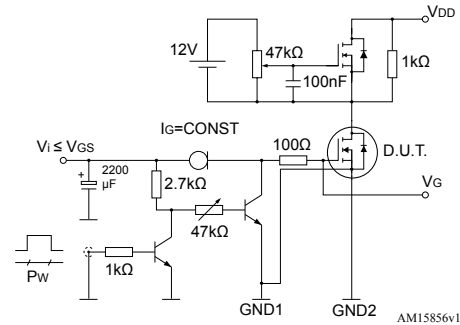
Figure 12. Output capacitance stored energy



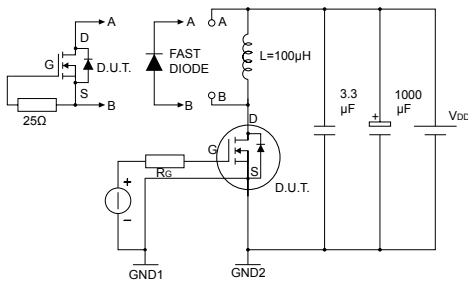
### 3 Test circuits

**Figure 13. Switching times test circuit for resistive load**


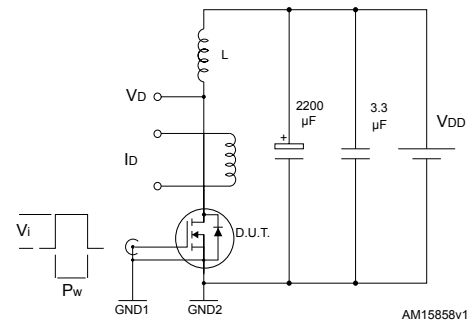
AM15855v1

**Figure 14. Test circuit for gate charge behavior**


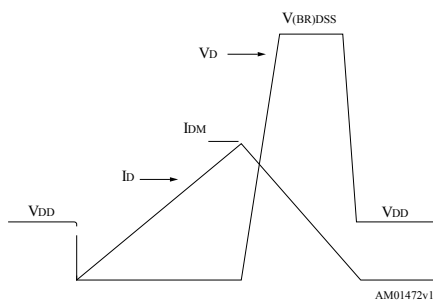
AM15856v1

**Figure 15. Test circuit for inductive load switching and diode recovery times**


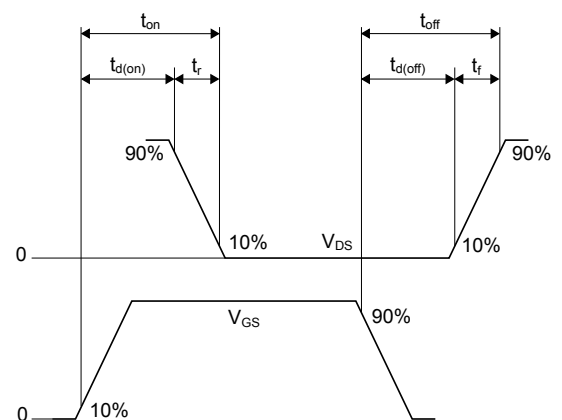
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**Figure 16. Unclamped inductive load test circuit**


AM15858v1

**Figure 17. Unclamped inductive waveform**


AM01472v1

**Figure 18. Switching time waveform**


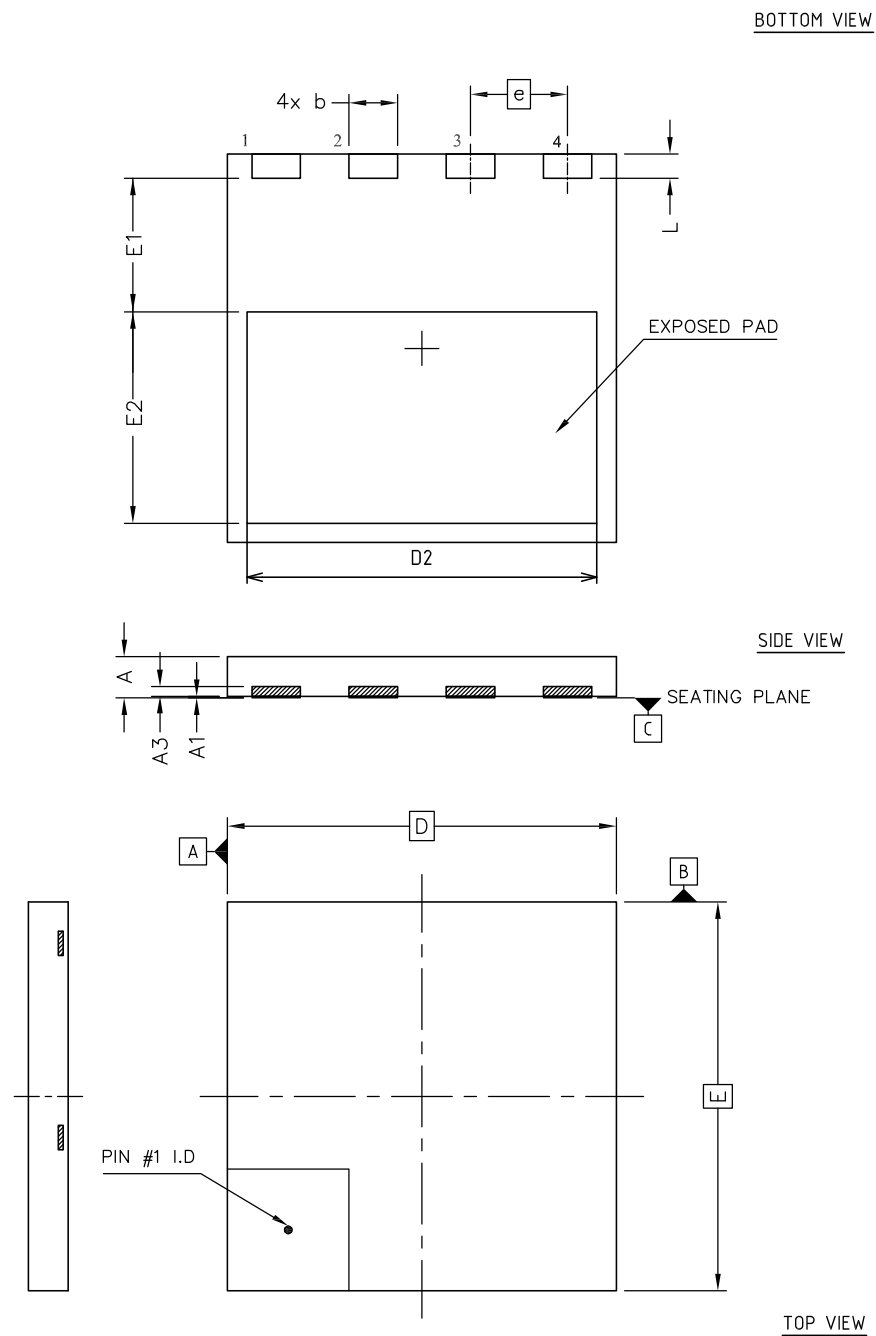
AM01473v1

## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 4.1 PowerFLAT 8x8 HV package information

Figure 19. PowerFLAT 8x8 HV package outline



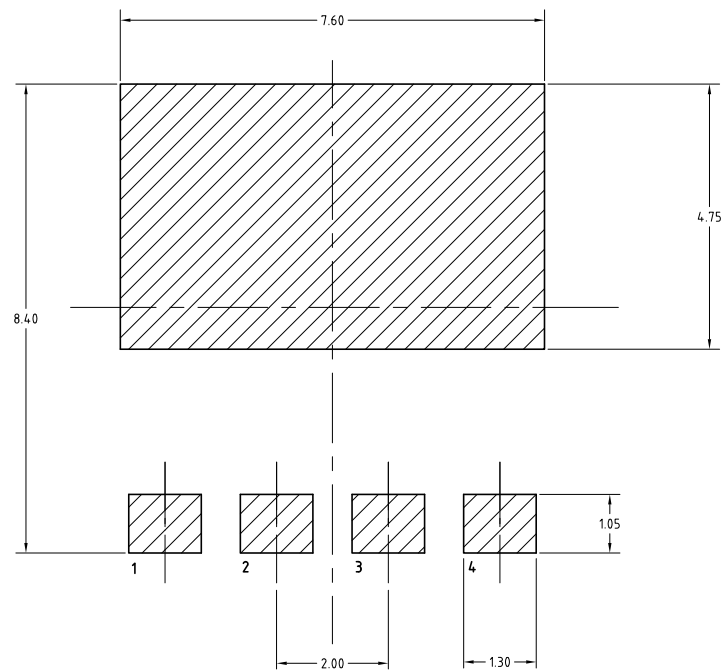
8222871\_Rev\_4



**Table 8. PowerFLAT 8x8 HV mechanical data**

Ref.	Dimensions (in mm)		
	Min.	Typ.	Max.
A	0.75	0.85	0.95
A1	0.00		0.05
A3	0.10	0.20	0.30
b	0.90	1.00	1.10
D	7.90	8.00	8.10
E	7.90	8.00	8.10
D2	7.10	7.20	7.30
E1	2.65	2.75	2.85
E2	4.25	4.35	4.45
e	2.00 BSC		
L	0.40	0.50	0.60

**Figure 20. PowerFLAT 8x8 HV footprint**

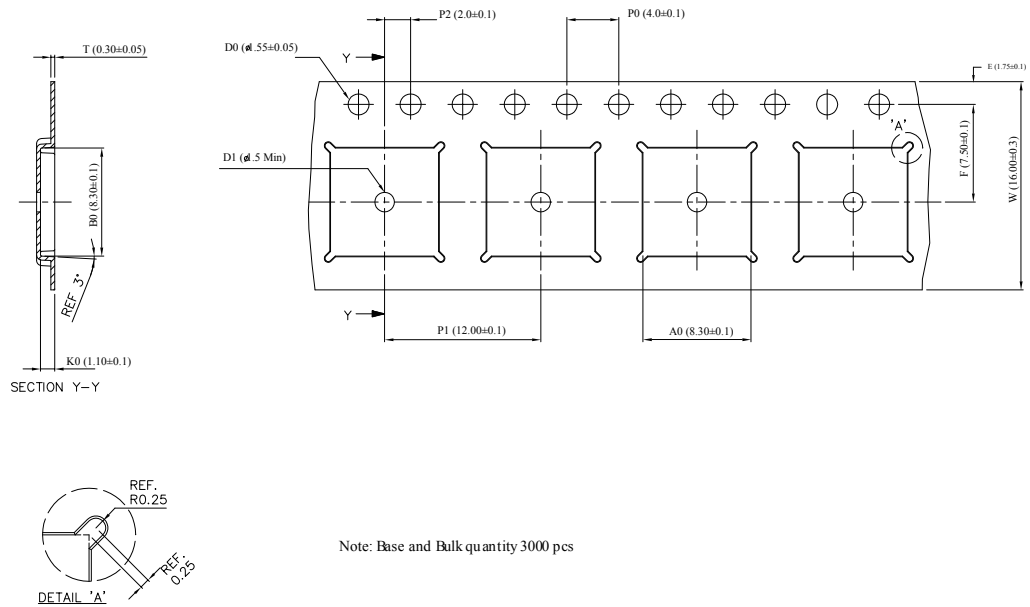


8222871\_REV\_4\_footprint

*Note: All dimensions are in millimeters.*

## 4.2 PowerFLAT 8x8 HV packing information

Figure 21. PowerFLAT 8x8 HV tape



8229819\_Tape\_revA

Note: All dimensions are in millimeters.

Figure 22. PowerFLAT 8x8 HV package orientation in carrier tape

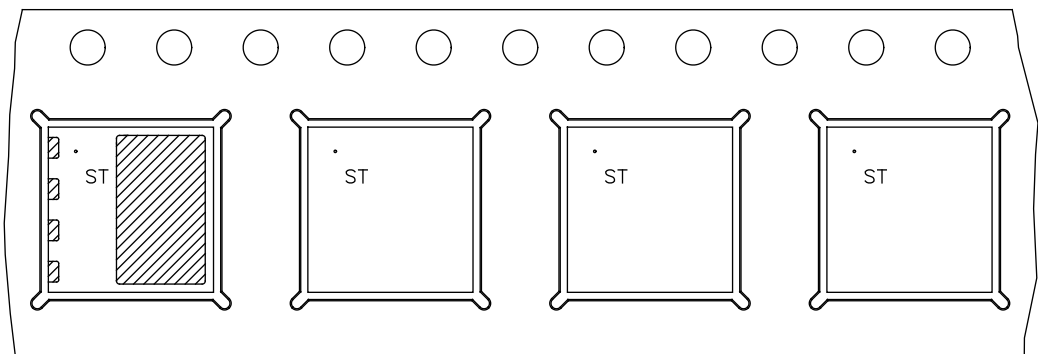
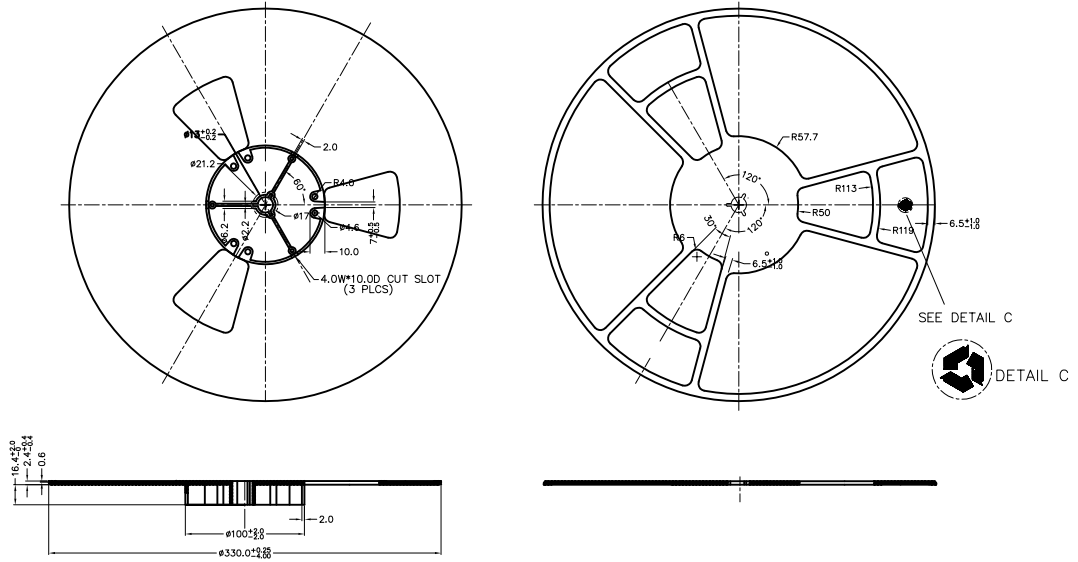


Figure 23. PowerFLAT 8x8 HV reel



8229819\_Reel\_revA

Note: All dimensions are in millimeters.

## Revision history

**Table 9. Document revision history**

Date	Version	Changes
08-Aug-2014	1	Initial release.
05-Jun-2019	2	Modified <a href="#">Table 4. Static</a> , <a href="#">Table 5. Dynamic</a> , <a href="#">Table 6. Switching times</a> and <a href="#">Table 7. Source-drain diode</a> . Added <a href="#">Section 2.1 Electrical characteristics (curves)</a> . Modified <a href="#">Section 4.1 PowerFLAT 8x8 HV package information</a> . Minor text changes.

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[SSM6P69NU,LF](#) [DMP22D4UFO-7B](#)