

N-channel 60 V, 1.2 mΩ typ., 120 A STripFET™ F7 Power MOSFET in a PowerFLAT™ 5x6 package

Datasheet - production data

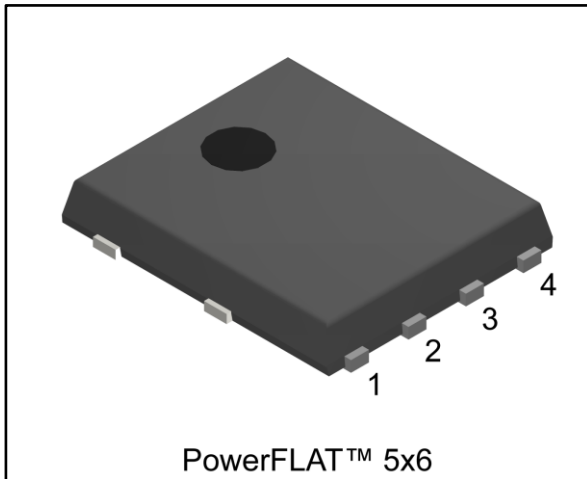
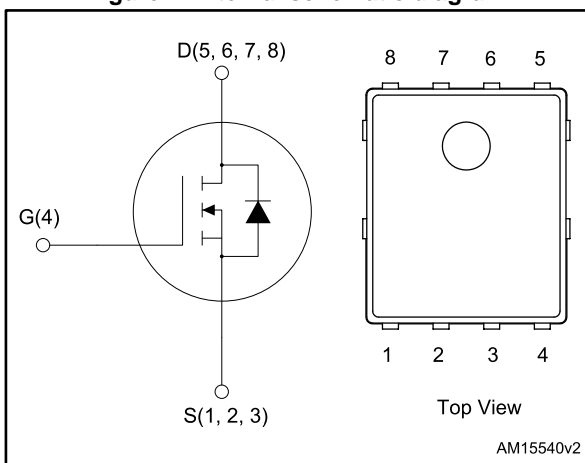


Figure 1: Internal schematic diagram



Features

| Order code | V _{DS} | R _{DS(on)} max. | I _D |
|------------|-----------------|--------------------------|----------------|
| STL220N6F7 | 60 V | 1.4 mΩ | 120 A |

- Among the lowest R_{DS(on)} on the market
- Excellent FoM (figure of merit)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness

Applications

- Switching applications

Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Table 1: Device summary

| Order code | Marking | Package | Packaging |
|------------|---------|----------------|---------------|
| STL220N6F7 | 220N6F7 | PowerFLAT™ 5x6 | Tape and reel |

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1 Electrical ratings

Table 2: Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|-------------------|-----------------------------------------------------------------------------------------------------|------------|------------------|
| V_{DS} | Drain-source voltage | 60 | V |
| V_{GS} | Gate-source voltage | ± 20 | V |
| $I_D^{(1)}$ | Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$ | 120 | A |
| $I_D^{(1)}$ | Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$ | 120 | A |
| $I_{DM}^{(1)(2)}$ | Drain current (pulsed) | 480 | A |
| $I_D^{(3)}$ | Drain current (continuous) at $T_{pcb} = 25\text{ }^\circ\text{C}$ | 40 | A |
| $I_D^{(3)}$ | Drain current (continuous) at $T_{pcb} = 100\text{ }^\circ\text{C}$ | 28.5 | A |
| $I_{DM}^{(2)(3)}$ | Drain current (pulsed) | 160 | A |
| E_{AS} | Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$, $I_{AS} = 20\text{ A}$) | 900 | mJ |
| $P_{TOT}^{(1)}$ | Total dissipation at $T_C = 25\text{ }^\circ\text{C}$ | 188 | W |
| $P_{TOT}^{(3)}$ | Total dissipation at $T_{pcb} = 25\text{ }^\circ\text{C}$ | 4.8 | W |
| T_J | Operating junction temperature range | -55 to 175 | $^\circ\text{C}$ |
| | Storage temperature range | | |

Notes:

(1) This value is rated according to R_{thj-c} .

(2) Pulse width limited by safe operating area.

(3) This value is rated according to $R_{thj-pcb}$.

Table 3: Thermal data

| Symbol | Parameter | Value | Unit |
|---------------------|----------------------------------|-------|--------------------|
| $R_{thj-pcb}^{(1)}$ | Thermal resistance junction-pcb | 31.3 | $^\circ\text{C/W}$ |
| $R_{thj-case}$ | Thermal resistance junction-case | 0.8 | $^\circ\text{C/W}$ |

Notes:

(1) When mounted on FR-4 board of 1 inch², 2oz Cu, $t < 10\text{ s}$.

2 Electrical characteristics

($T_C = 25\text{ }^\circ\text{C}$ unless otherwise specified)

Table 4: On /off states

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------|-----------------------------------|----------------------------------------------------|------|------|------|---------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $I_D = 1\text{ mA}$, $V_{GS} = 0\text{ V}$ | 60 | | | V |
| I_{DSS} | Zero gate voltage drain current | $V_{GS} = 0\text{ V}$ $V_{DS} = 60\text{ V}$ | | | 1 | μA |
| I_{GSS} | Gate-body leakage current | $V_{GS} = 20\text{ V}$, $V_{DS} = 0\text{ V}$ | | | 100 | nA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$ | 2 | | 4 | V |
| $R_{DS(on)}$ | Static drain-source on-resistance | $V_{GS} = 10\text{ V}$, $I_D = 20\text{ A}$ | | 1.2 | 1.4 | m Ω |

Table 5: Dynamic

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------|------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|------|
| C_{iss} | Input capacitance | $V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$ | - | 6500 | - | pF |
| C_{oss} | Output capacitance | | - | 3200 | - | pF |
| C_{rss} | Reverse transfer capacitance | | - | 230 | - | pF |
| Q_g | Total gate charge | $V_{DD} = 30\text{ V}$, $I_D = 40\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 14: "Test circuit for gate charge behavior") | - | 98 | - | nC |
| Q_{gs} | Gate-source charge | | - | 38 | - | nC |
| Q_{gd} | Gate-drain charge | | - | 28 | - | nC |

Table 6: Switching times

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|--------------|---------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|------|
| $t_{d(on)}$ | Turn-on delay time | $V_{DD} = 30\text{ V}$, $I_D = 20\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 13: "Test circuit for resistive load switching times" and Figure 18: "Switching time waveform") | - | 41 | - | ns |
| t_r | Rise time | | - | 45 | - | ns |
| $t_{d(off)}$ | Turn-off delay time | | - | 68 | - | ns |
| t_f | Fall time | | - | 35 | - | ns |

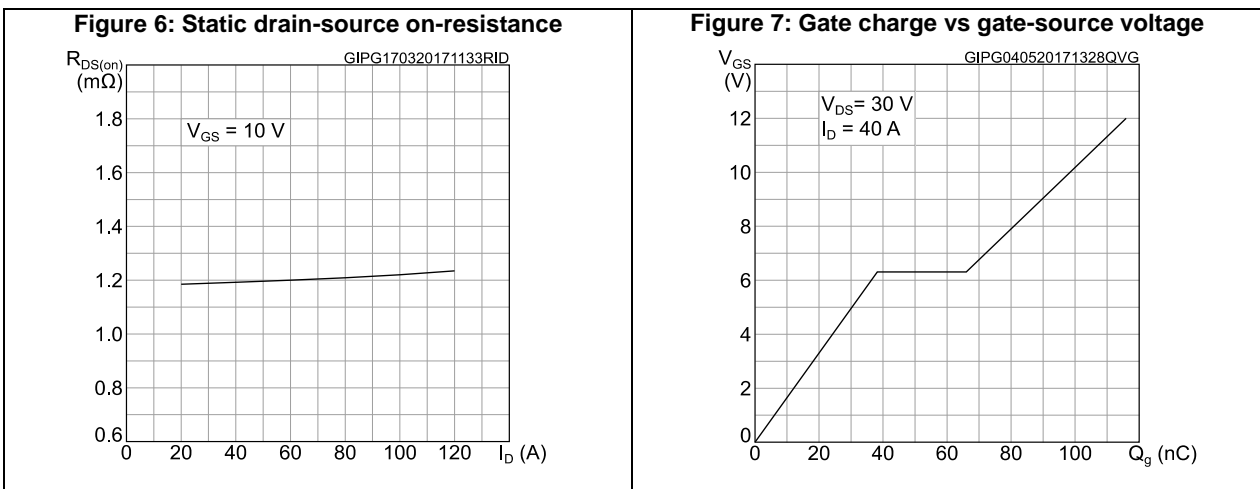
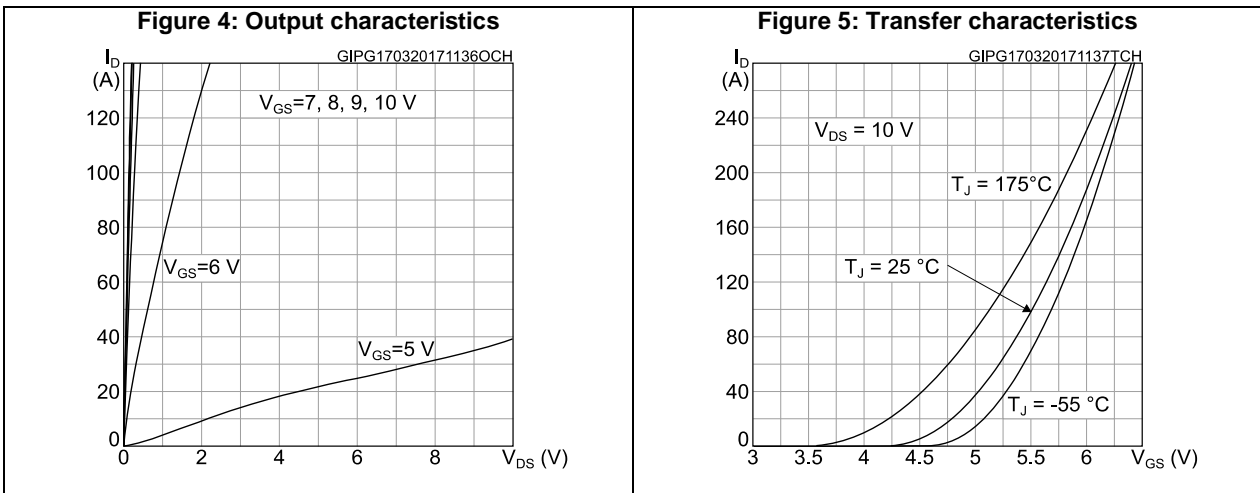
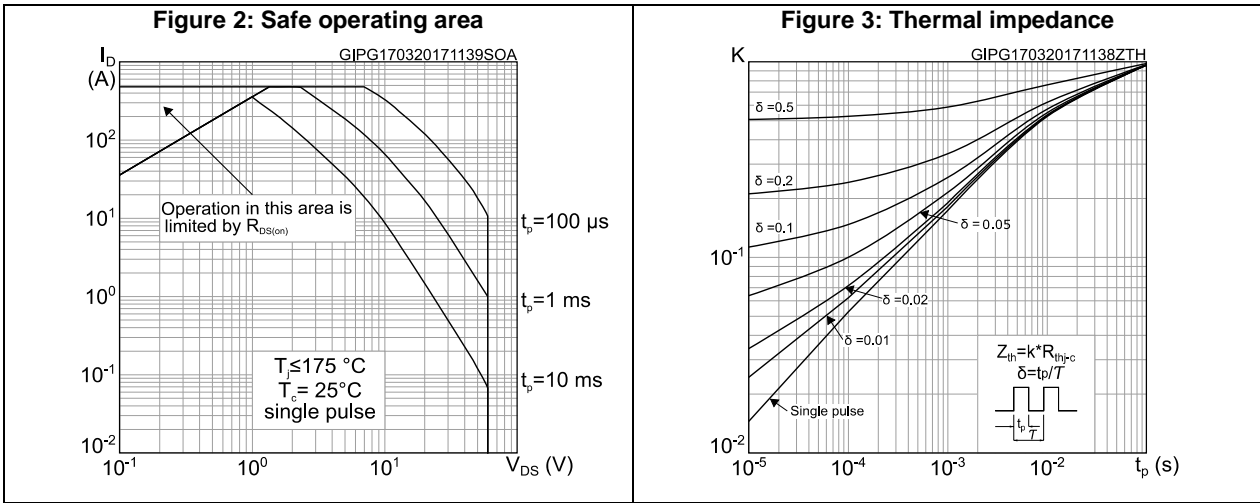
Table 7: Source-drain diode

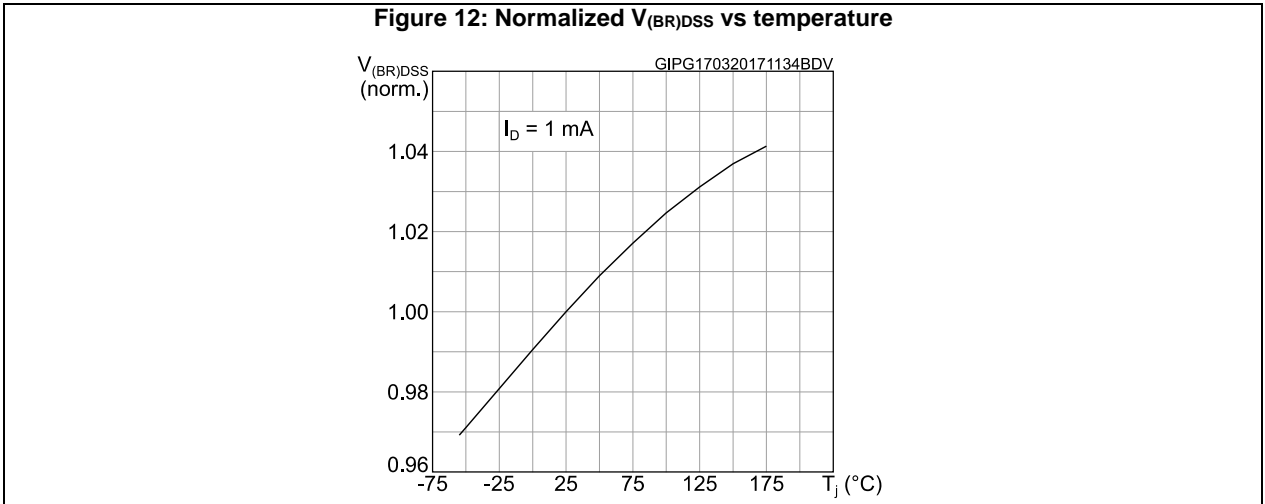
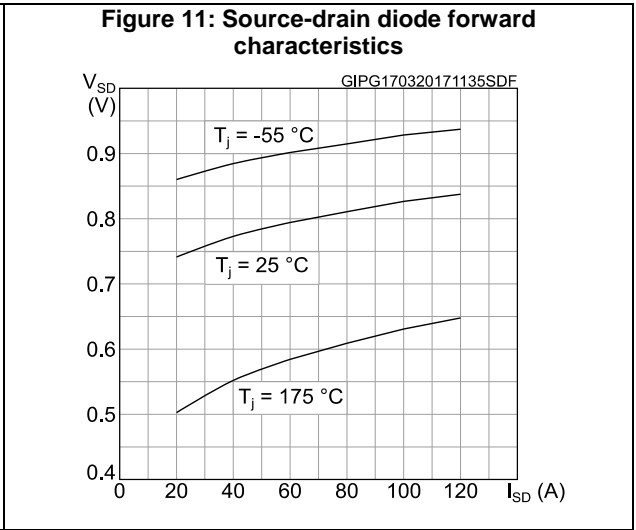
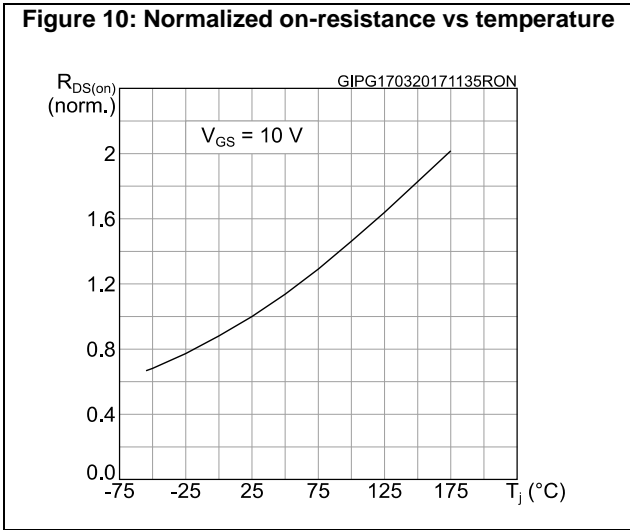
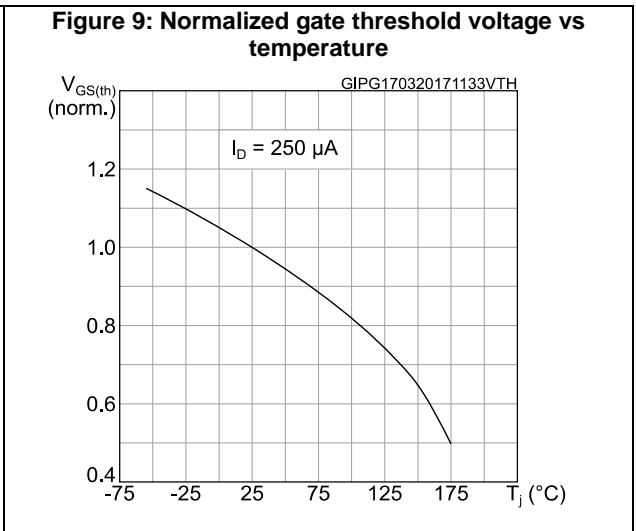
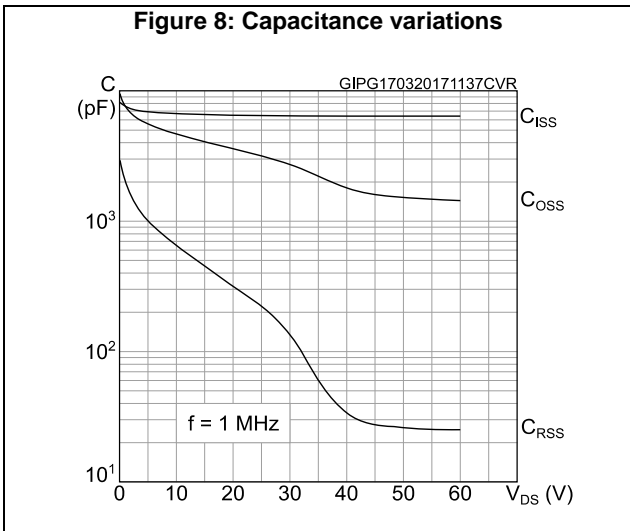
| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|----------------|--------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|------|
| $V_{SD}^{(1)}$ | Forward on voltage | $I_{SD} = 40\text{ A}$, $V_{GS} = 0\text{ V}$ | - | | 1.2 | V |
| t_{rr} | Reverse recovery time | $I_D = 40\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 48\text{ V}$ (see Figure 15: "Test circuit for inductive load switching and diode recovery times") | - | 69 | | ns |
| Q_{rr} | Reverse recovery charge | | - | 103 | | nC |
| I_{RRM} | Reverse recovery current | | - | 3 | | A |

Notes:

⁽¹⁾Pulsed: pulse duration = 300 μs , duty cycle 1.5%

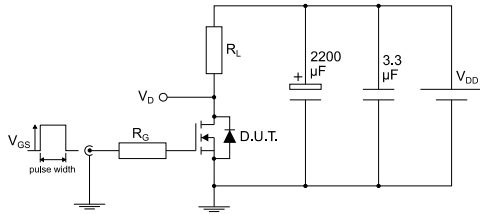
2.1 Electrical characteristics (curves)





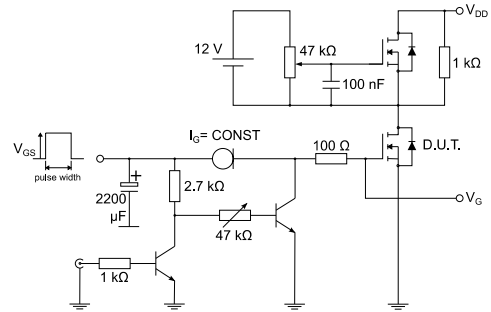
3 Test circuits

Figure 13: Test circuit for resistive load switching times



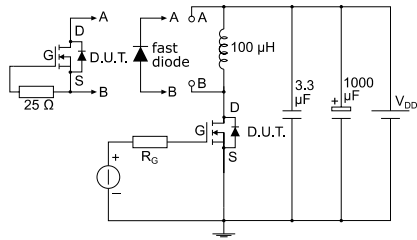
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Figure 14: Test circuit for gate charge behavior



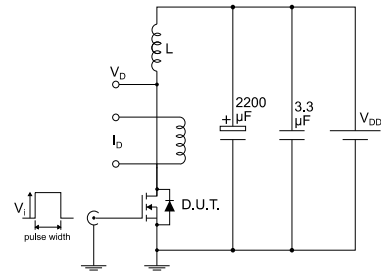
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Figure 15: Test circuit for inductive load switching and diode recovery times



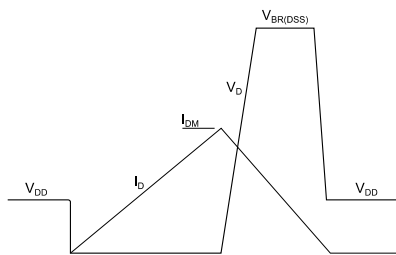
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Figure 16: Unclamped inductive load test circuit



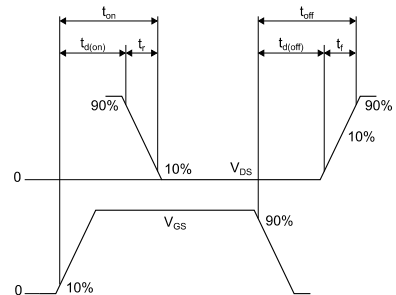
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Figure 17: Unclamped inductive waveform



AM01472v1

Figure 18: Switching time waveform



AM01473v1

4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 PowerFLAT 5x6 type C package mechanical data

Figure 19: PowerFLAT™ 5x6 type C package outline

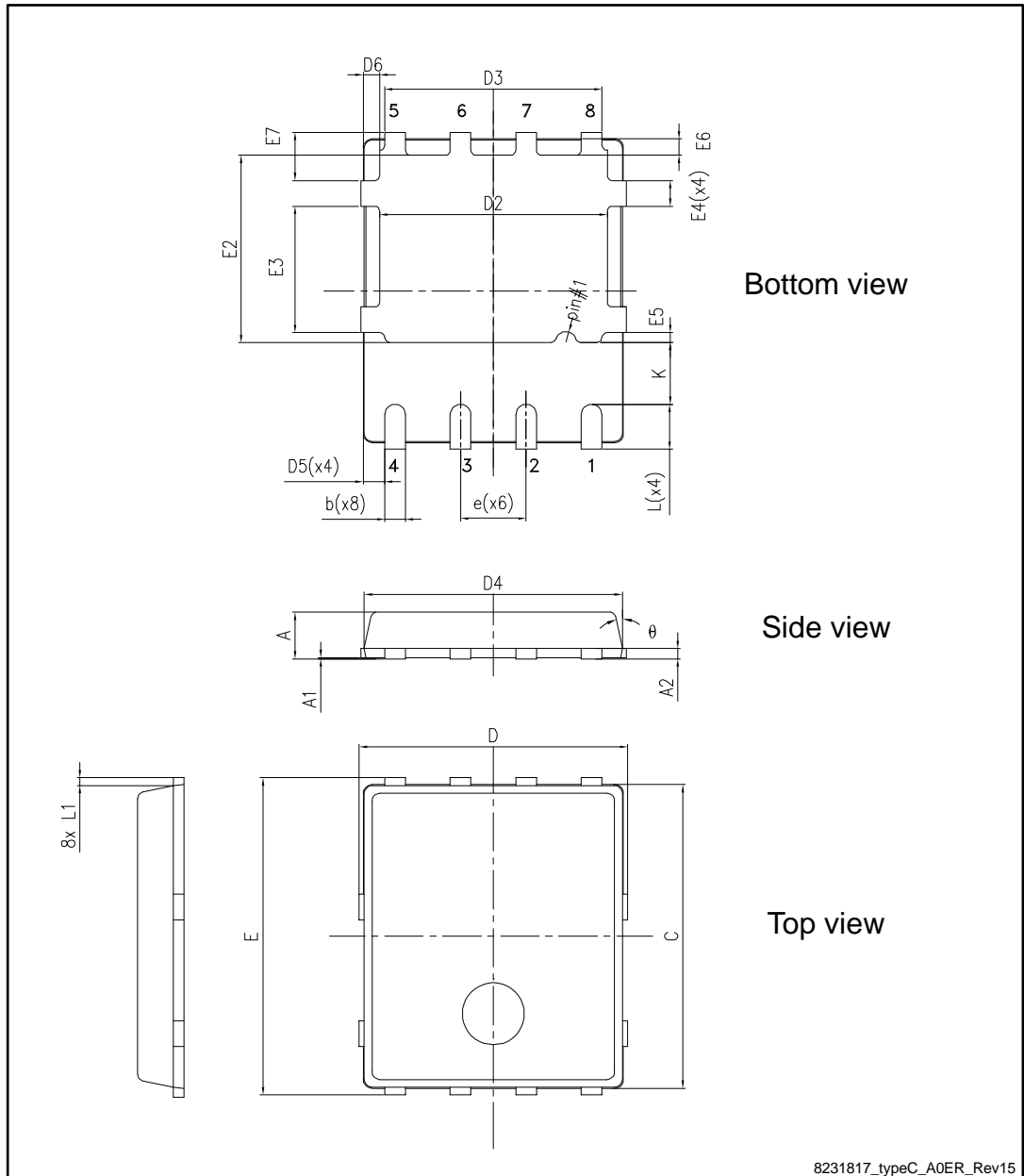
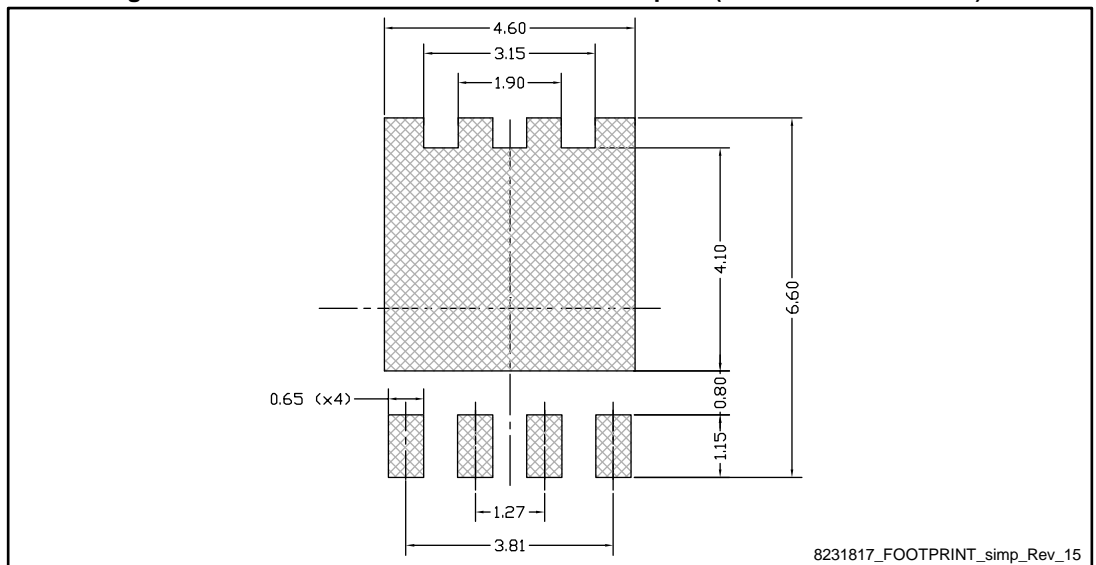


Table 8: PowerFLAT™ 5x6 type C package mechanical data

| Dim. | mm | | |
|------|-------|-------|-------|
| | Min. | Typ. | Max. |
| A | 0.80 | | 1.00 |
| A1 | 0.02 | | 0.05 |
| A2 | | 0.25 | |
| b | 0.30 | | 0.50 |
| C | 5.80 | 6.00 | 6.20 |
| D | 5.00 | 5.20 | 5.40 |
| D2 | 4.15 | | 4.45 |
| D3 | 4.05 | 4.20 | 4.35 |
| D4 | 4.80 | 5.00 | 5.20 |
| D5 | 0.25 | 0.40 | 0.55 |
| D6 | 0.15 | 0.30 | 0.45 |
| e | | 1.27 | |
| E | 5.95 | 6.15 | 6.35 |
| E2 | 3.50 | | 3.70 |
| E3 | 2.35 | | 2.55 |
| E4 | 0.40 | | 0.60 |
| E5 | 0.08 | | 0.28 |
| E6 | 0.20 | 0.325 | 0.45 |
| E7 | 0.75 | 0.90 | 1.05 |
| K | 1.05 | | 1.35 |
| L | 0.725 | | 1.025 |
| L1 | 0.05 | 0.15 | 0.25 |
| θ | 0° | | 12° |

Figure 20: PowerFLAT™ 5x6 recommended footprint (dimensions are in mm)



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4.2 PowerFLAT 5x6 packaging information

Figure 21: PowerFLAT™ 5x6 tape (dimensions are in mm)

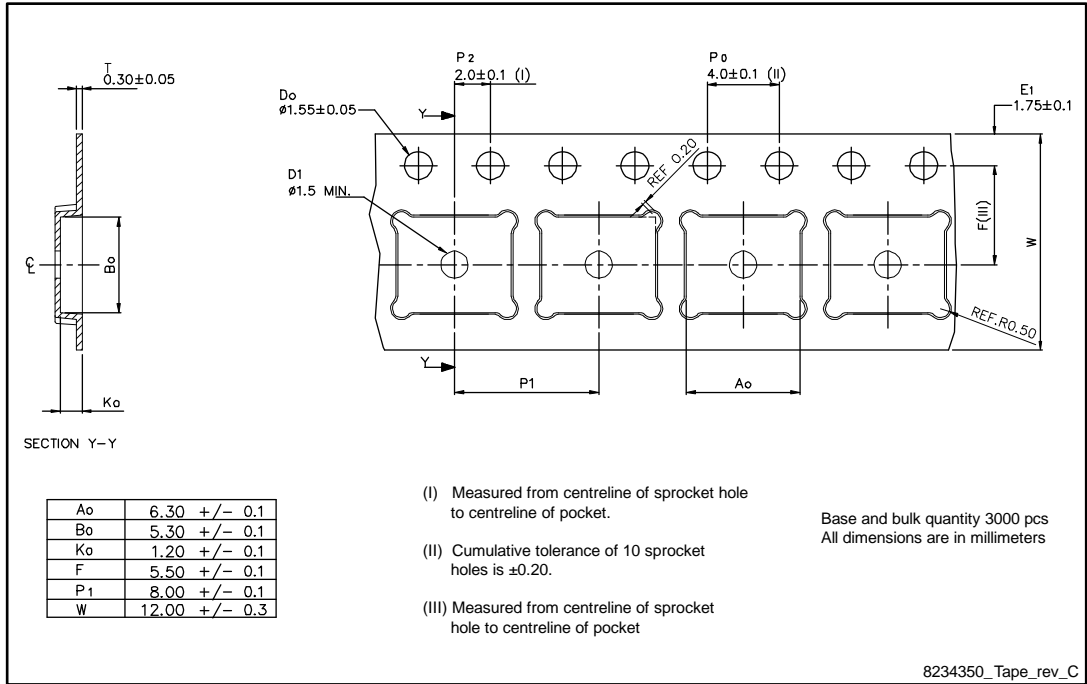


Figure 22: PowerFLAT™ 5x6 package orientation in carrier tape

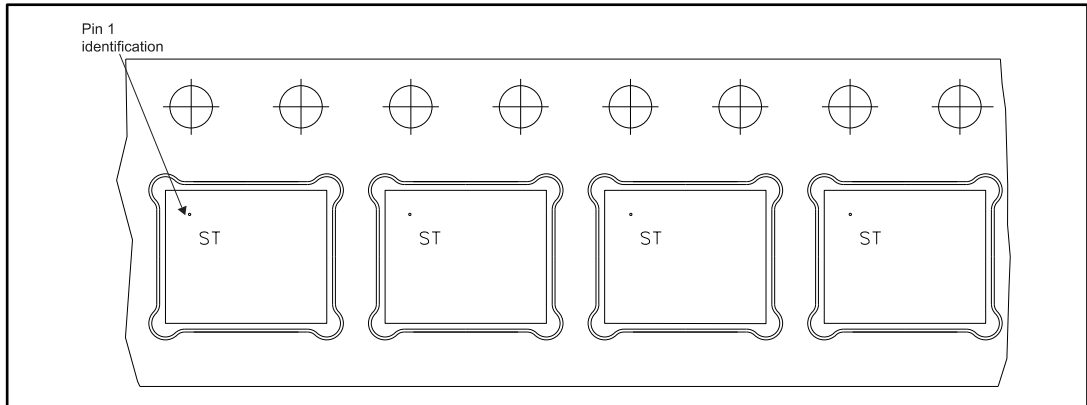
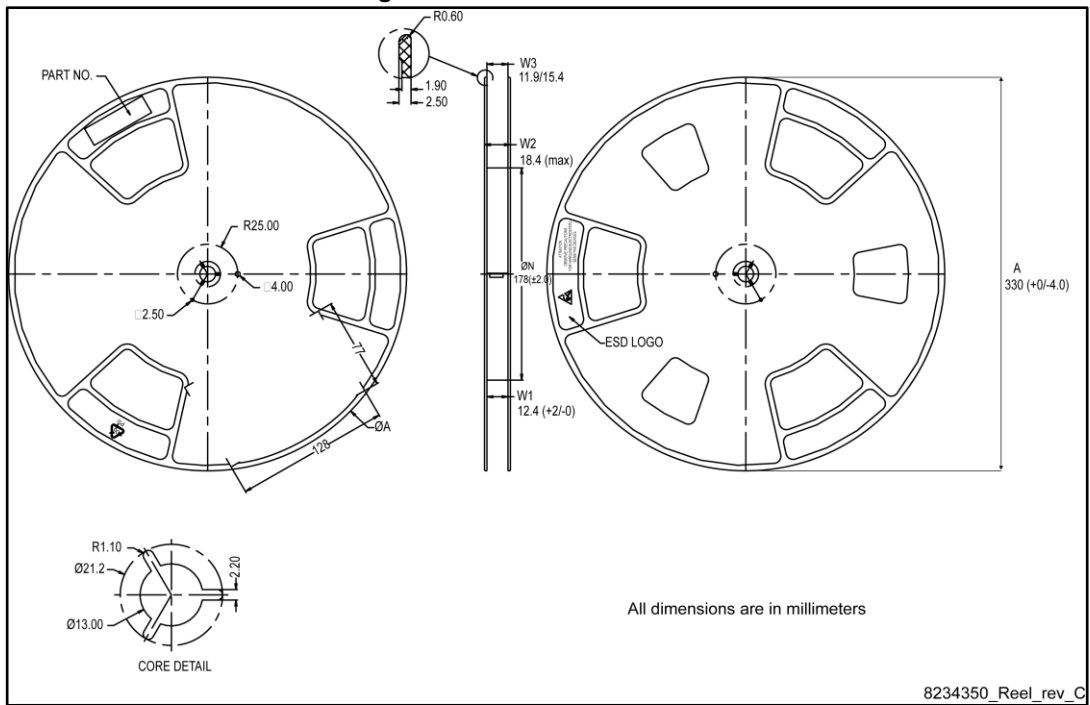


Figure 23: PowerFLAT™ 5x6 reel



5 Revision history

Table 9: Document revision history

| Date | Revision | Changes |
|-------------|----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 13-Jun-2014 | 1 | First release. |
| 22-Sep-2014 | 2 | Updated title, features and description in cover page. Updated <i>Table 2: "Absolute maximum ratings"</i> , <i>Table 4: "On /off states"</i> , <i>Table 5: "Dynamic"</i> , <i>Table 6: "Switching times"</i> and <i>Table 7: "Source-drain diode"</i> . Added <i>Section 3: "Electrical characteristics (curves)"</i> . |
| 14-Jan-2015 | 3 | Document status promoted from preliminary to production data. |
| 02-May-2017 | 4 | Modified title and features table on cover page. Modified <i>Table 2: "Absolute maximum ratings"</i> , <i>Table 4: "On /off states"</i> , <i>Table 5: "Dynamic"</i> , <i>Table 6: "Switching times"</i> and <i>Table 7: "Source-drain diode"</i> . Modified <i>Section 2.1: "Electrical characteristics (curves)"</i> . Minor text changes. |

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