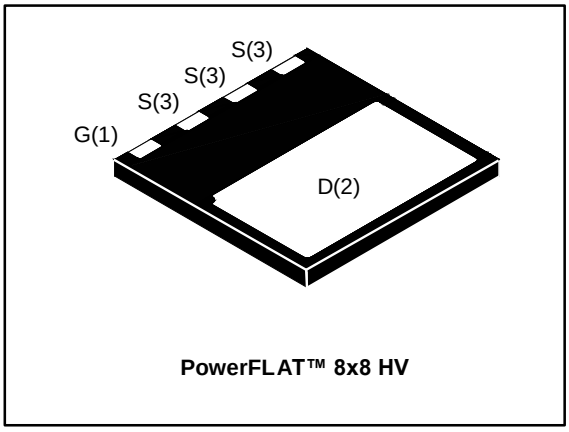
STL24N65M2

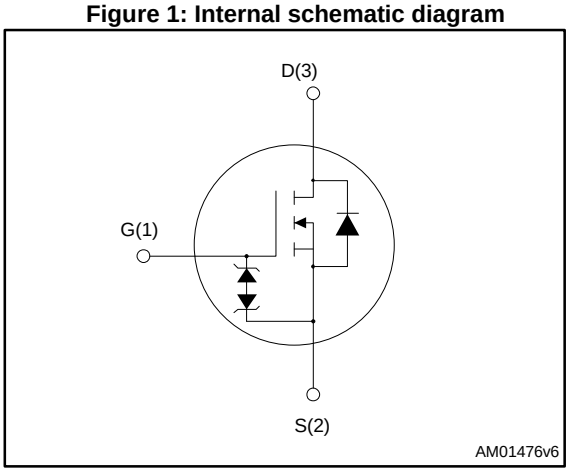
N-channel 650 V, 0.205 Ω typ., 14 A MDmesh M2 Power MOSFET in a PowerFLAT™ 8x8 HV package

Datasheet - production data



PowerFLAT™ 8x8 HV

Figure 1: Internal schematic diagram



Features

Order codes	V_{DS}	$R_{DS(on)}$ max	I_D
STL24N65M2	650 V	0.250 Ω	14 A

- Extremely low gate charge
- Excellent output capacitance (C_{oss}) profile
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using MDmesh™ M2 technology. Thanks to its strip layout and improved vertical structure, the devices exhibit low on-resistance and optimized switching characteristics, rendering it suitable for the most demanding high efficiency converters.

Table 1: Device summary

Order codes	Marking	Package	Packaging
STL24N65M2	24N65M2	PowerFLAT™ 8x8 HV	Tape and reel

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at T_C = 25 °C	14	A
I_D	Drain current (continuous) at T_C = 100 °C	8.8	A
I_{DM} (1)	Drain current (pulsed)	56	A
P_{TOT}	Total dissipation at T_C = 25 °C	125	W
dv/dt (2)	Peak diode recovery voltage slope	15	V/ns
dv/dt (3)	MOSFET dv/dt ruggedness	50	V/ns
T_{stg}	Storage temperature	- 55 to 150	°C
T_j	Max. operating junction temperature		

Notes:

(1)Pulse width limited by safe operating area.

(2)$I_{SD} \leq 14$ A, di/dt ≤ 400 A/µs; $V_{DS(peak)} < V_{(BR)DSS}$, V_{DD} = 80% $V_{(BR)DSS}$.

(3)$V_{DS} \leq 520$ V

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	1	°C/W
$R_{thj\text{-}pcb}$	Thermal resistance junction-pcb max (1)	50	°C/W

Notes:

(1)When mounted on 1 inch² FR-4, 2 Oz copper board.

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	2	A
E_{AS}	Single pulse avalanche energy (starting T_j=25°C, I_D= I_{AR}; V_{DD}=50V)	655	mJ

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 5: On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0 V	650			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0 V)	V_{DS} = 650 V			1	µA
		V_{DS} = 650 V, T_C=125 °C			100	µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0 V)	V_{GS} = ± 25 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 7 A		0.205	0.250	Ω

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	1060	-	pF
C_{oss}	Output capacitance		-	47.5	-	pF
C_{rss}	Reverse transfer capacitance		-	1.65	-	pF
$C_{oss\ eq.}$ (1)	Equivalent output capacitance	V_{DS} = 0 to 520 V, V_{GS} = 0 V	-	229	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz, I_D = 0	-	7	-	Ω
Q_g	Total gate charge	V_{DD} = 520 V, I_D = 16 A, V_{GS} = 10 V	-	29	-	nC
Q_{gs}	Gate-source charge		-	3.8	-	nC
Q_{gd}	Gate-drain charge		-	14	-	nC

Notes:

(1) $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 325 V, I_D = 8 A, R_G = 4.7 Ω, V_{GS} = 10 V	-	10	-	ns
t_r	Rise time		-	9.5	-	ns
$t_{d(off)}$	Turn-off delay time		-	68	-	ns
t_f	Fall time		-	25.5	-	ns

Table 8: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		16	A
I_{SDM}(1)	Source-drain current (pulsed)		-		64	A
V_{SD}(2)	Forward on voltage	I_{SD} = 16 A, V_{GS} = 0 V	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 16 A, di/dt = 100 A/µs V_{DD} = 60 V	-	350		ns
Q_{rr}	Reverse recovery charge		-	4.5		µC
I_{RRM}	Reverse recovery current		-	26		A
t_{rr}	Reverse recovery time	I_{SD} = 16 A, di/dt = 100 A/µs V_{DD} = 60 V, T_j = 150 °C	-	496		ns
Q_{rr}	Reverse recovery charge		-	6.5		µC
I_{RRM}	Reverse recovery current		-	25.5		A

Notes:

(1)Pulse width limited by safe operating area.

(2)Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

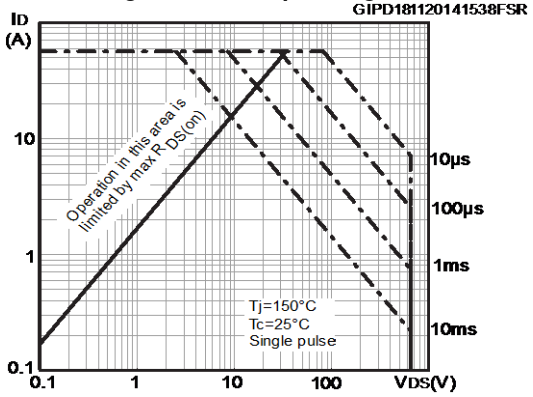


Figure 3: Thermal resistance

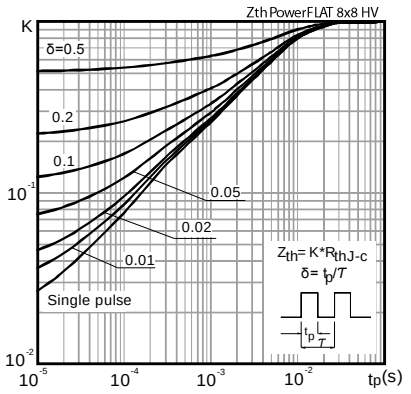


Figure 4: Output characteristics

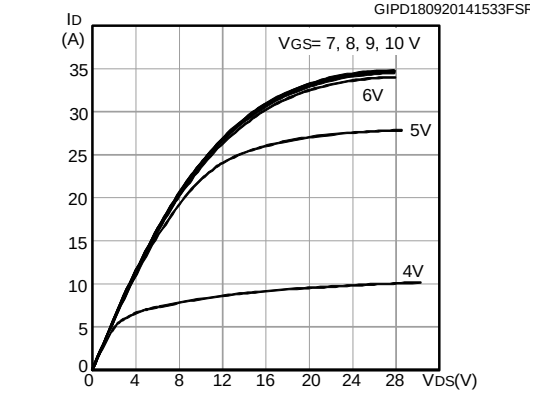


Figure 5: Transfer characteristics

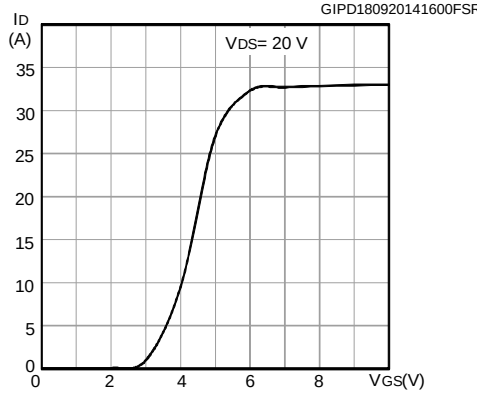


Figure 6: Gate charge vs gate-source voltage

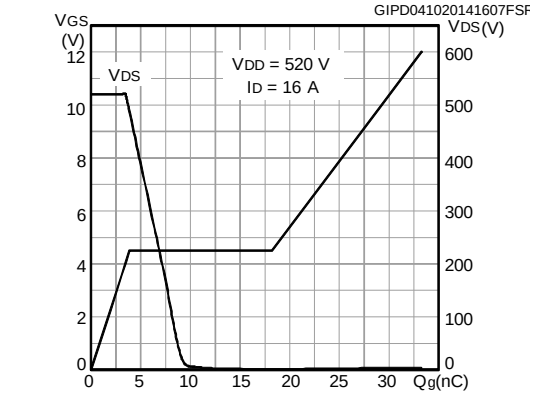


Figure 7: Static drain-source on-resistance

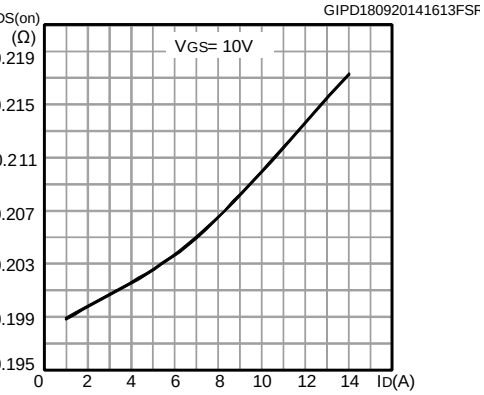


Figure 8: Capacitance variations

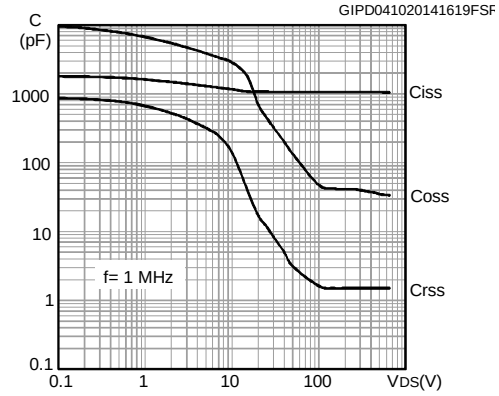


Figure 9: Normalized gate threshold voltage vs temperature

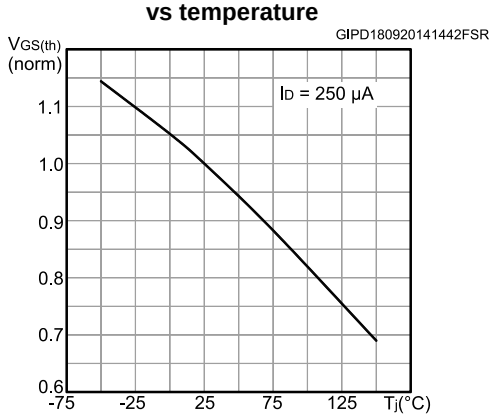


Figure 10: Normalized on-resistance

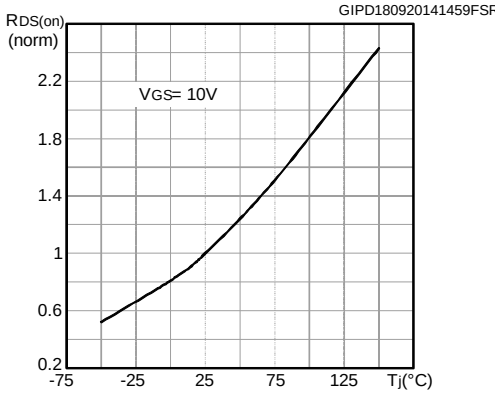


Figure 11: Normalized V(BR)DSS vs temperature

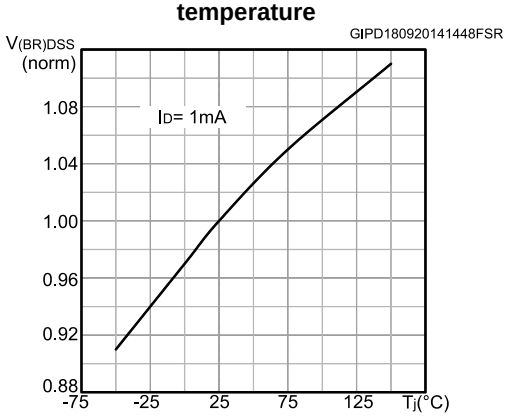


Figure 12: Source-drain diode forward characteristics

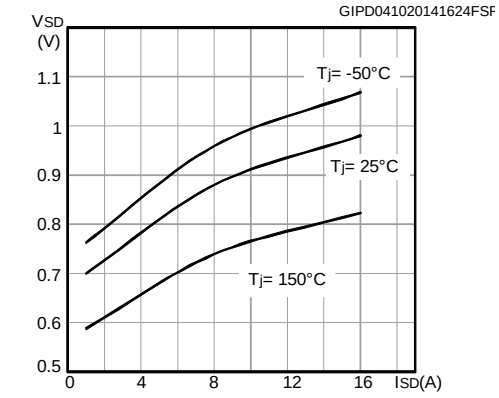
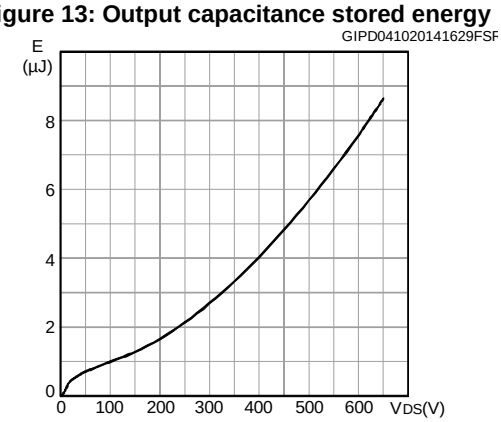


Figure 13: Output capacitance stored energy



3 Test circuits

Figure 14: Switching times test circuit for resistive load

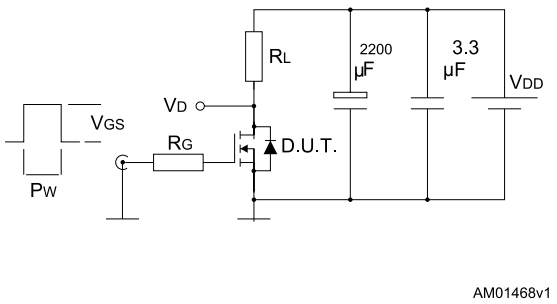


Figure 15: Gate charge test circuit

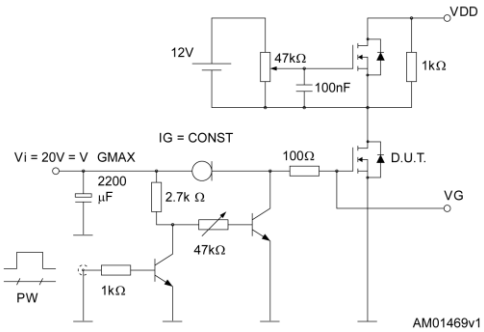


Figure 16: Test circuit for inductive load switching and diode recovery times

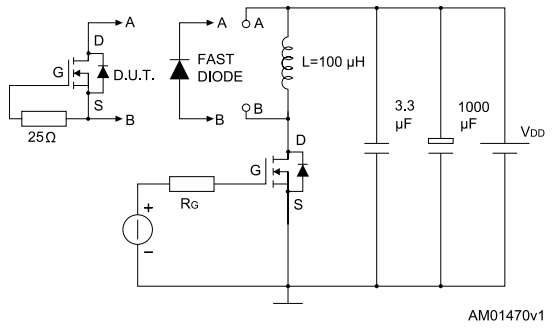


Figure 17: Unclamped inductive load test circuit

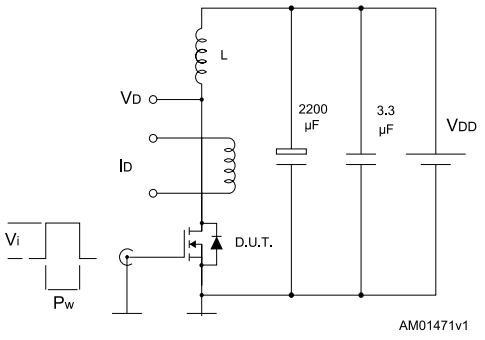


Figure 18: Unclamped inductive waveform

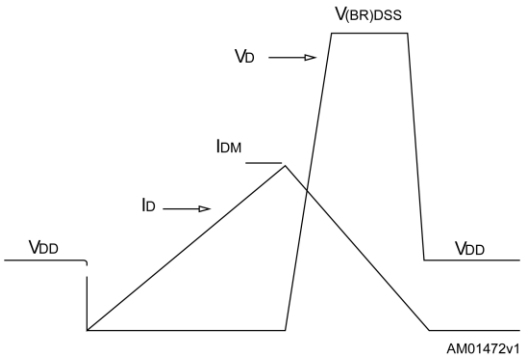
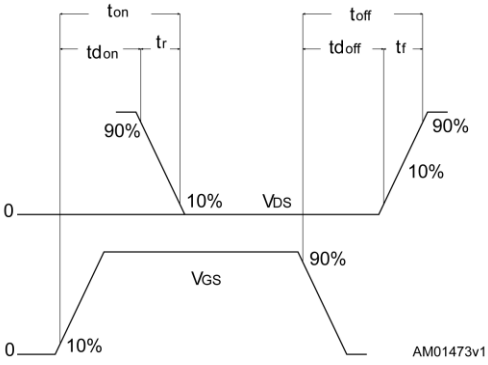


Figure 19: Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 PowerFLAT 8x8 HV package information

Figure 20: PowerFLAT™ 8x8 HV drawing

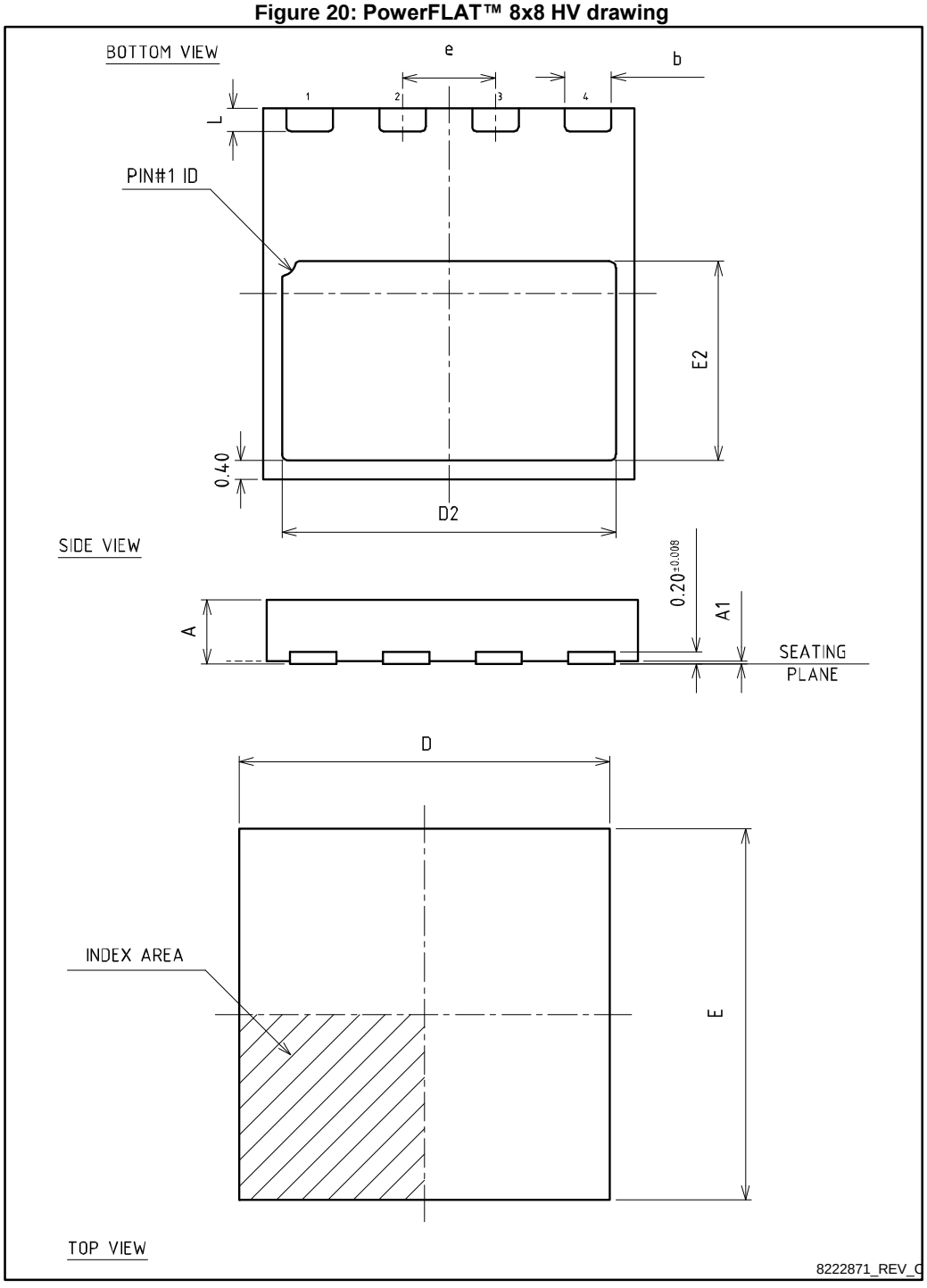
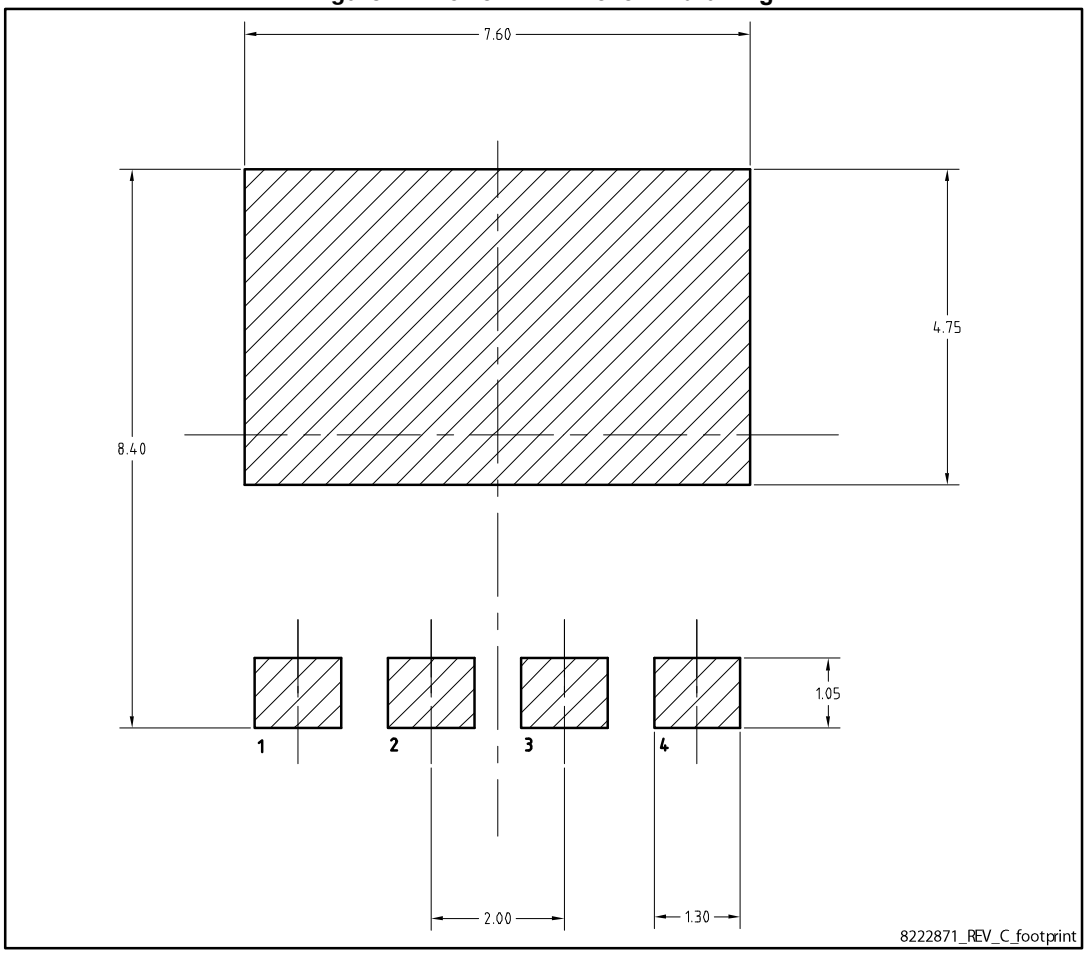


Table 9: PowerFLAT™ 8x8 HV mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
b	0.95	1.00	1.05
D		8.00	
E		8.00	
D2	7.05	7.20	7.30
E2	4.155	4.30	4.40
e		2.00	
L	0.40	0.50	0.60

Figure 21: PowerFLAT™ 8x8 HV drawing



All the dimensions are in millimeters.

5 Packaging mechanical data

Figure 22: PowerFLAT™ 8x8 HV tape

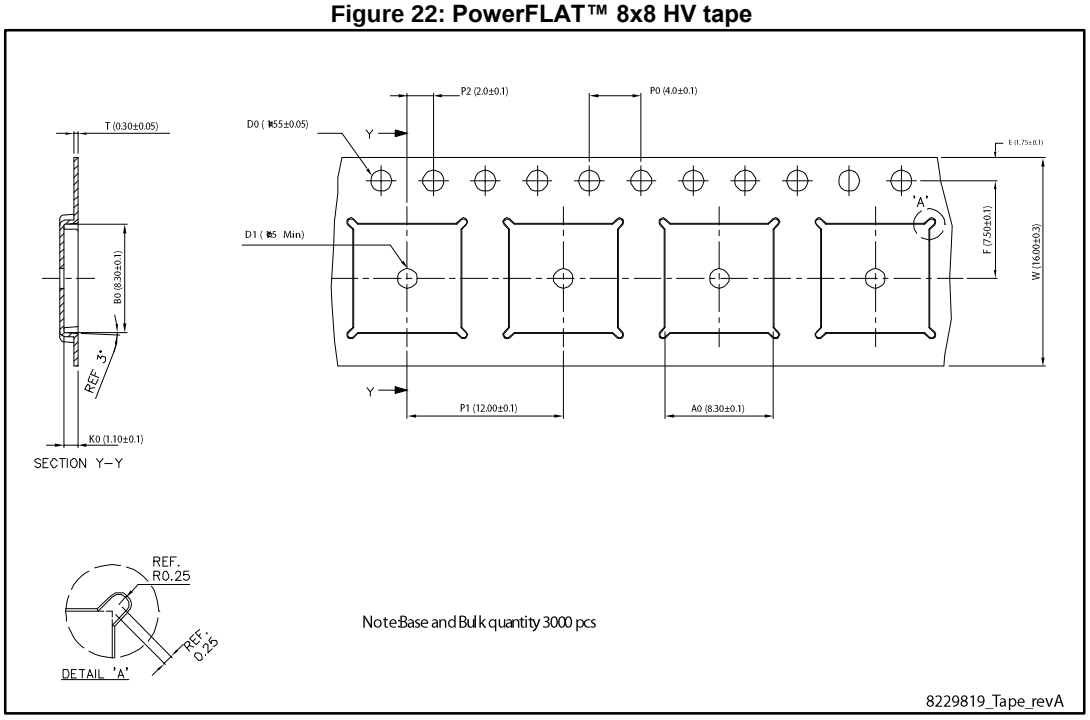


Figure 23: PowerFLAT™ 8x8 HV package orientation in carrier tape

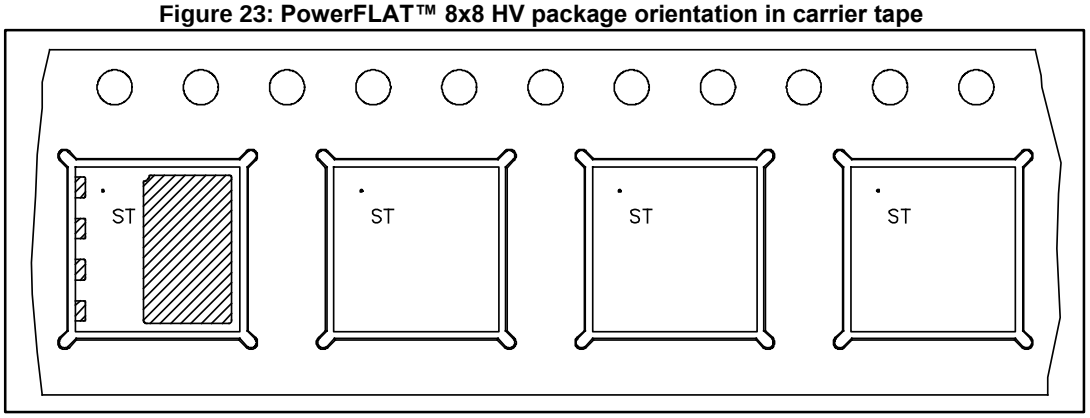
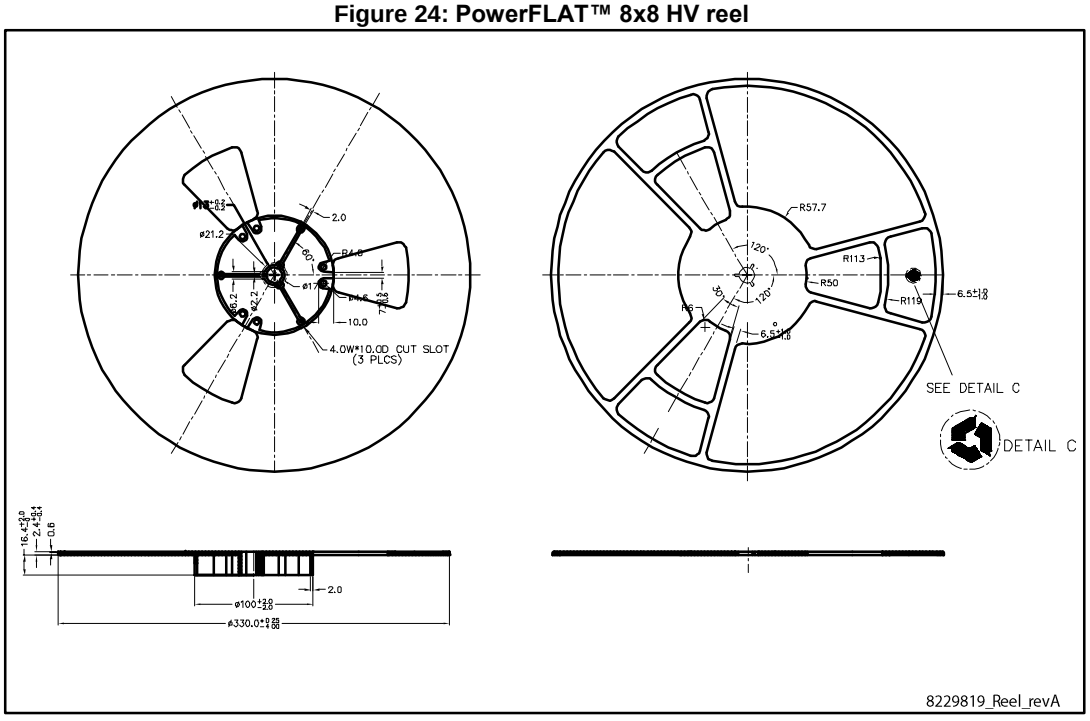


Figure 24: PowerFLAT™ 8x8 HV reel



6 Revision history

Table 10: Document revision history

Date	Revision	Changes
19-Nov-2014	1	First release.

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