

N-channel 600 V, 0.115 Ω typ., 21 A MDmesh™ DM2 Power MOSFET in a PowerFLAT™ 8x8 HV package

Datasheet - production data

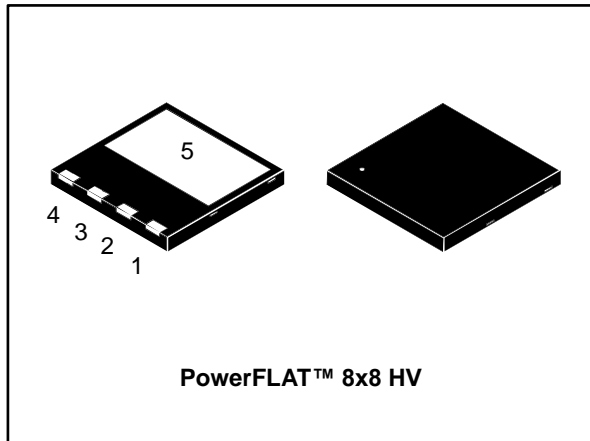
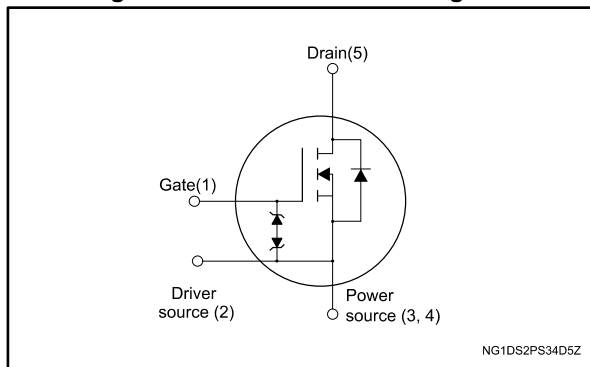


Figure 1: Internal schematic diagram



Features

| Order code | V_{DS} @ T_{Jmax} | $R_{DS(on)max}$ | I_D |
|-------------|-----------------------|-----------------|-------|
| STL33N60DM2 | 650 V | 0.140 Ω | 21 A |

- Fast-recovery body diode
- Extremely low gate charge and input capacitance
- Low on-resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected

Applications

- Switching applications

Description

This high voltage N-channel Power MOSFET is part of the MDmesh™ DM2 fast recovery diode series. It offers very low recovery charge (Q_{rr}) and time (t_{rr}) combined with low $R_{DS(on)}$, rendering it suitable for the most demanding high efficiency converters and ideal for bridge topologies and ZVS phase-shift converters.

Table 1: Device summary

| Order code | Marking | Package | Packaging |
|-------------|----------|-------------------|---------------|
| STL33N60DM2 | 33N60DM2 | PowerFLAT™ 8x8 HV | Tape and reel |

Contents

- 1 Electrical ratings 3**
- 2 Electrical characteristics 4**
 - 2.1 Electrical characteristics (curves)..... 6
- 3 Test circuits 8**
- 4 Package mechanical data 9**
 - 4.1 PowerFLAT™ 8x8 HV package mechanical data 10
 - 4.2 PowerFLAT™ 8x8 HV packing information..... 12
- 5 Revision history 14**



1 Electrical ratings

Table 2: Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|--------------------|---|-------------|------------------|
| V_{GS} | Gate-source voltage | ± 25 | V |
| $I_D^{(1)}$ | Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$ | 21 | A |
| $I_D^{(1)}$ | Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$ | 15 | A |
| $I_{DM}^{(1),(2)}$ | Drain current (pulsed) | 84 | A |
| $P_{TOT}^{(1)}$ | Total dissipation at $T_C = 25\text{ }^\circ\text{C}$ | 150 | W |
| I_{AR} | Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max) | 4.5 | A |
| E_{AS} | Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$) | 570 | mJ |
| $dv/dt^{(3)}$ | Peak diode recovery voltage slope | 50 | V/ns |
| $dv/dt^{(4)}$ | MOSFET dv/dt ruggedness | 50 | V/ns |
| T_{stg} | Storage temperature range | - 55 to 150 | $^\circ\text{C}$ |
| T_j | Operating junction temperature range | | |

Notes:

(1) The value is rated according to $R_{thj-case}$ and limited by package.

(2) Pulse width limited by safe operating area.

(3) $I_{SD} \leq 21\text{ A}$, $di/dt \leq 900\text{ A}/\mu\text{s}$, $V_{DS(peak)} < V_{(BR)DSS}$, $V_{DD} = 400\text{ V}$.

(4) $V_{DS} \leq 480\text{ V}$.

Table 3: Thermal data

| Symbol | Parameter | Value | Unit |
|---------------------|---|-------|---------------------------|
| $R_{thj-case}$ | Thermal resistance junction-case max | 0.83 | $^\circ\text{C}/\text{W}$ |
| $R_{thj-amb}^{(1)}$ | Thermal resistance junction-ambient max | 45 | $^\circ\text{C}/\text{W}$ |

Notes:

(1) When mounted on FR-4 board of inch^2 , 2oz Cu.

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified)

Table 4: On /off states

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------|------------------------------------|--|------|-------|----------|---------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $V_{GS} = 0, I_D = 1\text{ mA}$ | 600 | | | V |
| I_{DSS} | Zero gate voltage drain current | $V_{GS} = 0, V_{DS} = 600\text{ V}$ | | | 1 | μA |
| | | $V_{GS} = 0, V_{DS} = 600\text{ V}, T_C = 125\text{ °C}^{(1)}$ | | | 100 | μA |
| I_{GSS} | Gate-body leakage current | $V_{DS} = 0, V_{GS} = \pm 25\text{ V}$ | | | ± 10 | μA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$ | 3 | 4 | 5 | V |
| $R_{DS(on)}$ | Static drain-source on- resistance | $V_{GS} = 10\text{ V}, I_D = 10.5\text{ A}$ | | 0.115 | 0.140 | Ω |

Notes:

⁽¹⁾Defined by design, not subject to production test.

Table 5: Dynamic

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|----------------------------|-------------------------------|--|------|------|------|----------|
| C_{iss} | Input capacitance | $V_{DS} = 100\text{ V}, f = 1\text{ MHz}, V_{GS} = 0$ | - | 1870 | - | pF |
| C_{oss} | Output capacitance | | - | 87 | - | pF |
| C_{riss} | Reverse transfer capacitance | | - | 2 | - | pF |
| $C_{oss\text{ eq.}}^{(1)}$ | Equivalent output capacitance | $V_{DS} = 0\text{ to }480\text{ V}, V_{GS} = 0$ | - | 157 | - | pF |
| R_G | Intrinsic gate resistance | $f = 1\text{ MHz}, I_D = 0\text{ A}$ | - | 4.5 | - | Ω |
| Q_g | Total gate charge | $V_{DD} = 480\text{ V}, I_D = 21\text{ A}$ $V_{GS} = 10\text{ V}$ (see Figure 15: "Gate charge test circuit") | - | 43 | - | nC |
| Q_{gs} | Gate-source charge | | - | 9.8 | - | nC |
| Q_{gd} | Gate-drain charge | | - | 21.4 | - | nC |

Notes:

⁽¹⁾ $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 6: Switching times

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|--------------|---------------------|--|------|------|------|------|
| $t_{d(on)}$ | Turn-on delay time | $V_{DD} = 300\text{ V}$, $I_D = 10.5\text{ A}$ $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 14: "Switching times test circuit for resistive load") | - | 17 | - | ns |
| t_r | Rise time | | - | 8 | - | ns |
| $t_{d(off)}$ | Turn-off delay time | | - | 62 | - | ns |
| t_f | Fall time | | - | 9 | - | ns |

Table 7: Source drain diode

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|--------------------|-------------------------------|--|------|------|------|---------------|
| $I_{SD}^{(1)}$ | Source-drain current | | - | | 21 | A |
| $I_{SDM}^{(1)(2)}$ | Source-drain current (pulsed) | | - | | 84 | A |
| $V_{SD}^{(3)}$ | Forward on voltage | $I_{SD} = 21\text{ A}$, $V_{GS} = 0$ | - | | 1.6 | V |
| t_{rr} | Reverse recovery time | $I_{SD} = 21\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 100\text{ V}$ (see Figure 16: "Test circuit for inductive load switching and diode recovery times") | - | 120 | | ns |
| Q_{rr} | Reverse recovery charge | | - | 0.53 | | μC |
| I_{RRM} | Reverse recovery current | | - | 8.8 | | A |
| t_{rr} | Reverse recovery time | $I_{SD} = 21\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 100\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 16: "Test circuit for inductive load switching and diode recovery times") | - | 316 | | ns |
| Q_{rr} | Reverse recovery charge | | - | 2.85 | | μC |
| I_{RRM} | Reverse recovery current | | - | 18 | | A |

Notes:

- (1) The value is rated according to $R_{thj-case}$ and limited by package.
(2) Pulse width limited by safe operating area
(3) Pulsed: pulse duration = 300 μs , duty cycle 1.5%

Table 8: Gate-source Zener diode

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------|-------------------------------|--|----------|------|------|------|
| $V_{(BR)GSO}$ | Gate-source breakdown voltage | $I_{GS} = \pm 250\ \mu\text{A}$, $I_D = 0\text{ A}$ | ± 30 | - | - | V |

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

2.2 Electrical characteristics (curves)

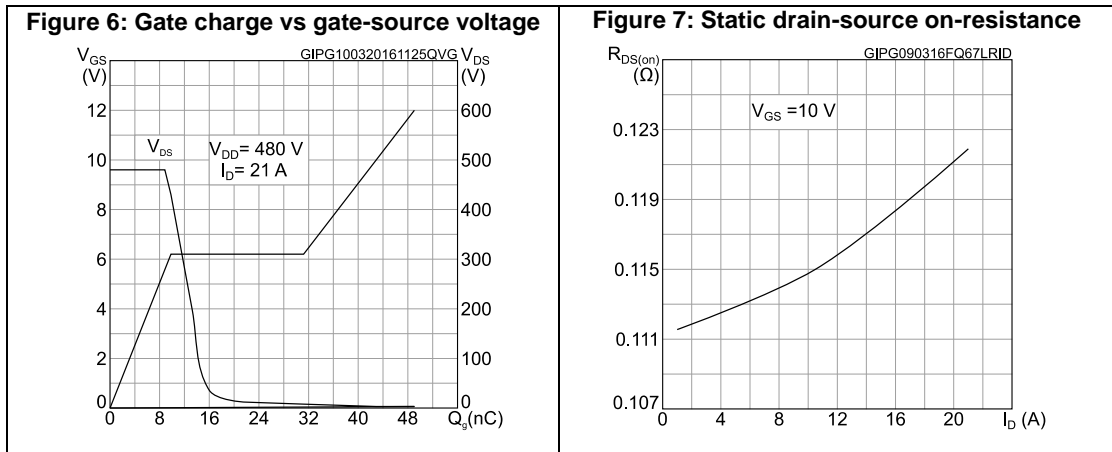
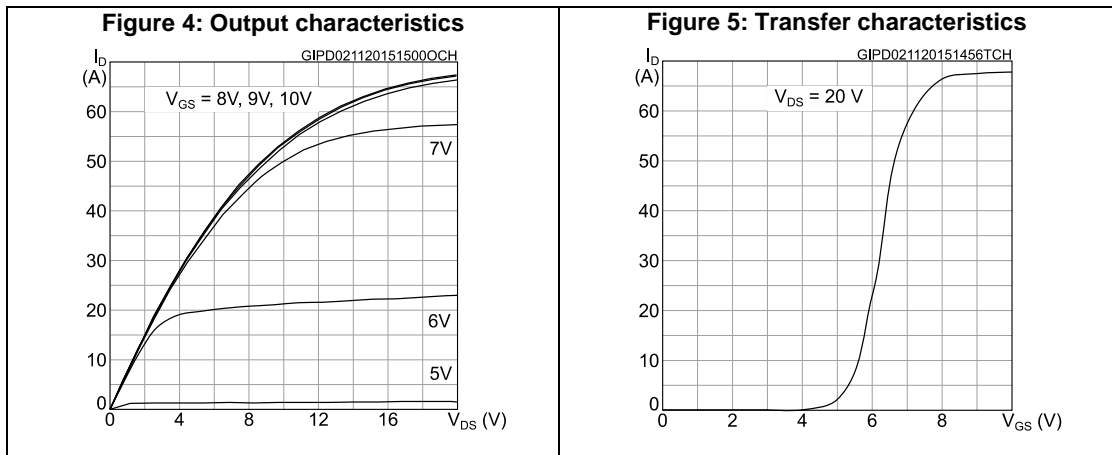
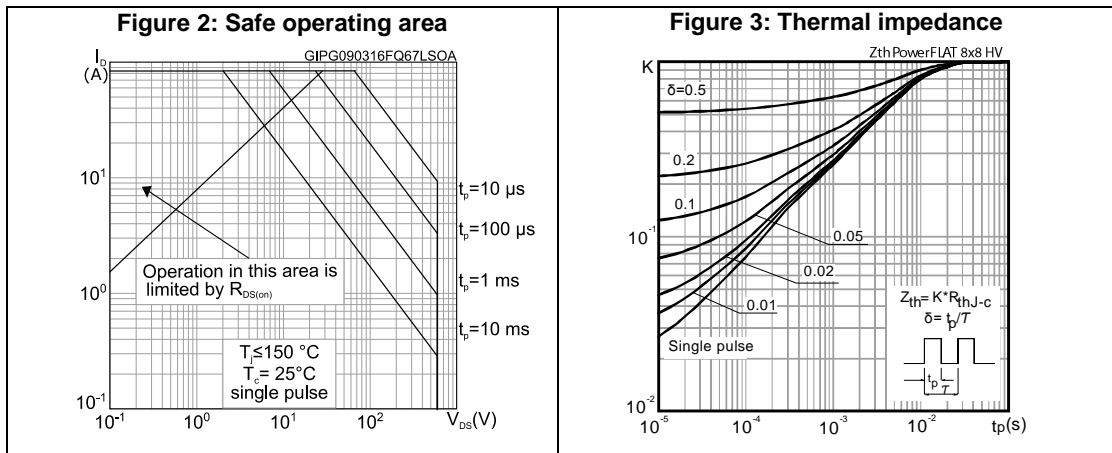


Figure 8: Capacitance variations

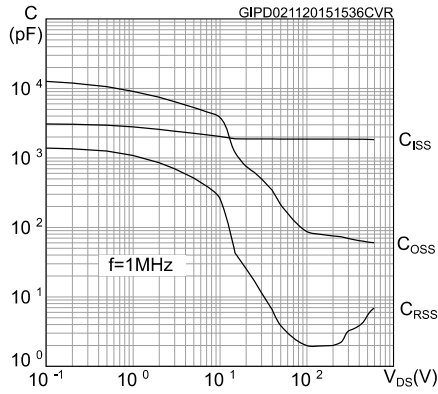


Figure 9: Normalized gate threshold voltage vs temperature

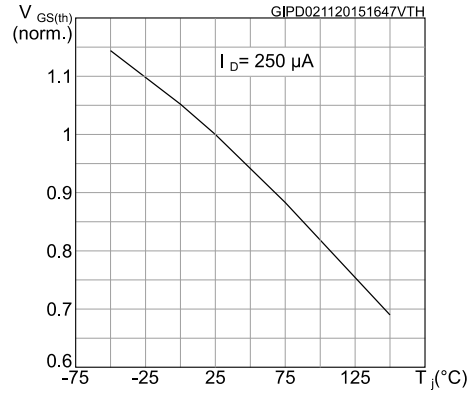


Figure 10: Normalized on-resistance vs temperature

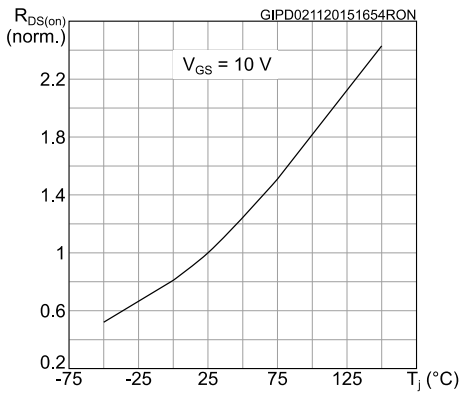


Figure 11: Normalized $V_{(BR)DSS}$ vs temperature

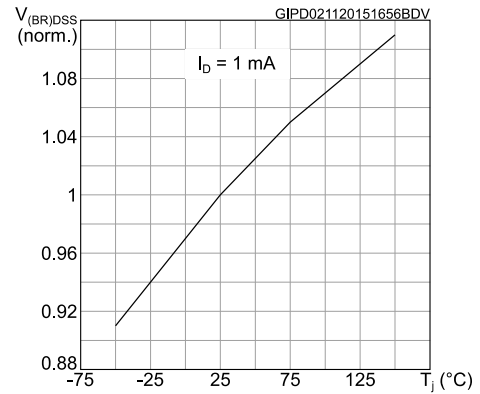


Figure 12: Output capacitance stored energy

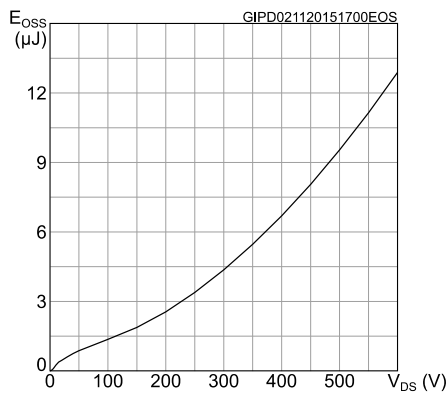
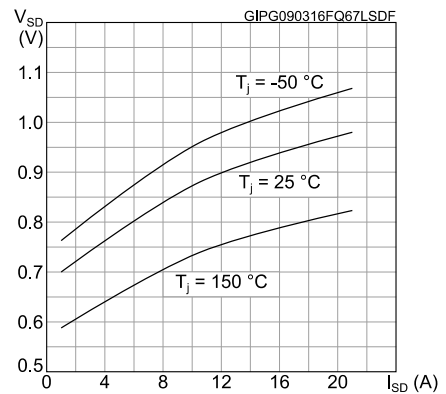
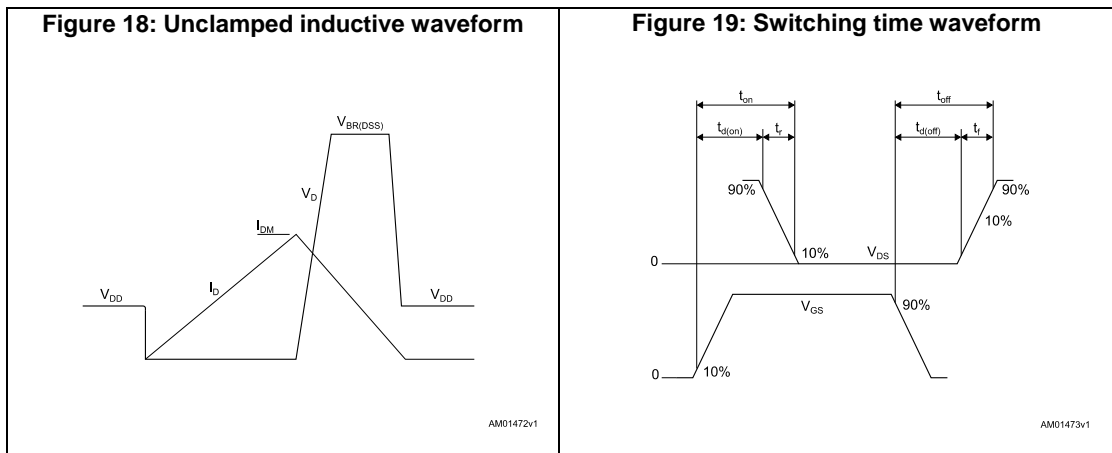
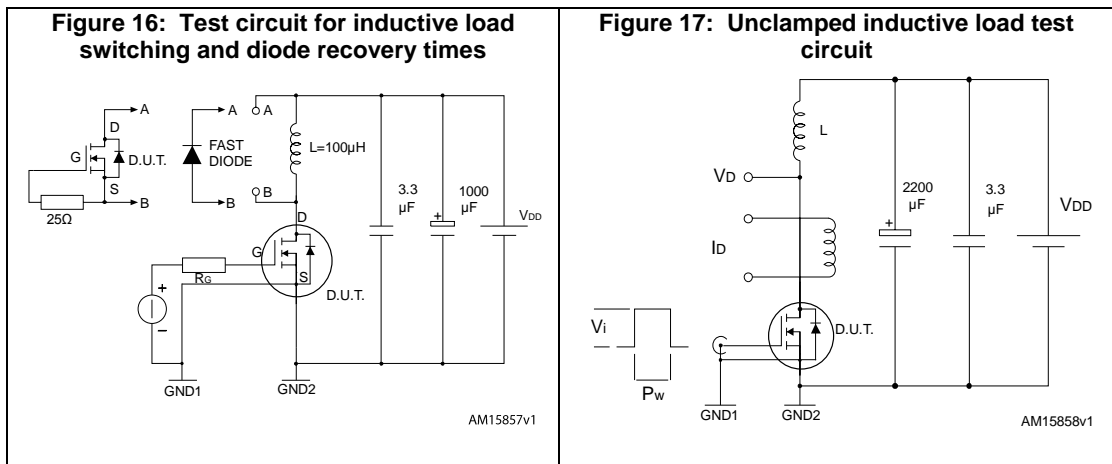
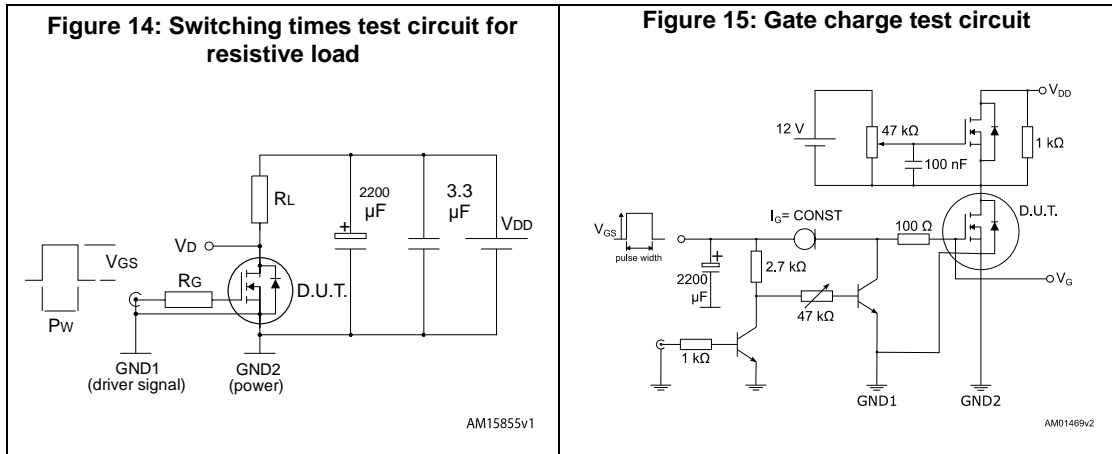


Figure 13: Source- drain diode forward characteristics



3 Test circuits

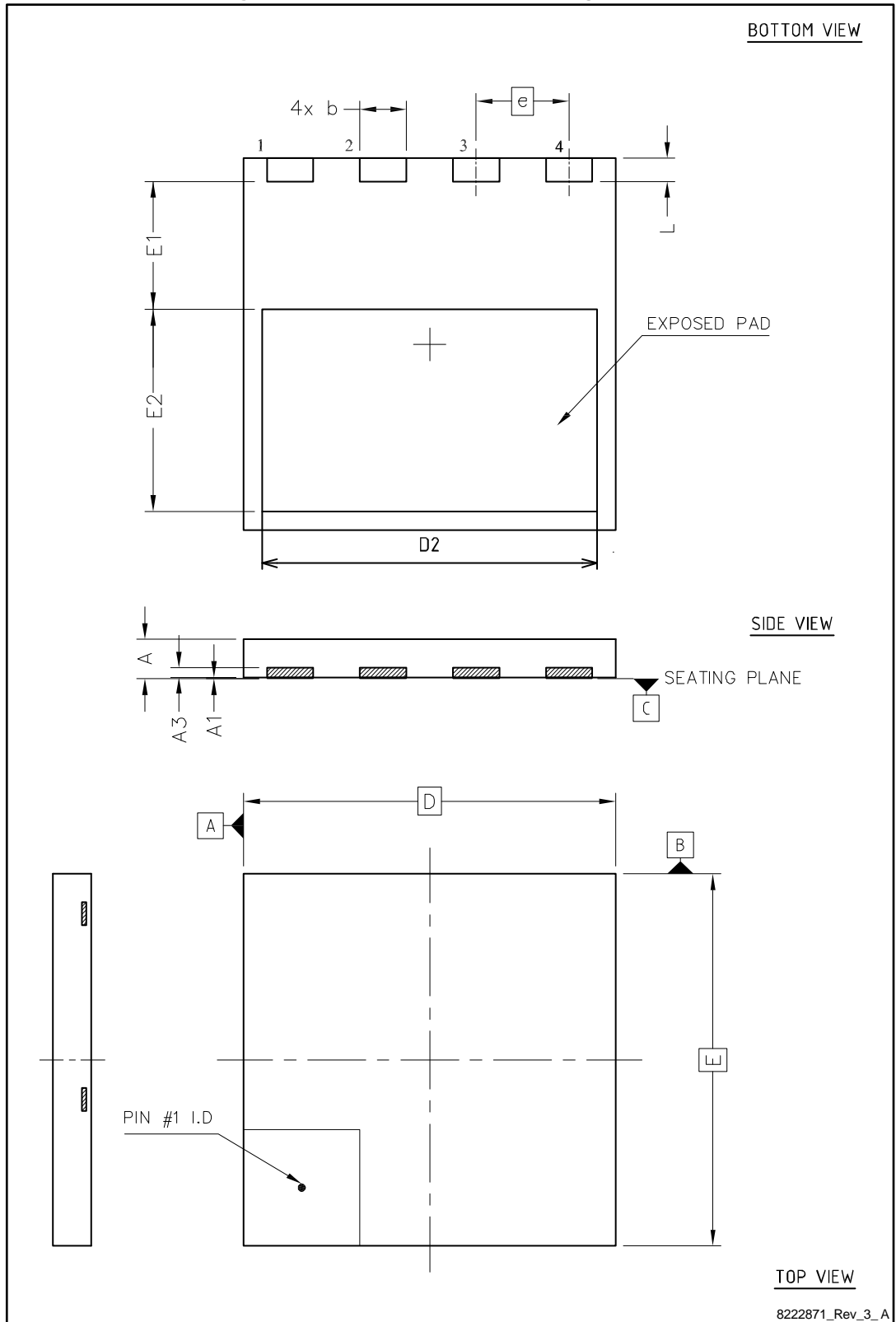


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

4.1 PowerFLAT™ 8x8 HV package mechanical data

Figure 20: PowerFLAT™ 8x8 HV package outline

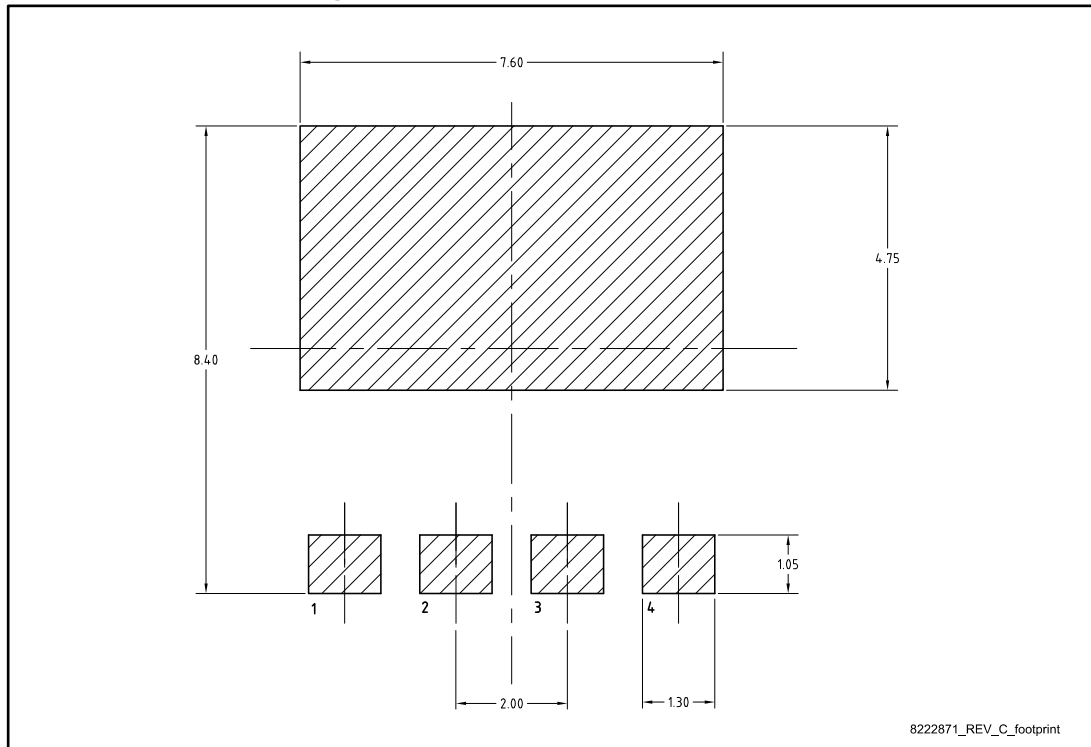


8222871_Rev_3_A

Table 9: PowerFLAT™ 8x8 HV mechanical data

| Dim. | mm | | |
|------|------|------|------|
| | Min. | Typ. | Max. |
| A | 0.75 | 0.85 | 0.95 |
| A1 | 0.00 | | 0.05 |
| A3 | 0.10 | 0.20 | 0.30 |
| b | 0.90 | 1.00 | 1.10 |
| D | 7.90 | 8.00 | 8.10 |
| E | 7.90 | 8.00 | 8.10 |
| D2 | 7.10 | 7.20 | 7.30 |
| E1 | 2.65 | 2.75 | 2.85 |
| E2 | 4.25 | 4.35 | 4.45 |
| e | | 2.00 | |
| L | 0.40 | 0.50 | 0.60 |

Figure 21: PowerFLAT™ 8x8 HV footprint



All dimensions are in millimeters.

4.2 PowerFLAT™ 8x8 HV packing information

Figure 22: PowerFLAT™ 8x8 HV tape

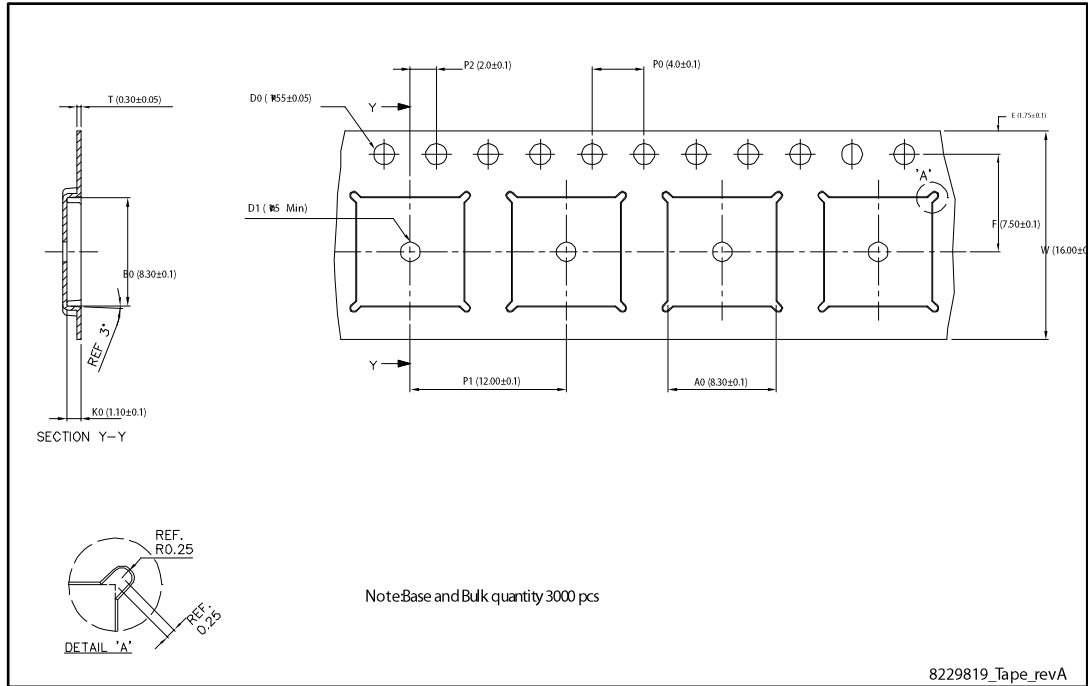


Figure 23: PowerFLAT™ 8x8 HV package orientation in carrier tape

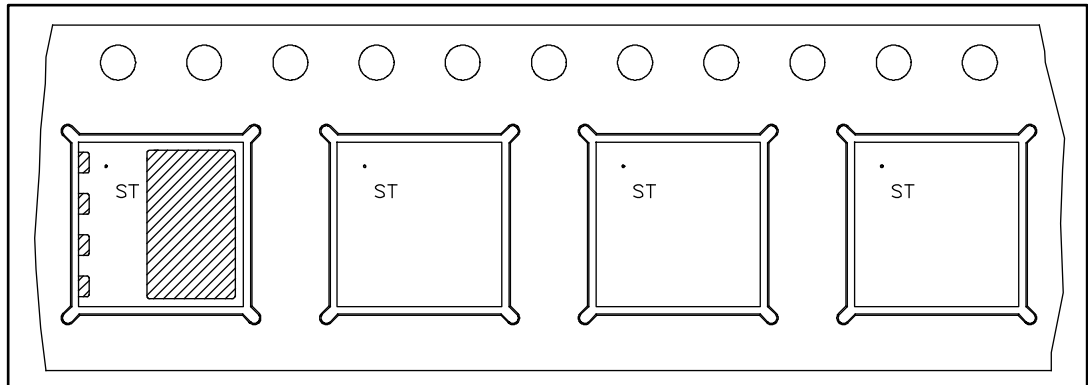
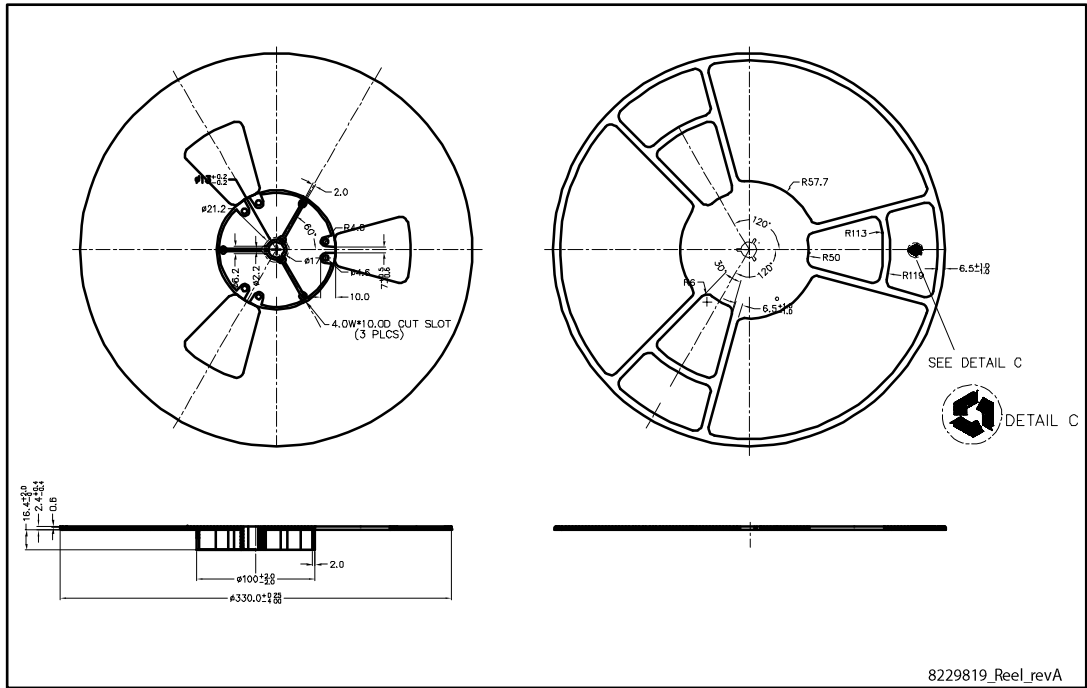


Figure 24: PowerFLAT™ 8x8 HV reel



5 Revision history

Table 10: Document revision history

| Date | Revision | Changes |
|-------------|----------|---|
| 08-Aug-2014 | 1 | First release. |
| 09-Mar-2016 | 2 | Updated title and internal schematic in cover page. Document status promoted from preliminary data to production data. Modified: <i>Table 2: "Absolute maximum ratings"</i> , <i>Table 4: "On /off states"</i> , <i>Table 5: "Dynamic"</i> , <i>Table 6: "Switching times"</i> and <i>Table 7: "Source drain diode"</i> Added: <i>Section 4.1: "Electrical characteristics (curves)"</i> Updated: <i>Section 6.1: "PowerFLAT™ 8x8 HV package mechanical data"</i> Minor text changes |

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