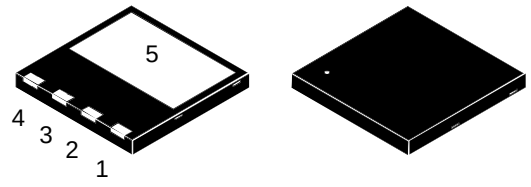
STL33N65M2

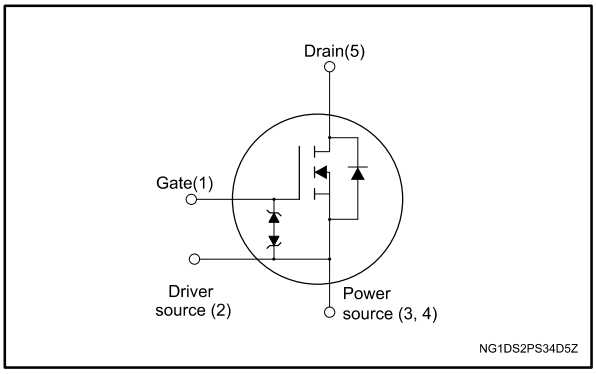
N-channel 650 V, 0.124 Ω typ., 20 A MDmesh™ M2 Power MOSFET in a PowerFLAT™ 8x8 HV package

Datasheet - production data



PowerFLAT™ 8x8 HV

Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$max	I_D
STL33N65M2	650 V	0.154 Ω	20 A

- Extremely low gate charge
- Excellent output capacitance (C_{OSS}) profile
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using MDmesh™ M2 technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance and optimized switching characteristics, rendering it suitable for the most demanding high efficiency converters.

Table 1: Device summary

Order code	Marking	Package	Packing
STL33N65M2	33N65M2	PowerFLAT™ 8x8 HV	Tape and reel

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at T_C = 25 °C	20	A
I_D	Drain current (continuous) at T_C = 100 °C	12.6	A
I_{DM} (1)	Drain current (pulsed)	80	A
P_{TOT}	Total dissipation at T_C = 25 °C	150	W
dv/dt (2)	Peak diode recovery voltage slope	15	V/ns
dv/dt (3)	MOSFET dv/dt ruggedness	50	V/ns
T_{stg}	Storage temperature range	- 55 to 150	°C
T_j	Operating junction temperature range		°C

Notes:

(1)Pulse width limited by safe operating area.

(2)I_{SD} ≤ 20 A, di/dt ≤ 400 A/µs, $V_{DS(peak)} < V_{(BR)DSS}$, V_{DD} = 400 V.

(3)V_{DS} ≤ 520 V.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	0.83	°C/W
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb max	45	°C/W

Notes:

(1)When mounted on FR-4 board of inch², 2oz Cu.

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or notrepetitive (pulse width limited by T_{jmax})	2.2	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	600	mJ

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 5: On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	650			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 650 V			1	µA
		V_{GS} = 0 V, V_{DS} = 650 V, T_C=125 °C (1)			100	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ± 25 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on- resistance	V_{GS} = 10 V, I_D = 10 A		0.124	0.154	Ω

Notes:

(1)Defined by design, not subject to production test.

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0	-	1790	-	pF
C_{oss}	Output capacitance		-	75	-	pF
C_{rss}	Reverse transfer capacitance		-	2	-	pF
$C_{oss\ eq.}$ (1)	Equivalent output capacitance	V_{DS} = 0 to 520 V, V_{GS} = 0	-	380	-	pF
Q_g	Total gate charge	V_{DD} = 520 V, I_D = 24 A V_{GS} = 10 V (see *Figure 15: "Gate charge test circuit"*)	-	41.5	-	nC
Q_{gs}	Gate-source charge		-	6.8	-	nC
Q_{gd}	Gate-drain charge		-	18	-	nC

Notes:

(1)Coss eq. is defined as a constant equivalent capacitance giving the same charging time as Coss when VDS increases from 0 to 80% V_{DSS}.

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 325 V, I_D = 12 A R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 14: "Switching times test circuit for resistive load"* and *Figure 19: "Switching time waveform"*)	-	13.5	-	ns
t_r	Voltage rise time		-	11.5	-	ns
$t_{d(off)}$	Turn-off delay time		-	72.5	-	ns
t_f	Current fall time		-	11.5	-	ns

Table 8: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		20	A
I_{SDM} (1)	Source-drain current (pulsed)		-		80	A
V_{SD} (2)	Forward on voltage	I_{SD} = 24 A, V_{GS} = 0 V	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 24 A, di/dt = 100 A/µs V_{DD} = 60 V (see *Figure 16: " Test circuit for inductive load switching and diode recovery times"*)	-	426		ns
Q_{rr}	Reverse recovery charge		-	7		µC
I_{RRM}	Reverse recovery current		-	33.5		A
t_{rr}	Reverse recovery time	I_{SD} = 24 A, di/dt = 100 A/µs V_{DD} = 60 V, T_j = 150 °C (see *Figure 16: " Test circuit for inductive load switching and diode recovery times"*)	-	544		ns
Q_{rr}	Reverse recovery charge		-	10		µC
I_{RRM}	Reverse recovery current		-	36.5		A

Notes:

(1)Pulse width limited by safe operating area.

(2)Pulsed: pulse duration = 300 µs, duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

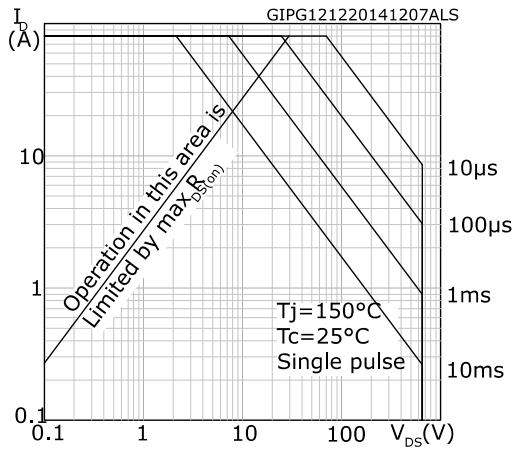


Figure 3: Thermal impedance

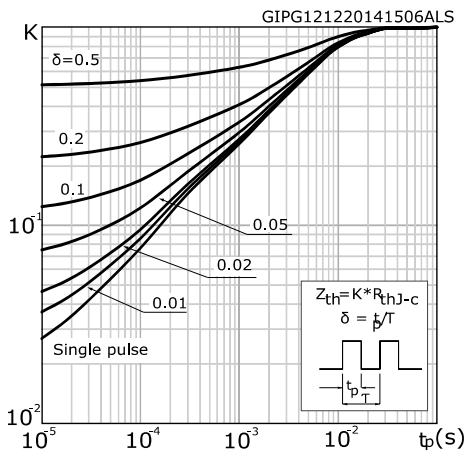


Figure 4: Output characteristics

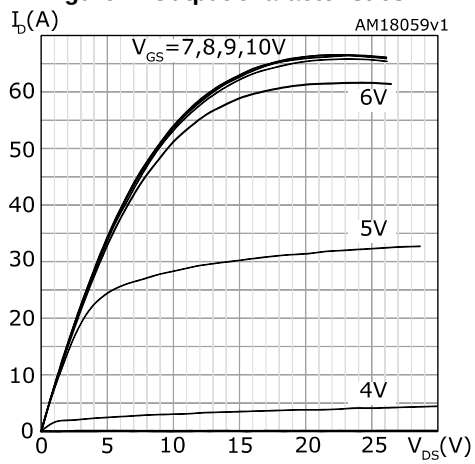


Figure 5: Transfer characteristics

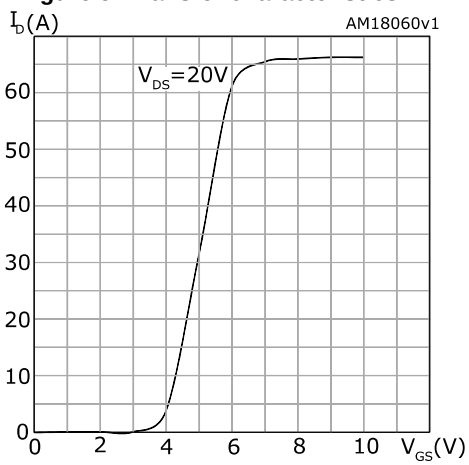


Figure 6: Gate charge vs gate-source voltage

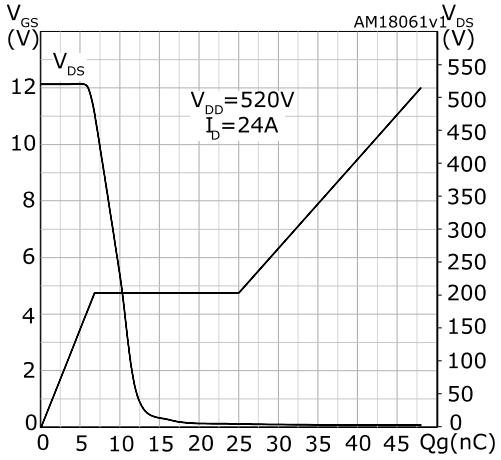


Figure 7: Static drain-source on-resistance

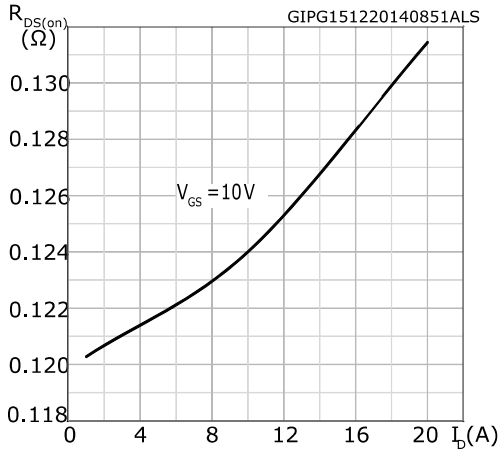


Figure 8: Capacitance variations

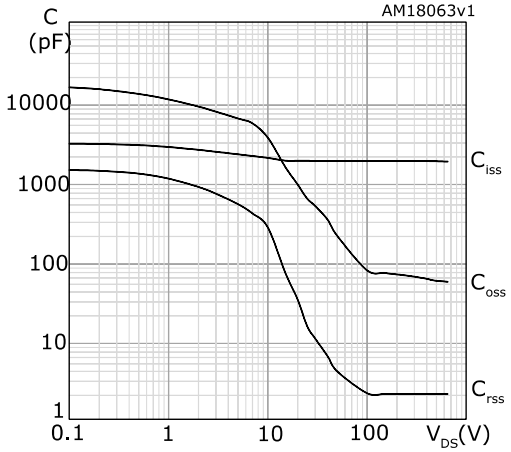


Figure 9: Output capacitance stored energy

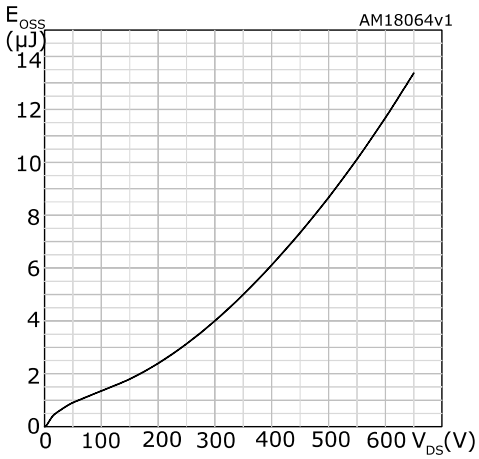


Figure 10: Normalized gate threshold voltage vs temperature

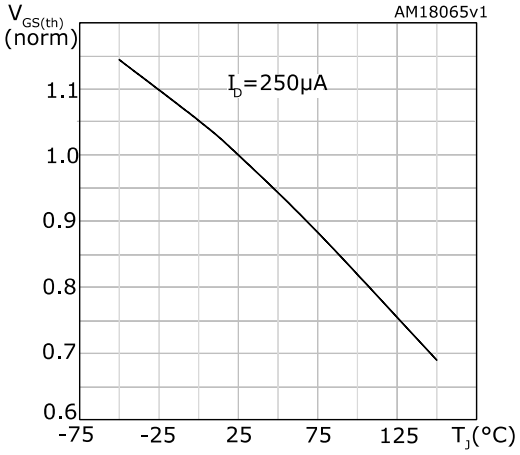


Figure 11: Normalized on-resistance vs temperature

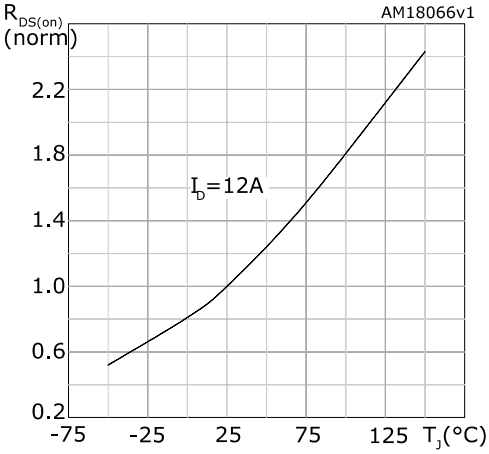


Figure 12: Source-drain diode forward characteristics

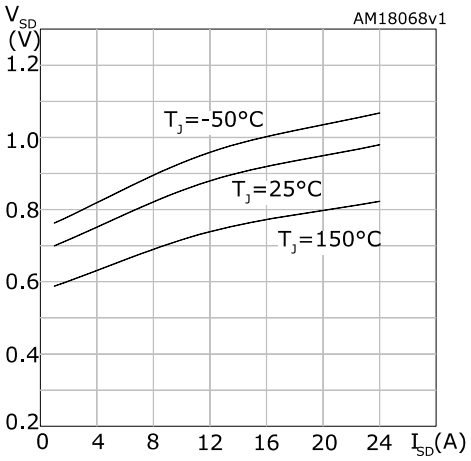
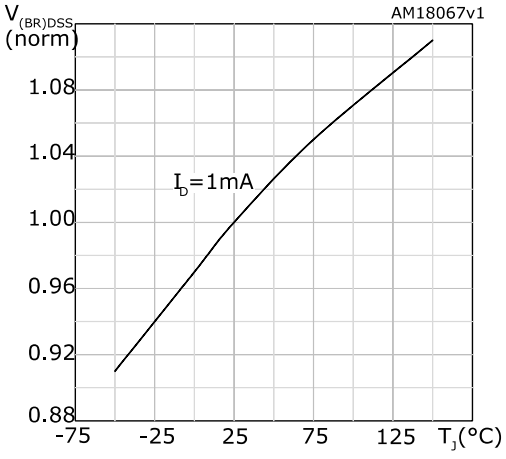


Figure 13: Normalized $V_{(BR)DSS}$ vs temperature



3 Test circuits

Figure 14: Switching times test circuit for resistive load

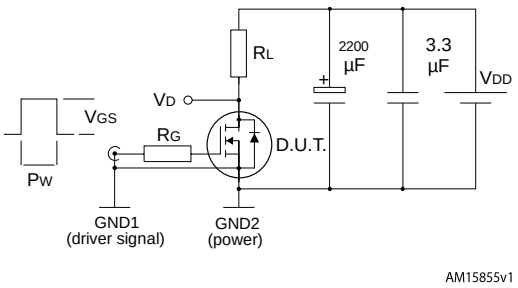


Figure 15: Gate charge test circuit

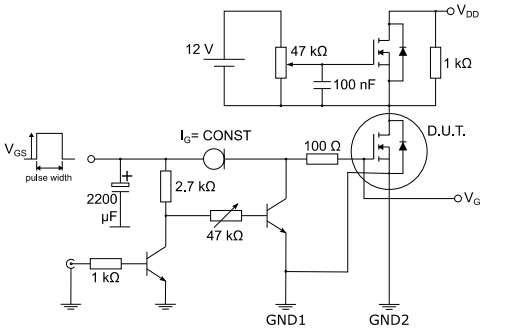


Figure 16: Test circuit for inductive load switching and diode recovery times

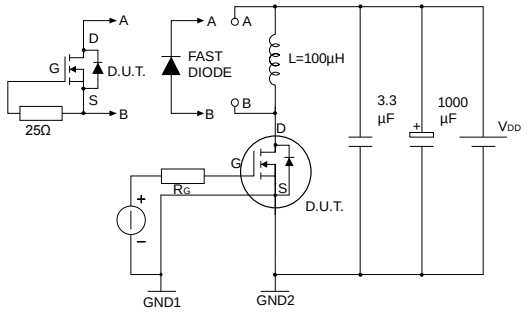


Figure 17: Unclamped inductive load test circuit

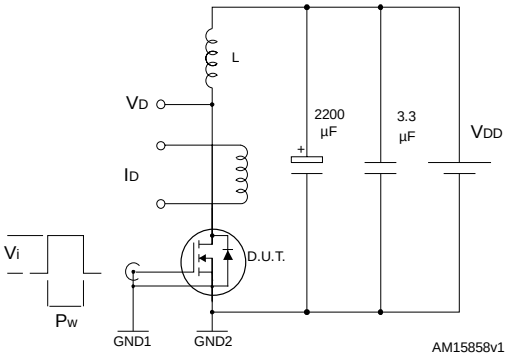


Figure 18: Unclamped inductive waveform

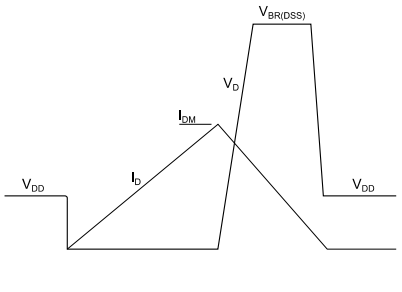
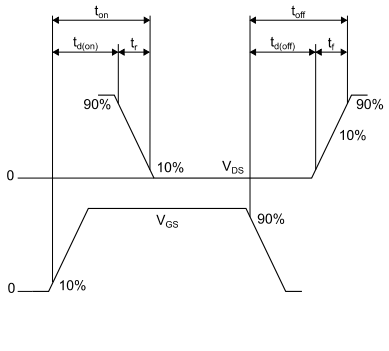


Figure 19: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 PowerFLAT™ 8x8 HV package information

Figure 20: PowerFLAT™ 8x8 HV package outline

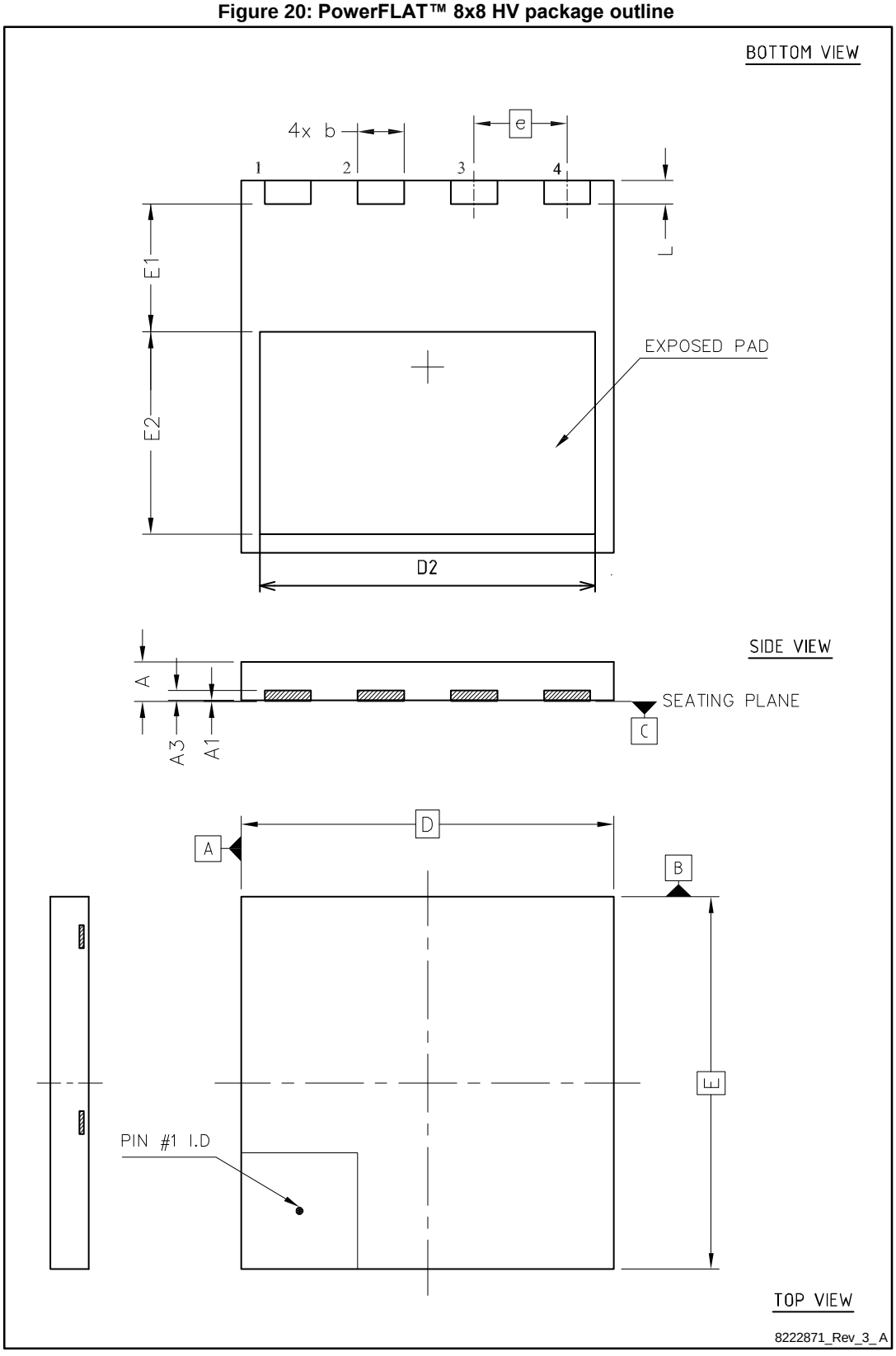
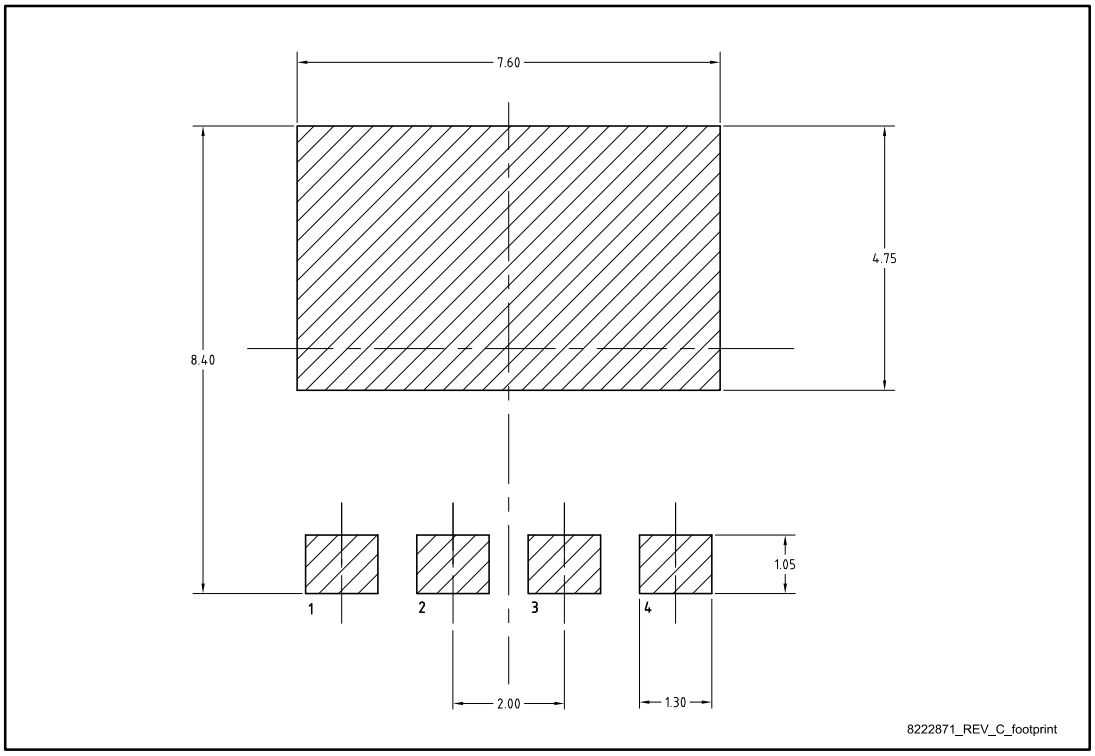


Table 9: PowerFLAT™ 8x8 HV mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.75	0.85	0.95
A1	0.00		0.05
A3	0.10	0.20	0.30
b	0.90	1.00	1.10
D	7.90	8.00	8.10
E	7.90	8.00	8.10
D2	7.10	7.20	7.30
E1	2.65	2.75	2.85
E2	4.25	4.35	4.45
e		2.00	
L	0.40	0.50	0.60

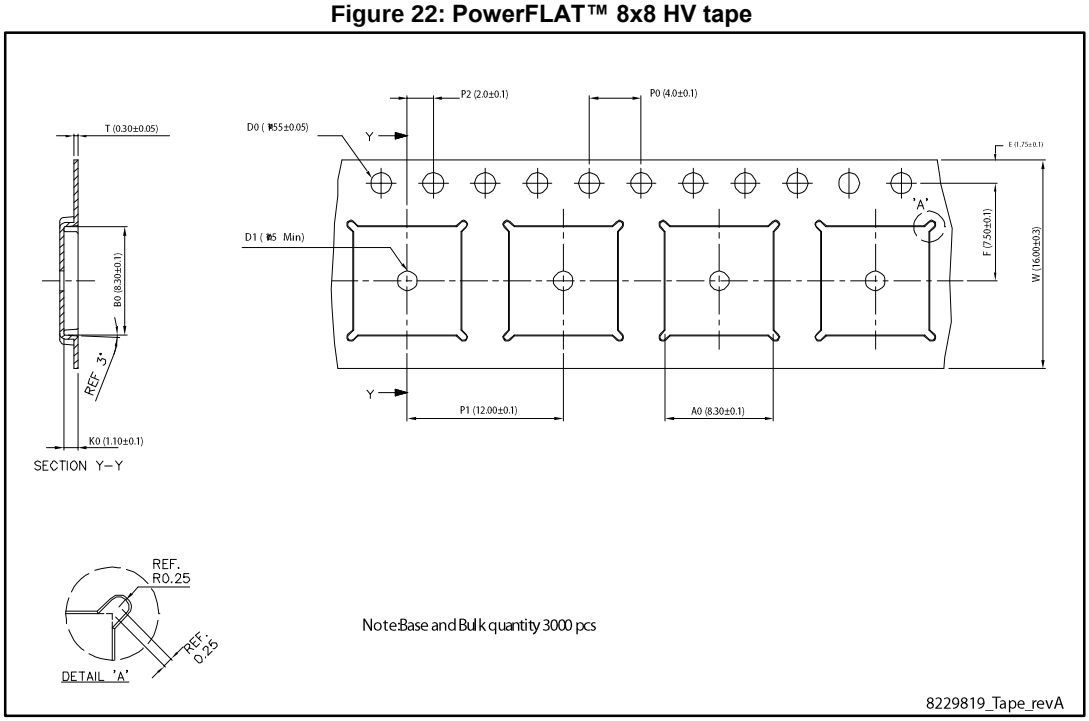
Figure 21: PowerFLAT™ 8x8 HV footprint



All dimensions are in millimeters.

4.2 PowerFLAT™ 8x8 HV packing information

Figure 22: PowerFLAT™ 8x8 HV tape



All dimensions are in millimeters.

Figure 23: PowerFLAT™ 8x8 HV package orientation in carrier tape

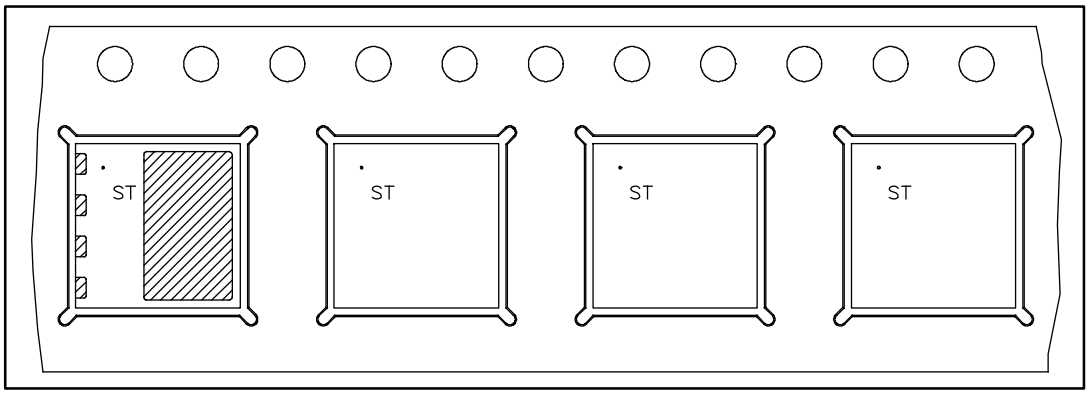
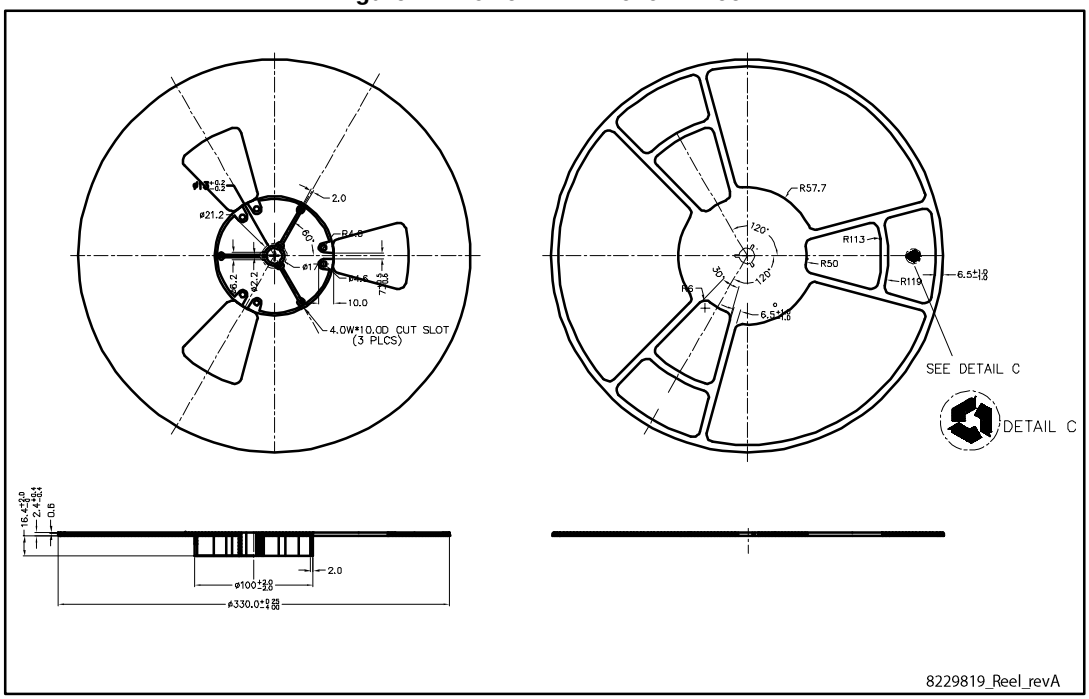


Figure 24: PowerFLAT™ 8x8 HV reel



All dimensions are in millimeters.

5 Revision history

Table 10: Document revision history

Date	Revision	Changes
26-Jun-2013	1	First release.
23-Jul-2014	2	Text edits throughout document. On cover page, updated title, features and description. Updated Table 2: Absolute maximum ratings. Updated Table 3: Thermal data. Added Table 4: Avalanche characteristics. Updated Table 5: On /off states. Updated Table 6: Dynamic. Updated Table 7: Switching times. Updated Table 8: Source drain diode.
13-Apr-2016	3	Updated cover image and *Figure 1: "Internal schematic diagram"*. Updated *Section 3: "Test circuits"*. Added footnote in *Table 5: "On /off states"*. Removed footnote in *Table 8: "Source drain diode"*. Updated *Section 4: "Package information"*. Minor text changes.

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