STL34N65M5



N-channel 650 V, 0.099 Ω typ., 22.5 A MDmesh™ V Power MOSFET in PowerFLAT™ 8x8 HV package

Datasheet - production data

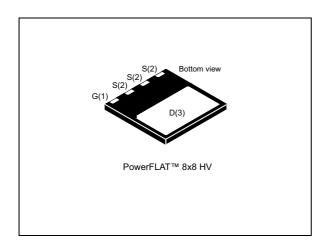
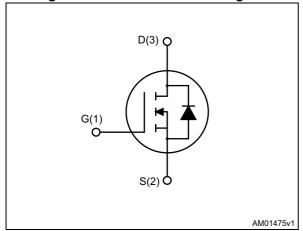


Figure 1. Internal schematic diagram



Features

Order code	V _{DS} @ T _{Jmax}	R _{DS(on)} max	I _D
STL34N65M5	710 V	$0.120~\Omega$	22.5 A ⁽¹⁾

- The value is rated according to R_{thj-case} and limited by package.
- 100% avalanche tested
- · Low input capacitance and gate charge
- · Low gate input resistance

Applications

· Switching applications

Description

This device is an N-channel MDmesh™ V Power MOSFET based on an innovative proprietary vertical process technology, which is combined with STMicroelectronics' well-known PowerMESH™ horizontal layout structure. The resulting product has extremely low onresistance, which is unmatched among siliconbased Power MOSFETs, making it especially suitable for applications which require superior power density and outstanding efficiency.

Table 1. Device summary

Order code	Marking	Package	Packaging
STL34N65M5	34N65M5	PowerFLAT™ 8x8 HV	Tape and reel

Contents STL34N65M5

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STL34N65M5 Electrical ratings

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source voltage	650	V
V _{GS}	Gate-source voltage	± 25	٧
I _D ⁽¹⁾	Drain current (continuous) at T _C = 25 °C	22.5	Α
I _D ⁽¹⁾	Drain current (continuous) at T _C = 100 °C	15	Α
I _{DM} (1),(2)	Drain current (pulsed)	90	Α
I _D (3)	Drain current (continuous) at T _{amb} = 25 °C	3.2	Α
I _D (3)	Drain current (continuous) at T _{amb} = 100 °C	2	Α
P _{TOT} (3)	Total dissipation at T _{amb} = 25 °C	2.8	W
P _{TOT} (1)	Total dissipation at T _C = 25 °C	150	W
I _{AR}	Avalanche current, repetitive or not- repetitive (pulse width limited by T_j max)	6	Α
E _{AS}	Single pulse avalanche energy (starting $T_j = 25$ °C, $I_D = I_{AR}$, $V_{DD} = 50$ V)	510	mJ
dv/dt (4)	Peak diode recovery voltage slope	15	V/ns
T _{stg}	Storage temperature	- 55 to 150	°C
T _j	Max. operating junction temperature	150	°C

- 1. The value is rated according to $R_{\mbox{\scriptsize thj-case}}$ and limited by package.
- 2. Pulse width limited by safe operating area.
- 3. When mounted on FR-4 board of inch², 2oz Cu.
- 4. $I_{SD} \leq 22.5 \text{ A}$, di/dt $\leq 400 \text{ A/µs}$, $V_{DS(peak)} < V_{(BR)DSS}$, V_{DD} = 400 V.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R _{thj-case}	Thermal resistance junction-case max	0.83	°C/W
R _{thj-amb} ⁽¹⁾	Thermal resistance junction-ambient max	45	°C/W

1. When mounted on FR-4 board of inch2, 2oz Cu.

Electrical characteristics STL34N65M5

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	$I_D = 1 \text{ mA}, V_{GS} = 0$	650			V
I _{DSS}		V _{DS} = 650 V V _{DS} = 650 V, T _C =125 °C			1 100	μA μA
I _{GSS}	Gate-body leakage current (V _{DS} = 0)	V _{GS} = ± 25 V			±100	nA
V _{GS(th)}	Gate threshold voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	3	4	5	V
R _{DS(on)}	Static drain-source on- resistance	$V_{GS} = 10 \text{ V}, I_D = 12 \text{ A}$		0.099	0.120	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
C _{iss}	Input capacitance		-	2700	-	pF
C _{oss}	Output capacitance	V _{DS} = 100 V, f = 1 MHz,	-	75	-	pF
C _{rss}	Reverse transfer capacitance	$V_{GS} = 0$	-	6.3	-	pF
C _{o(er)} ⁽¹⁾	Equivalent output capacitance energy related	V _{GS} = 0,	-	63	-	pF
C _{o(tr)} ⁽²⁾	Equivalent output capacitance time related	$V_{DS} = 0$ to 80% $V_{(BR)DSS}$	-	220	-	pF
R _G	Intrinsic gate resistance	f = 1 MHz open drain	-	1.95	-	Ω
Qg	Total gate charge	V _{DD} = 520 V, I _D = 14 A,	-	62.5	-	nC
Q_{gs}	Gate-source charge	V _{GS} = 10 V (see <i>Figure 15</i>)	-	17	-	nC
Q _{gd}	Gate-drain charge		-	28	-	nC

^{1.} $C_{o(er)}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}



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^{2.} $C_{o(tr)}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t _{d(v)}	Voltage delay time		-	59	-	ns
t _{r(v)}	Voltage rise time	$V_{DD} = 400 \text{ V}, I_D = 18 \text{ A},$	-	8.7	-	ns
t _{f(i)}	Current fall time	$R_G = 4.7 \Omega$, $V_{GS} = 10 V$ (see <i>Figure 19</i>)	-	7.5	-	ns
t _{c(off)}	Crossing time		-	12	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I _{SD} ⁽¹⁾	Source-drain current		-		22.5	Α
I _{SDM} (1),(2)	Source-drain current (pulsed)		-		90	Α
V _{SD} (3)	Forward on voltage	I _{SD} = 22.5 A, V _{GS} = 0			1.5	V
t _{rr}	Reverse recovery time	I _{SD} = 22.5 A,	ı	330		ns
Q_{rr}	Reverse recovery charge	di/dt = 100 A/μs	-	5.3		μC
I _{RRM}	Reverse recovery current	V _{DD} = 100 V (see <i>Figure 16</i>)	-	32.5		Α
t _{rr}	Reverse recovery time	I _{SD} = 22.5 A,	-	412		ns
Q _{rr}	Reverse recovery charge	di/dt = 100 A/μs V _{DD} = 100 V, T _i = 150 °C	-	7.3		μC
I _{RRM}	Reverse recovery current	(see <i>Figure 16</i>)	•	35.5		Α

^{1.} The value is rated according to $\ensuremath{R_{thj\text{-}case}}$ and limited by package.

^{2.} Pulse width limited by safe operating area.

^{3.} Pulsed: pulse duration = $300 \mu s$, duty cycle 1.5%.

Electrical characteristics STL34N65M5

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

Figure 3. Thermal impedance

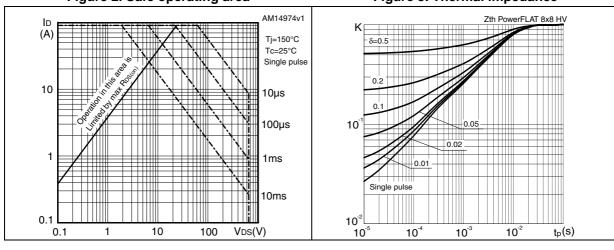


Figure 4. Output characteristics

Figure 5. Transfer characteristics

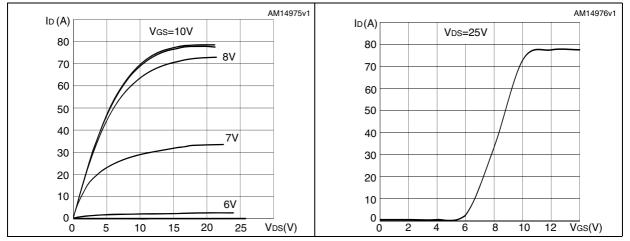
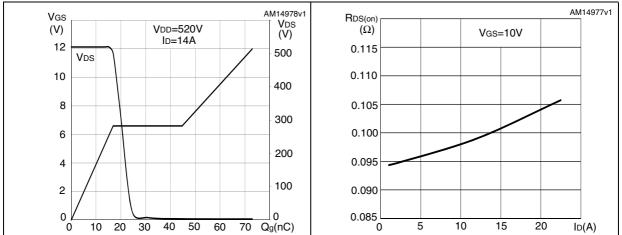


Figure 6. Gate charge vs gate-source voltage

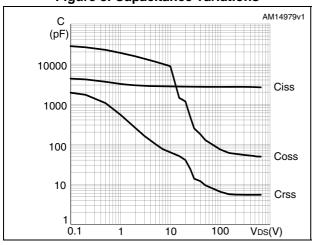
Figure 7. Static drain-source on-resistance



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Figure 8. Capacitance variations

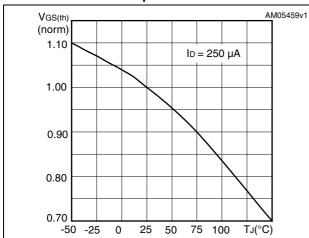
Figure 9. Output capacitance stored energy



AM14980v1 Eoss (µJ) 12 10 8 6 4 2 100 200 300 400 500 600 V_{DS}(V)

Figure 10. Normalized gate threshold voltage vs temperature

Figure 11. Normalized on-resistance vs temperature



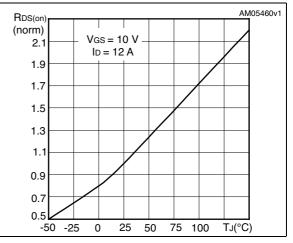
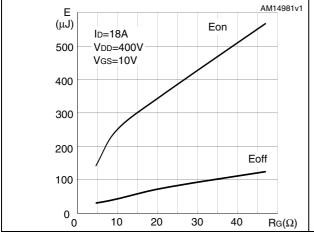
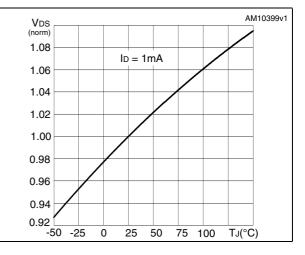


Figure 12. Switching losses vs gate resistance

Figure 13. Normalized V_{DS} vs temperature





1. Eon including reverse recovery of a SiC diode

Test circuits STL34N65M5

3 Test circuits

Figure 14. Switching times test circuit for resistive load

Figure 15. Gate charge test circuit

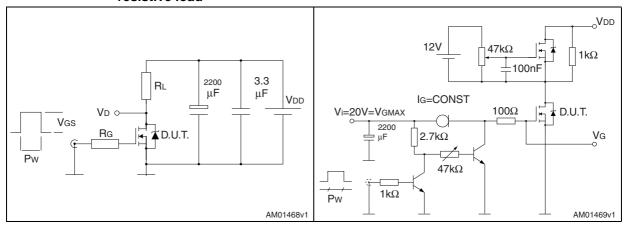


Figure 16. Test circuit for inductive load switching and diode recovery times

Figure 17. Unclamped inductive load test circuit

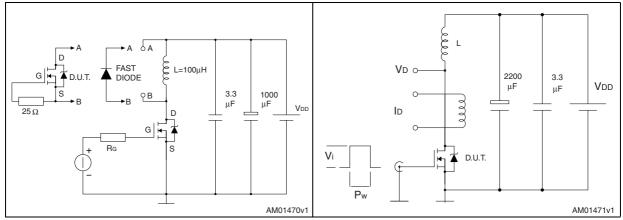
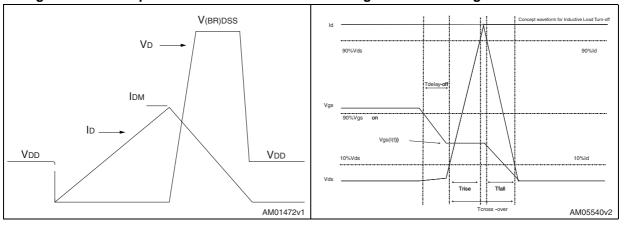


Figure 18. Unclamped inductive waveform

Figure 19. Switching time waveform



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4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.



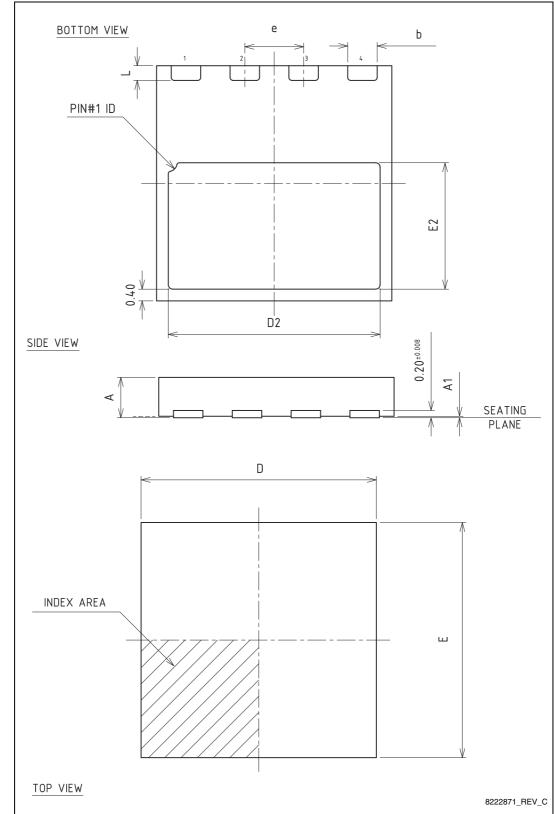


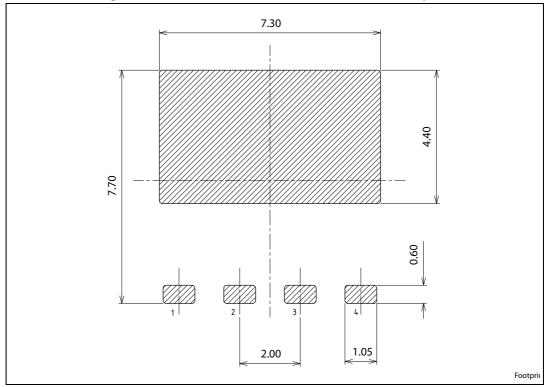
Figure 20. PowerFLAT™ 8x8 HV drawing mechanical data



Table 8. PowerFLAT™ 8x8 HV mechanical data

Dim.	mm				
Dilli.	Min.	Тур.	Max.		
А	0.80	0.90	1.00		
A1	0.00	0.02	0.05		
b	0.95	1.00	1.05		
D		8.00			
E		8.00			
D2	7.05	7.20	7.30		
E2	4.15	4.30	4.40		
е		2.00			
L	0.40	0.50	0.60		

Figure 21. PowerFLAT™ 8x8 HV recommended footprint



5 Packaging mechanical data

P2 (2.0±0.1)

P0 (4.0±0.1)

P1 (12.00±0.1)

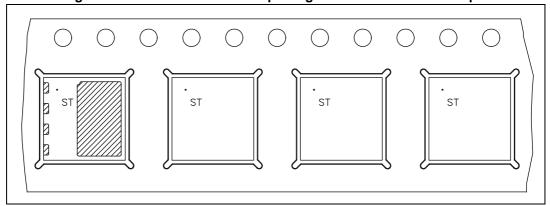
REF.

RO.25

Note: Base and Bulk quantity 3000 pcs

Figure 22. PowerFLAT™ 8x8 HV tape

Figure 23. PowerFLAT™ 8x8 HV package orientation in carrier tape.



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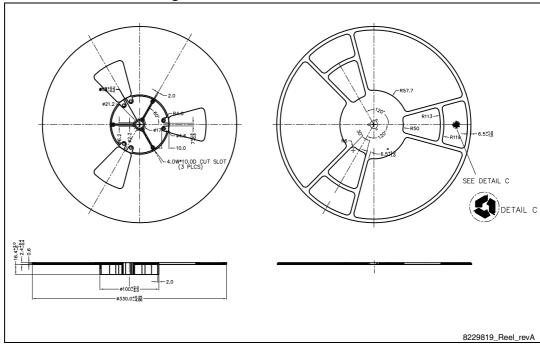


Figure 24. PowerFLAT™ 8x8 HV reel

Revision history STL34N65M5

6 Revision history

Table 9. Document revision history

Date	Revision	Changes
07-Apr-2014	1	First release.

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