

STL45N10F7AG

Automotive-grade N-channel 100 V, 20 mΩ typ., 18 A, STripFET™ F7 Power MOSFET in a PowerFLAT™ 5x6 package

Datasheet - production data

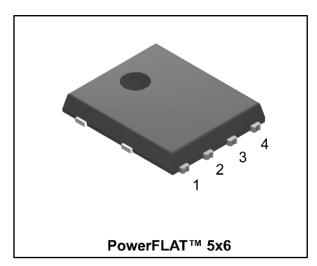
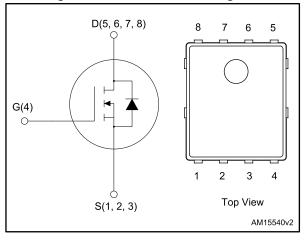


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max	ID	Ртот
STL45N10F7AG	100 V	24 mΩ	18 A	72 W

AEC-Q101 qualified



- Among the lowest R_{DS(on)} on the market
- Excellent FoM (figure of merit)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness
- Wettable flank package

Applications

• Switching applications

Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low onstate resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Table 1: Device summary

Order code	Marking	Package	Packing
STL45N10F7AG	45N10F7	PowerFLAT™ 5x6	Tape and reel

Contents STL45N10F7AG

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STL45N10F7AG Electrical ratings

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit	
V _{DS}	Drain-source voltage	100	V	
V _{GS}	Gate-source voltage	±20	V	
I _D ⁽¹⁾	Drain current (continuous) at T _C = 25 °C	18	Α	
I _D ⁽¹⁾	Drain current (continuous) at T _C = 100 °C	18	Α	
I _{DM} ⁽²⁾	Drain current (pulsed)	72	Α	
Ртот	Total dissipation at T _C = 25 °C	72	W	
E _{AS} ⁽³⁾	Single pulse avalanche energy	150	mJ	
TJ	Operating junction temperature range			
T _{stg}	Storage temperature range	-55 to 175 °C		

Notes:

Table 3: Thermal resistance

Symbol	Parameter	Value	Unit
R _{thj-case}	Thermal resistance junction-case	2.08	°C/W
R _{thj-pcb} (1)	Thermal resistance junction-pcb	31.3	°C/W

Notes:

⁽¹⁾Limited by package.

 $[\]ensuremath{^{(2)}}\mbox{Pulse}$ width limited by safe operating area.

 $^{^{(3)}}$ Starting $T_j = 25$ °C, $I_D = 9$ A, $V_{DD} = 60$ V

 $^{^{(1)}}$ When mounted on FR-4 board of 1inch², 2oz Cu, t < 10 s

Electrical characteristics STL45N10F7AG

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4: On/off states

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	V_{GS} = 0 V, I_{D} = 250 μA	100			V
	Zara gata valtaga drain	$V_{GS} = 0 \text{ V}, V_{DS} = 100 \text{ V}$			1	
I _{DSS}	Zero gate voltage drain current	$V_{GS} = 0 \text{ V}, V_{DS} = 100 \text{ V};$ $T_{C} = 125 \text{ °C}^{(1)}$			10	μΑ
I _{GSS}	Gate body leakage current	$V_{DS} = 0 \text{ V}, V_{GS} = 20 \text{ V}$			100	nA
V _{GS(th)}	Gate threshold voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	2.5		4.5	V
R _{DS(on)}	Static drain-source on- resistance	V _{GS} = 10 V, I _D = 9 A		20	24	mΩ

Notes:

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
Ciss	Input capacitance		-	1450	1	pF
Coss	Output capacitance	V _{DS} = 50 V, f = 1 MHz,	-	350	1	pF
Crss	Reverse transfer capacitance	$V_{GS} = 0 V$	-	25	-	pF
Qg	Total gate charge	$V_{DD} = 50 \text{ V}, I_{D} = 18 \text{ A}, V_{GS} = 0$	-	19.5	ı	nC
Q _{gs}	Gate-source charge	to 10 V (see Figure 14: "Test circuit	-	9.1	-	nC
Q_{gd}	Gate-drain charge	for gate charge behavior")	-	4.3	-	nC

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t _{d(on)}	Turn-on delay time	$V_{DD} = 50 \text{ V}, I_D = 9 \text{ A},$	-	15	-	ns
tr	Rise time	$R_G = 4.7 \Omega$, $V_{GS} = 10 V$ (see Figure 13: "Test circuit	ı	5.5	1	ns
t _{d(off)}	Turn-off delay time	for resistive load switching	1	17	-	ns
tf	Fall time	times" and Figure 18: "Switching time waveform")	-	5	-	ns

 $[\]ensuremath{^{(1)}}\mbox{Defined}$ by design, not subject to production test.

Table 7: Source drain diode

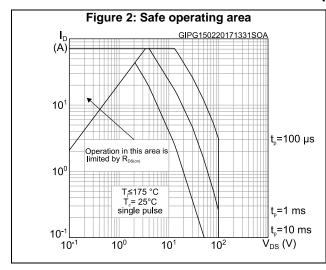
Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I _{SD}	Source-drain current		-		18	Α
I _{SDM} ⁽¹⁾	Source-drain current (pulsed)		-		72	Α
V _{SD} ⁽²⁾	Forward on voltage	I _{SD} = 9 A, V _{GS} = 0 V	-		1.2	V
t _{rr}	Reverse recovery time	I _{SD} = 18 A, di/dt = 100 A/μs,	-	46		ns
Qrr	Reverse recovery charge	V _{DD} = 80 V (see Figure 15: "Test circuit	-	46		nC
I _{RRM}	Reverse recovery current	for inductive load switching and diode recovery times")	-	2		Α

Notes:

⁽¹⁾Pulse width limited by safe operating area

 $^{^{(2)}\}text{Pulsed:}$ pulse duration=300 $\mu\text{s,}$ duty cycle 1.5%

2.1 Electrical characteristics (curves)



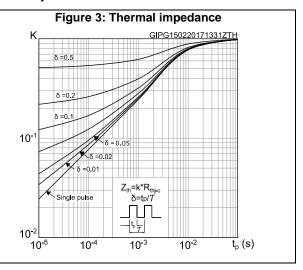


Figure 4: Output characteristics

(A)

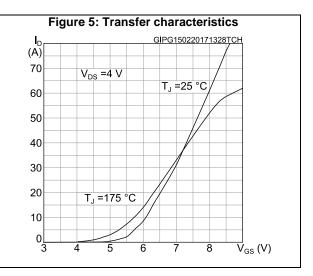
(V_{GS}= 9, 10 V

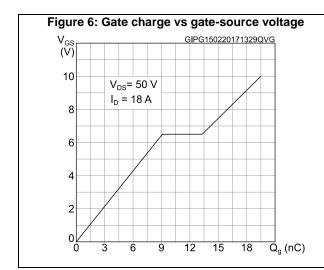
(V_{GS}= 8 V

(V_{GS}= 7 V

(V_{GS}= 6 V

(





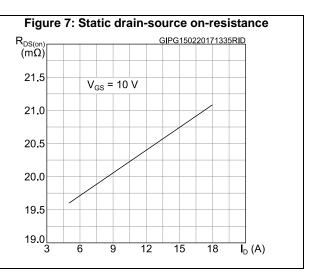
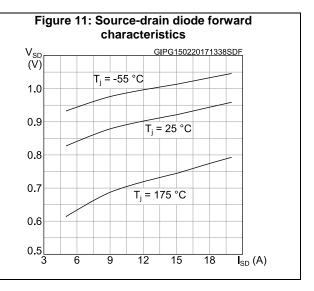
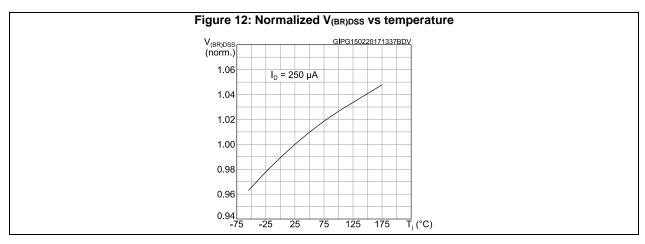


Figure 8: Capacitance variations C (pF) GIPG150220171329CVR C_{ISS} 10^{3} C_{oss} 10² f = 1 MHz C_{RSS} 10¹ 20 100 40 60 80 $\overline{V}_{DS}(V)$

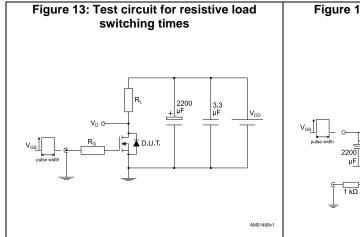
Figure 9: Normalized gate threshold voltage vs temperature V_{GS(th)} (norm.) GIPG150220171337VTH 1.1 $I_D = 250 \, \mu A$ 1.0 0.9 8.0 0.7 0.6 -75 -25 25 75 125 T_i (°C) 175

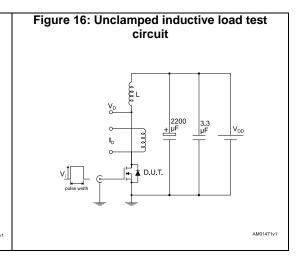


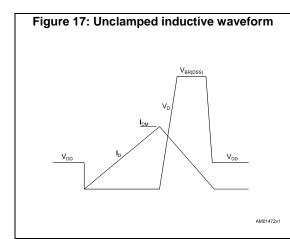


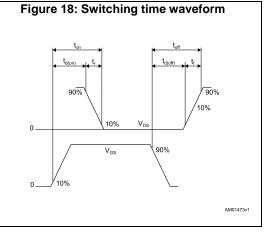
Test circuits STL45N10F7AG

3 Test circuits









Package information 4

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

PowerFLAT™ 5x6 WF type R package information 4.1

BOTTOM VIEW 5 E3 E3 Detail A Scale 3:1 62 0.08 L(x4) b(x8) D5(x4) D4 SIDE VIEW A Detail A ŏ A0Y5 8231817 R WF Rev 14

Figure 19: PowerFLAT™ 5x6 WF type R package outline

Table 8: PowerFLAT™ 5x6 WF type R mechanical data

	Table 8: PowerFLAT *** 5X6	mm	lata
Dim.	Min.	Тур.	Max.
А	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
С	5.80	6.00	6.10
D	5.00	5.20	5.40
D2	4.15		4.45
D3	4.05	4.20	4.35
D4	4.80	5.00	5.10
D5	0.25	0.4	0.55
D6	0.15	0.3	0.45
е		1.27	
E	6.20	6.40	6.60
E2	3.50		3.70
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28
E6	0.20	0.325	0.45
E7	0.85	1.00	1.15
E9	4.00	4.20	4.40
E10	3.55	3.70	3.85
K	1.275		1.575
L	0.725	0.825	0.925
L1	0.175	0.275	0.375
θ	0°		12°

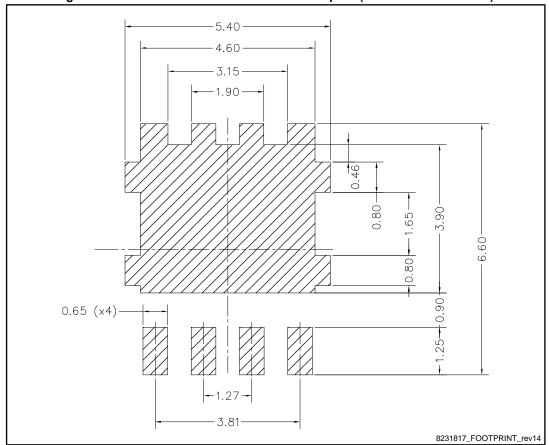


Figure 20: PowerFLAT™ 5x6 recommended footprint (dimensions are in mm)

Package information STL45N10F7AG

4.2 PowerFLAT™ 5x6 packing information

Figure 21: PowerFLAT™ 5x6 WF tape (dimensions are in mm)

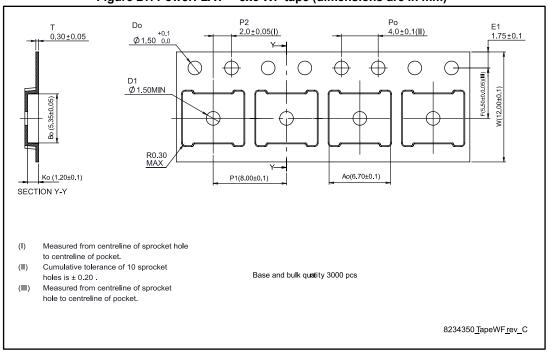
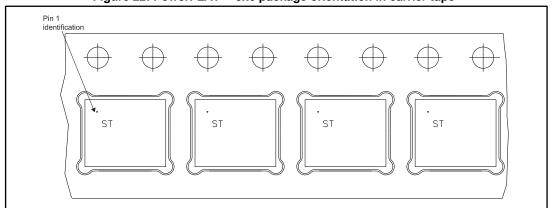


Figure 22: PowerFLAT™ 5x6 package orientation in carrier tape



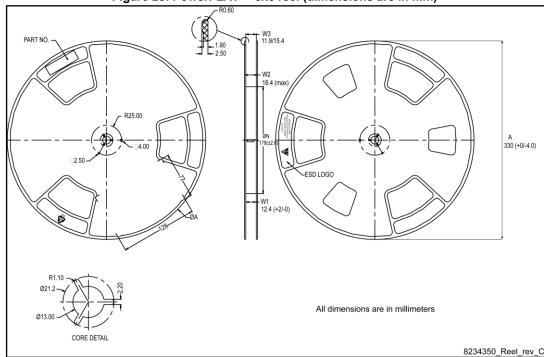


Figure 23: PowerFLAT™ 5x6 reel (dimensions are in mm)

Revision history STL45N10F7AG

5 Revision history

Table 9: Document revision history

Date	Revision	Changes
16-Feb-2017	1	First release.

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