

P-channel 20 V, 0.087 Ω typ., 4 A STripFET™ VII DeepGATE™ Power MOSFET in a PowerFLAT™ 2x2 package

Datasheet - production data

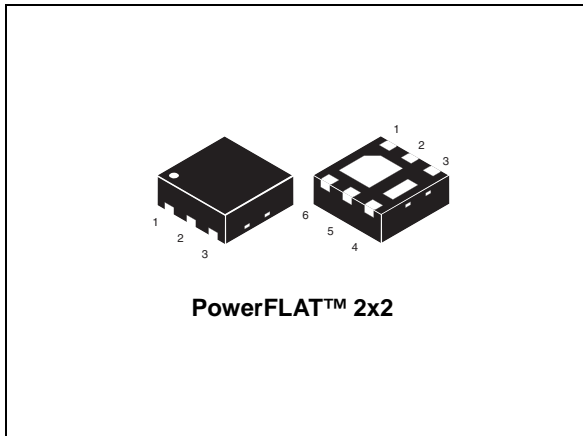
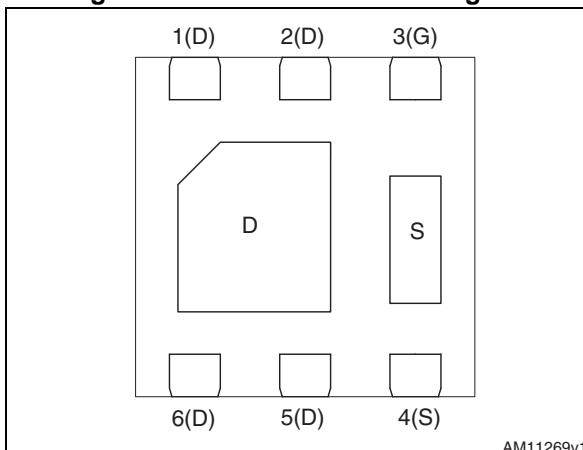


Figure 1. Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max	I _D
STL4P2UH7	20 V	0.1 Ω @ 4.5 V	4 A

- Ultra logic level
- Extremely low on-resistance R_{DS(on)}
- High avalanche ruggedness
- Low gate drive power losses

Applications

- Switching applications

Description

This device exhibits low on-state resistance and capacitance for improved conduction and switching performance.

Table 1. Device summary

Order code	Marking	Package	Packaging
STL4P2UH7	4L2U	PowerFLAT™ 2x2	Tape and reel

Note: For the P-channel Power MOSFET the actual polarity of the voltages and the current must be reversed.

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	20	V
V_{GS}	Gate-source voltage	± 8	V
$I_D^{(1)}$	Drain current (continuous) at $T_{pcb} = 25\text{ }^\circ\text{C}$	4	A
$I_D^{(1)}$	Drain current (continuous) at $T_{pcb} = 100\text{ }^\circ\text{C}$	2.5	A
$I_{DM}^{(1)(2)}$	Drain current (pulsed)	16	A
$P_{TOT}^{(1)}$	Total dissipation at $T_{pcb} = 25\text{ }^\circ\text{C}$	2.4	W
T_{stg}	Storage temperature	- 55 to 150	$^\circ\text{C}$
T_j	Max. operating junction temperature	150	$^\circ\text{C}$

1. The value is rated according to $R_{thj-pcb}$
2. Pulse width limited by safe operating area

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max, single operation	52	$^\circ\text{C}/\text{W}$

1. When mounted on 1inch² FR-4 board, 2 oz Cu.

Note: For the P-channel Power MOSFET the actual polarity of the voltages and the current must be reversed.

2 Electrical characteristics

($T_C = 25\text{ }^\circ\text{C}$ unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0, I_D = 250\ \mu\text{A}$	20			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0, V_{DS} = 20\ \text{V}$			1	μA
I_{GSS}	Gate-body leakage current	$V_{DS} = 0, V_{GS} = \pm 8\ \text{V}$			10	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	0.4		1	V
$R_{DS(on)}$	Static drain-source on- resistance	$V_{GS} = 4.5\ \text{V}, I_D = 2\ \text{A}$		0.087	0.1	Ω
		$V_{GS} = 2.5\ \text{V}, I_D = 2\ \text{A}$		0.11	0.13	Ω
		$V_{GS} = 1.8\ \text{V}, I_D = 2\ \text{A}$		0.145	0.18	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{GS} = 0, V_{DS} = 10\ \text{V}, f = 1\ \text{MHz}$	-	510	-	pF
C_{oss}	Output capacitance		-	66	-	pF
C_{riss}	Reverse transfer capacitance		-	44	-	pF
Q_g	Total gate charge	$V_{DD} = 10\ \text{V}, I_D = 3\ \text{A},$ $V_{GS} = 4.5\ \text{V}$ (see Figure 14)	-	4.8	-	nC
Q_{gs}	Gate-source charge		-	0.7	-	nC
Q_{gd}	Gate-drain charge		-	0.8	-	nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 10\ \text{V}, I_D = 1.5\ \text{A},$ $R_G = 4.7\ \Omega, V_{GS} = 4.5\ \text{V}$ (see Figure 15)	-	9	-	ns
t_r	Rise time		-	21	-	ns
$t_{d(off)}$	Turn-off delay time		-	40	-	ns
t_f	Fall time		-	19	-	ns

Note: For the P-channel Power MOSFET the actual polarity of the voltages and the current must be reversed.

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		4	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		16	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 1\text{ A}$, $V_{GS} = 0$	-		1	V
t_{rr}	Reverse recovery time	$V_{DD} = 16\text{ V}$	-	12.8		ns
Q_{rr}	Reverse recovery charge	$di/dt = 100\text{ A}/\mu\text{s}$, $I_{SD} = 1\text{ A}$	-	5		nC
I_{RRM}	Reverse recovery current	$T_j = 150\text{ }^\circ\text{C}$ (see Figure 15)	-	0.8		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

For the P-channel Power MOSFET the actual polarity of the voltages and the current must be reversed.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

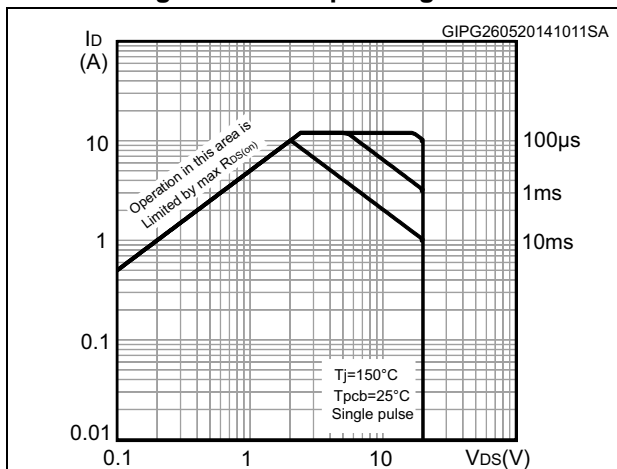


Figure 3. Thermal impedance

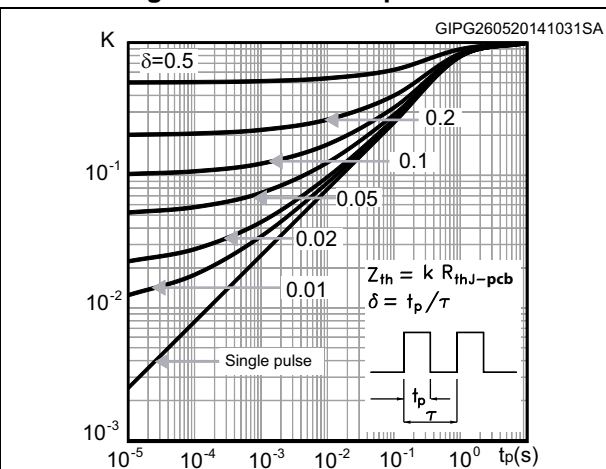


Figure 4. Output characteristics

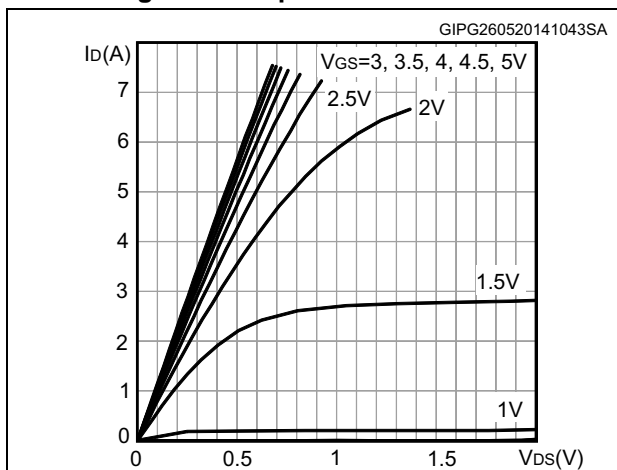


Figure 5. Transfer characteristics

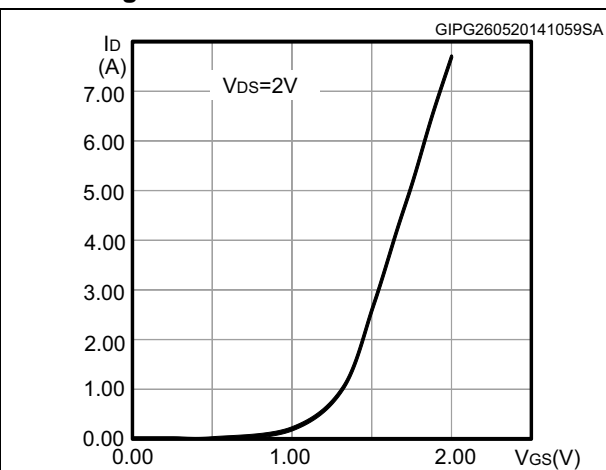


Figure 6. Gate charge vs gate-source voltage

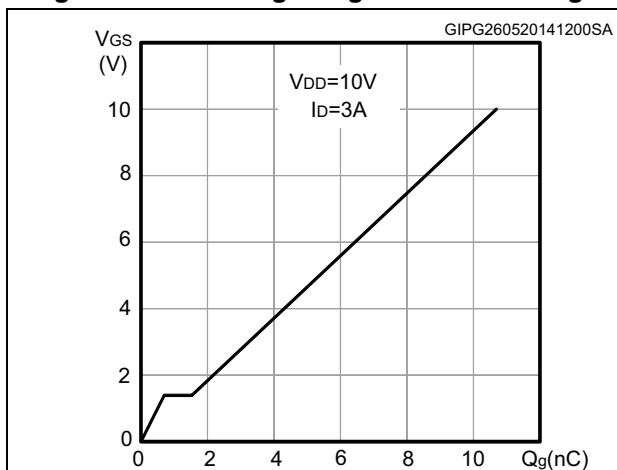


Figure 7. Static drain-source on-resistance

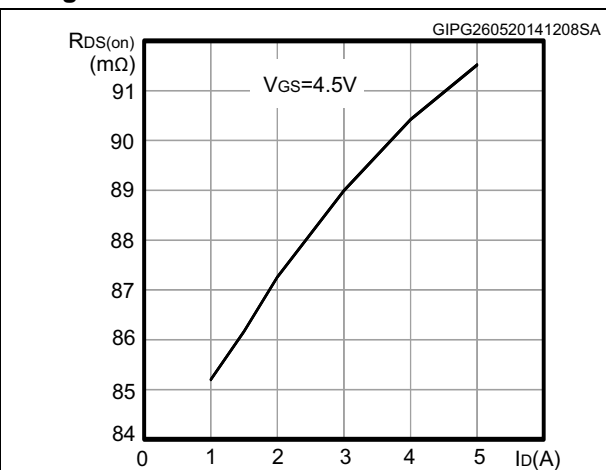


Figure 8. Capacitance variations

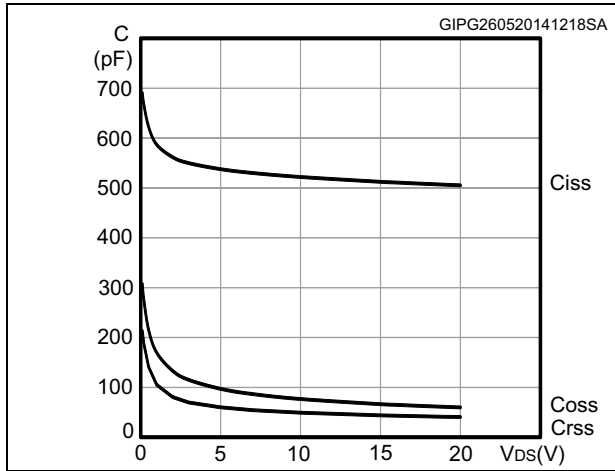


Figure 9. Normalized gate threshold voltage vs temperature

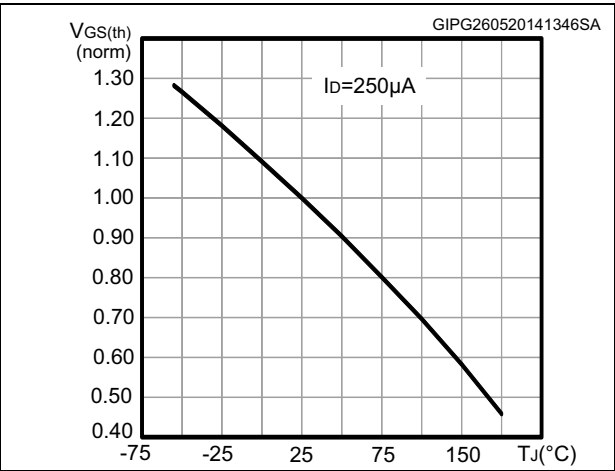


Figure 10. Normalized on-resistance vs temperature

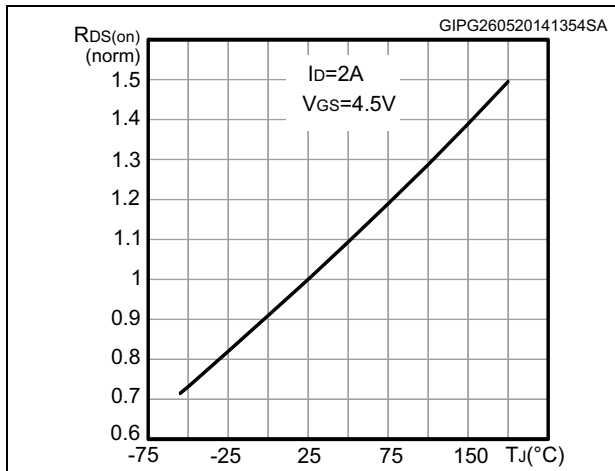


Figure 11. Normalized V_{(BR)DSS} vs temperature

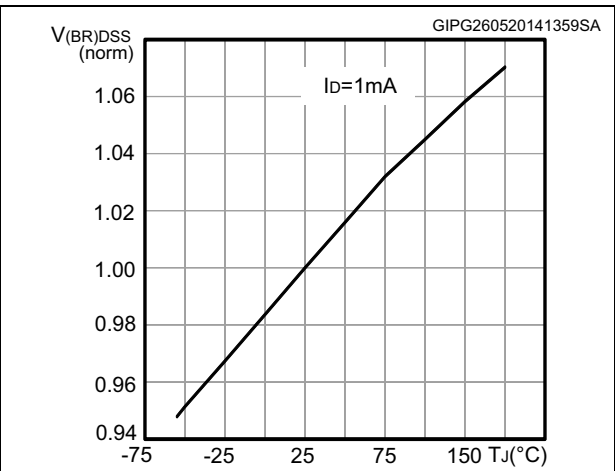
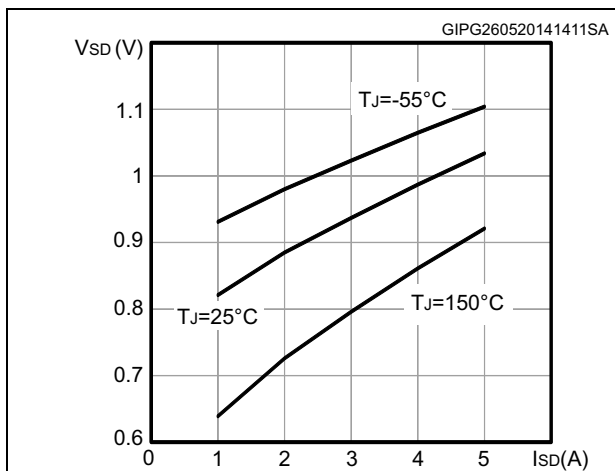


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

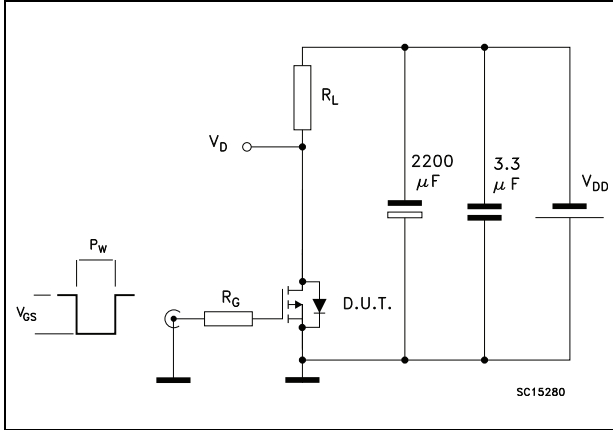


Figure 14. Gate charge test circuit

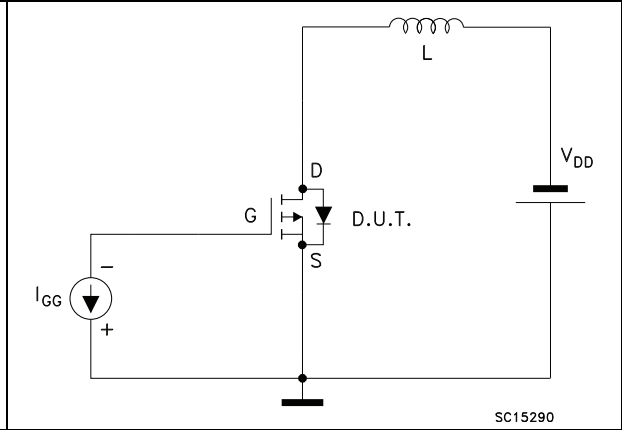
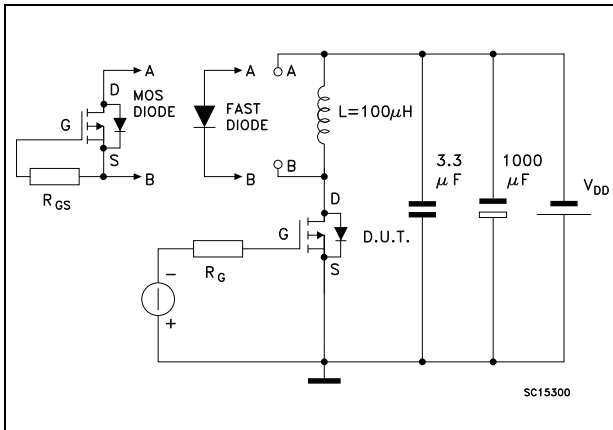


Figure 15. Test circuit for inductive load switching and diode recovery times



4 Package mechanical data

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Figure 16. Drawing dimension PowerFLAT™ 2 x 2

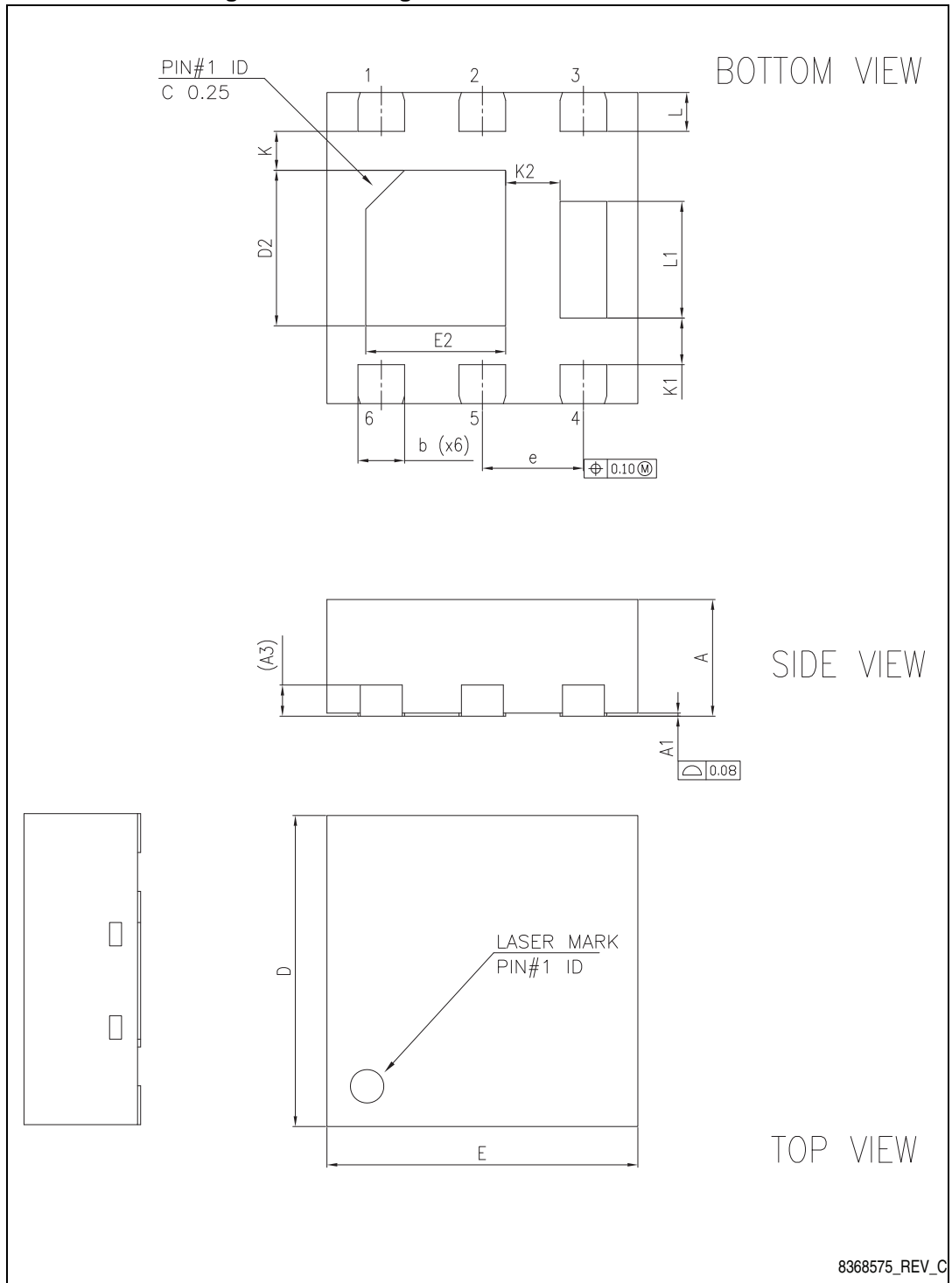
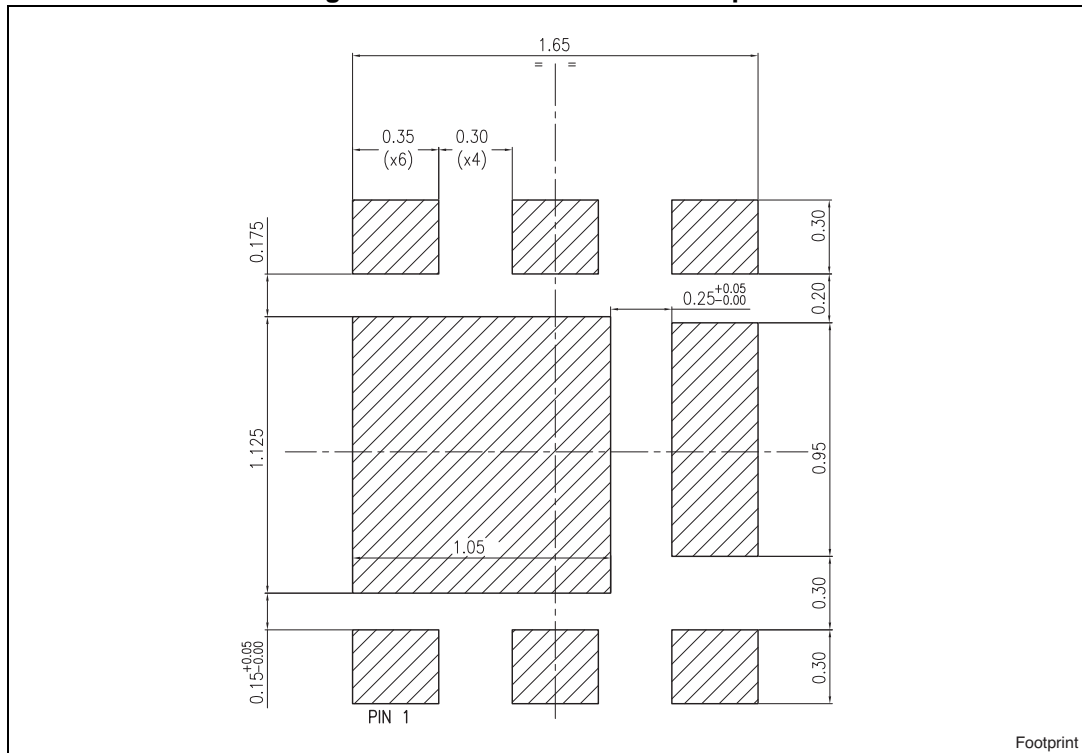


Table 8. PowerFLAT™ 2 x 2 mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20	
b	0.25	0.30	0.35
D	1.90	2.00	2.10
E	1.90	2.00	2.10
D2	0.90	1.00	1.10
E2	0.80	0.90	1.00
e	0.55	0.65	0.75
K	0.15	0.25	0.35
K1	0.20	0.30	0.40
K2	0.25	0.35	0.45
L	0.20	0.25	0.30
L1	0.65	0.75	0.85

Figure 17. PowerFLAT™ 2 x 2 footprint



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
22-Jul-2013	1	First release.
30-May-2014	2	<ul style="list-style-type: none">– Document status promoted from target to production data– Modified: title– Modified: $R_{DS(on)}$ typical and maximum values in Table 4– Modified: V_{DS}, V_{DD}, I_D and typical values in Table 5 and 6– Modified: typical values in Table 7– Added: Section 2.1: Electrical characteristics (curves)– Minor text changes
16-Jul-2014	3	<ul style="list-style-type: none">– Modified: V_{DS} value in Table 2– Minor text changes

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