

Dual N-channel 60 V, 9 mΩ typ., 57 A STripFET™ F7 Power MOSFET in a PowerFLAT™ 5x6 double island package

Datasheet - production data

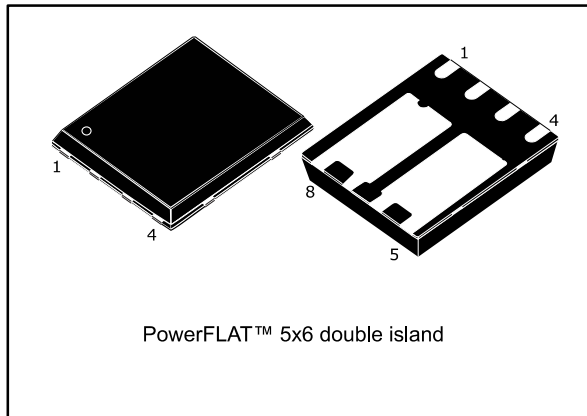
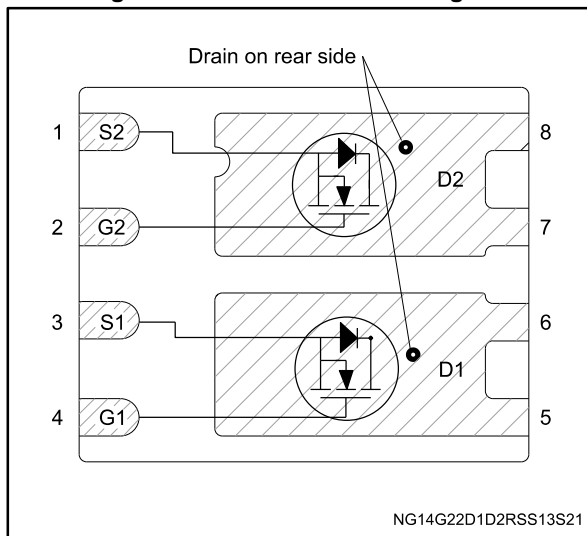


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D
STL50DN6F7	60 V	11 mΩ	57 A

- Among the lowest R_{DS(on)} on the market
- Excellent figure of merit (FoM)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness

Applications

- Switching applications

Description

This dual N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Table 1: Device summary

Order code	Marking	Package	Packaging
STL50DN6F7	50DN6F7	PowerFLAT™ 5x6 double island	Tape and reel

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	60	V
V_{GS}	Gate source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	57	A
	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	41	
$I_{DM}^{(1)(2)}$	Drain current (pulsed)	228	A
$I_D^{(3)}$	Drain current (continuous) at $T_{pcb} = 25\text{ }^\circ\text{C}$	15	A
	Drain current(continuous) at $T_{pcb} = 100\text{ }^\circ\text{C}$	11	
$I_{DM}^{(2)(3)}$	Drain current (pulsed)	60	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	62.5	W
	Total dissipation at $T_{pcb} = 25\text{ }^\circ\text{C}$	4.8	
T_J	Operating junction temperature	-55 to 175	$^\circ\text{C}$
T_{stg}	Storage temperature		

Notes:

- (1) This value is rated according to R_{thj-c}
- (2) Pulse width limited by safe operating area.
- (3) This value is rated according to $R_{thj-pcb}$

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	2.4	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	31.3	$^\circ\text{C}/\text{W}$

Notes:

- (1) When mounted on FR-4 board of 1inc2, 2oz Cu, $t < 10\text{ sec}$

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4: On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	V _{GS} = 0 V, I _D = 1 mA	60			V
I _{DSS}	Zero gate voltage drain current	V _{DS} = 60 V, V _{GS} = 0 V			1	μA
I _{GSS}	Gate-body leakage current	V _{DS} = 0 V, V _{GS} = 20 V			100	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	2		4	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 7.5 A		9	11	mΩ

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 30V, f = 1 MHz, V _{GS} = 0 V	-	1035	-	pF
C _{oss}	Output capacitance		-	450	-	pF
C _{rss}	Reverse transfer capacitance		-	53	-	pF
Q _g	Total gate charge	V _{DD} = 30 V, I _D = 15 A, V _{GS} = 10 V (see Figure 14: "Test circuit for gate charge behavior")	-	17	-	nC
Q _{gs}	Gate-source charge		-	5.7	-	nC
Q _{gd}	Gate-drain charge		-	5.7	-	nC

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 30V, I _D = 7.5 A, R _G = 4.7 Ω, V _{GS} = 10 V (see Figure 13: "Test circuit for resistive load switching times")	-	14.5	-	ns
t _r	Rise time		-	15.3	-	ns
t _{d(off)}	Turn-off delay time		-	19.4	-	ns
t _f	Fall time		-	8	-	ns

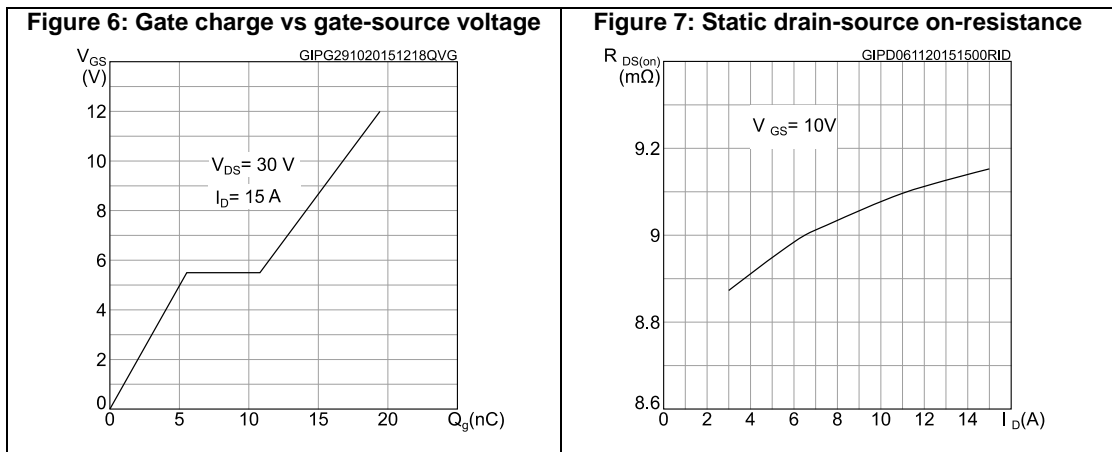
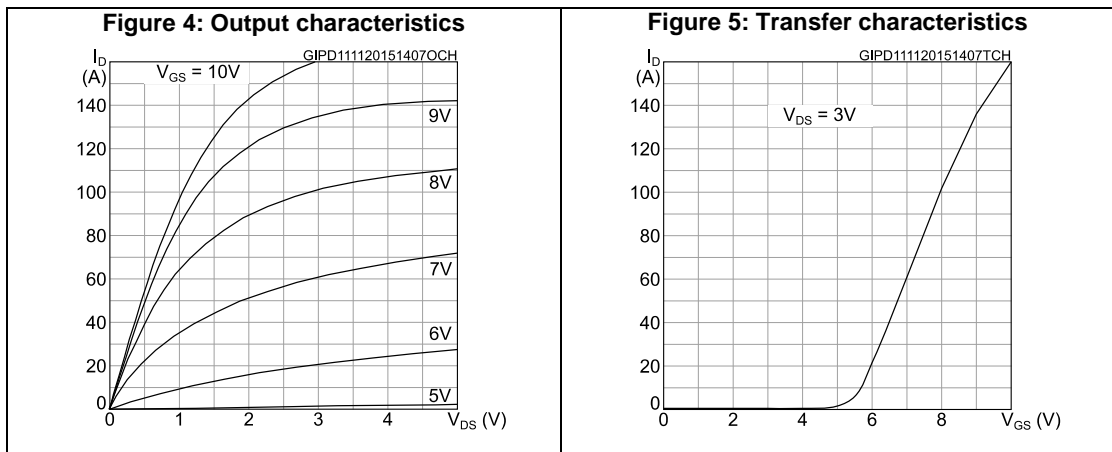
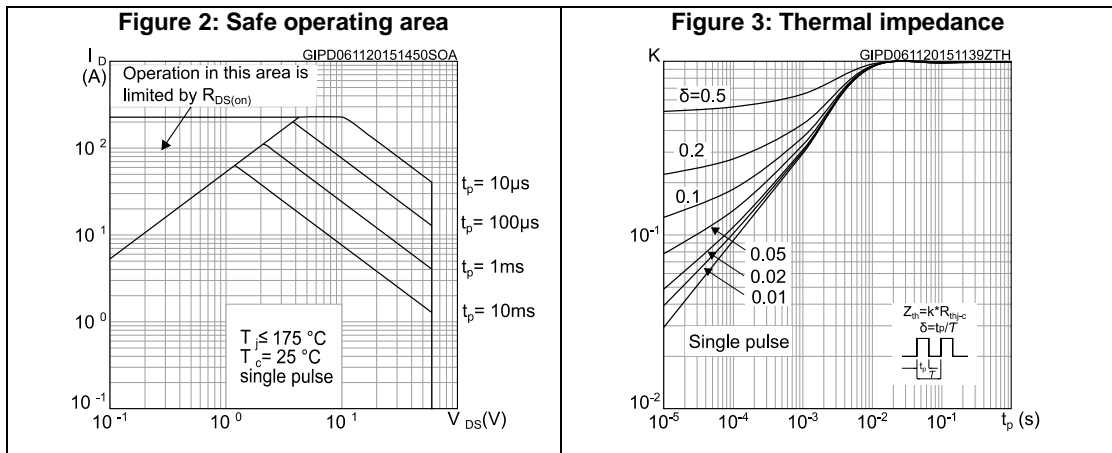
Table 7: Source-drain diode

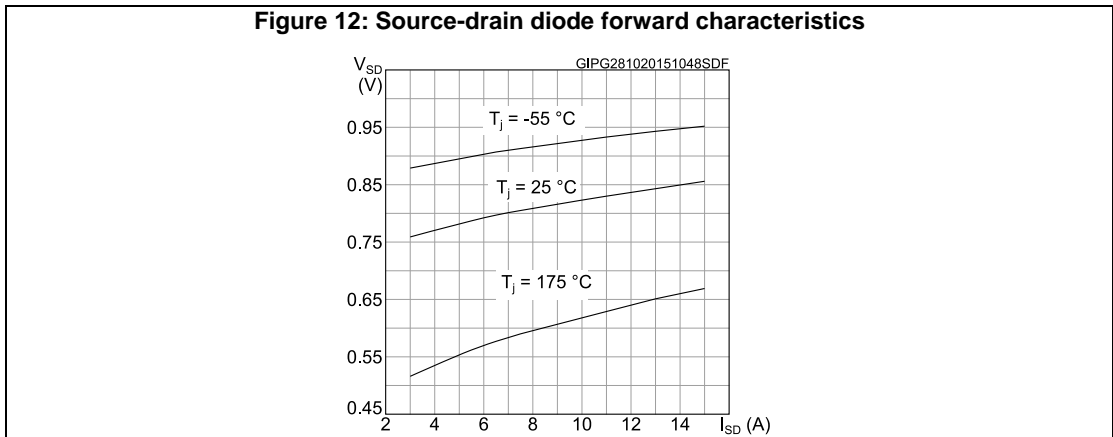
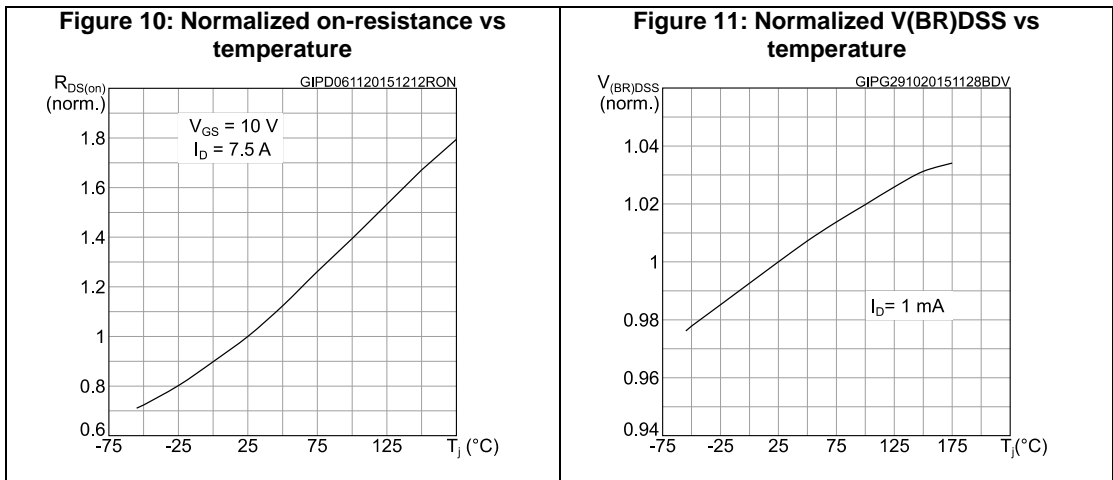
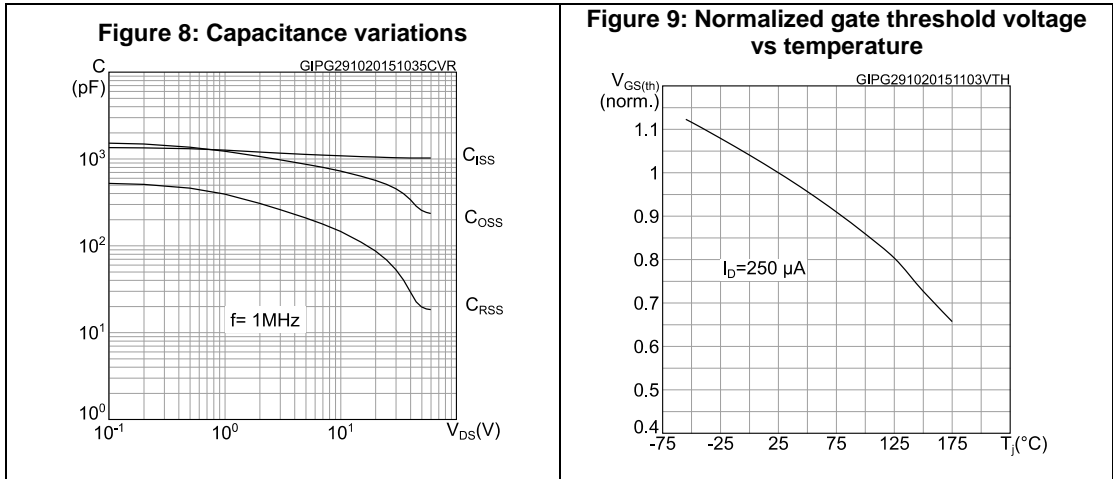
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{SD} ⁽¹⁾	Forward on voltage	I _{SD} = 15 A, V _{GS} = 0 V	-		1.2	V
t _{rr}	Reverse recovery time	I _{SD} = 15 A, di/dt = 100 A/μs, V _{DD} = 48 V (see Figure 15: "Test circuit for inductive load switching and diode recovery times")	-	26.8		ns
Q _{rr}	Reverse recovery charge		-	14.2		nC
I _{RRM}	Reverse recovery current		-	1.06		A

Notes:

⁽¹⁾Pulsed: pulse duration = 300 μs, duty cycle 1.5%

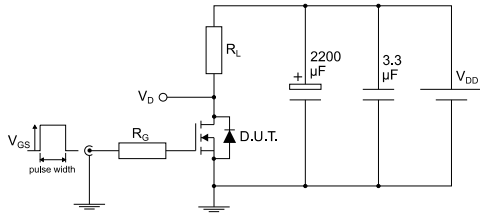
2.1 Electrical characteristics(curve)





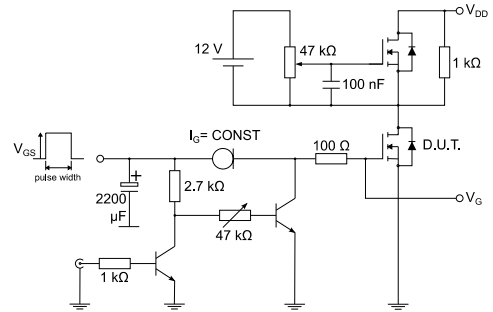
3 Test circuits

Figure 13: Test circuit for resistive load switching times



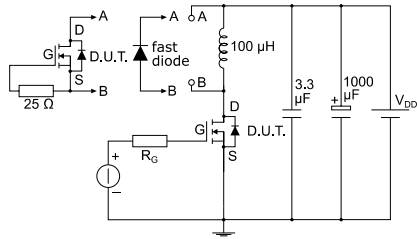
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Figure 14: Test circuit for gate charge behavior



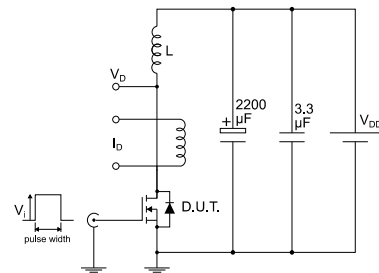
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Figure 15: Test circuit for inductive load switching and diode recovery times



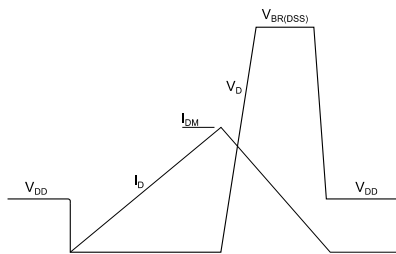
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Figure 16: Unclamped inductive load test circuit



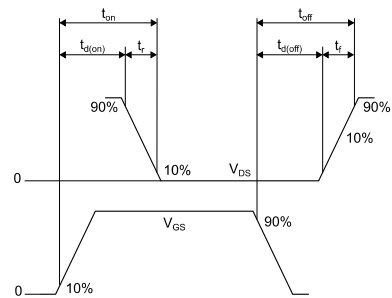
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Figure 17: Unclamped inductive waveform



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Figure 18: Switching time waveform



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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 PowerFLAT 5x6 double island type R package information

Figure 19: PowerFLAT™ 5x6 double island type R package outline

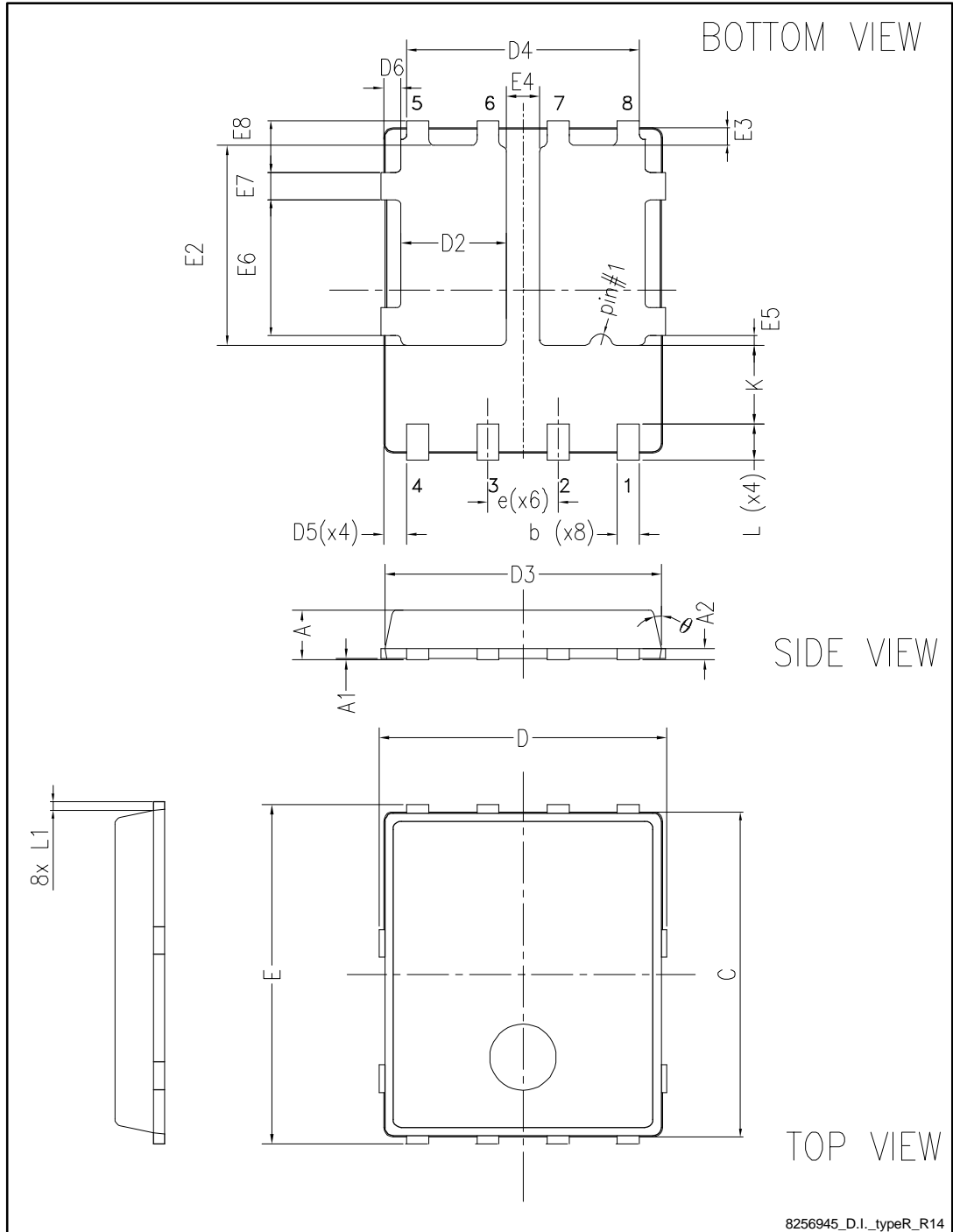
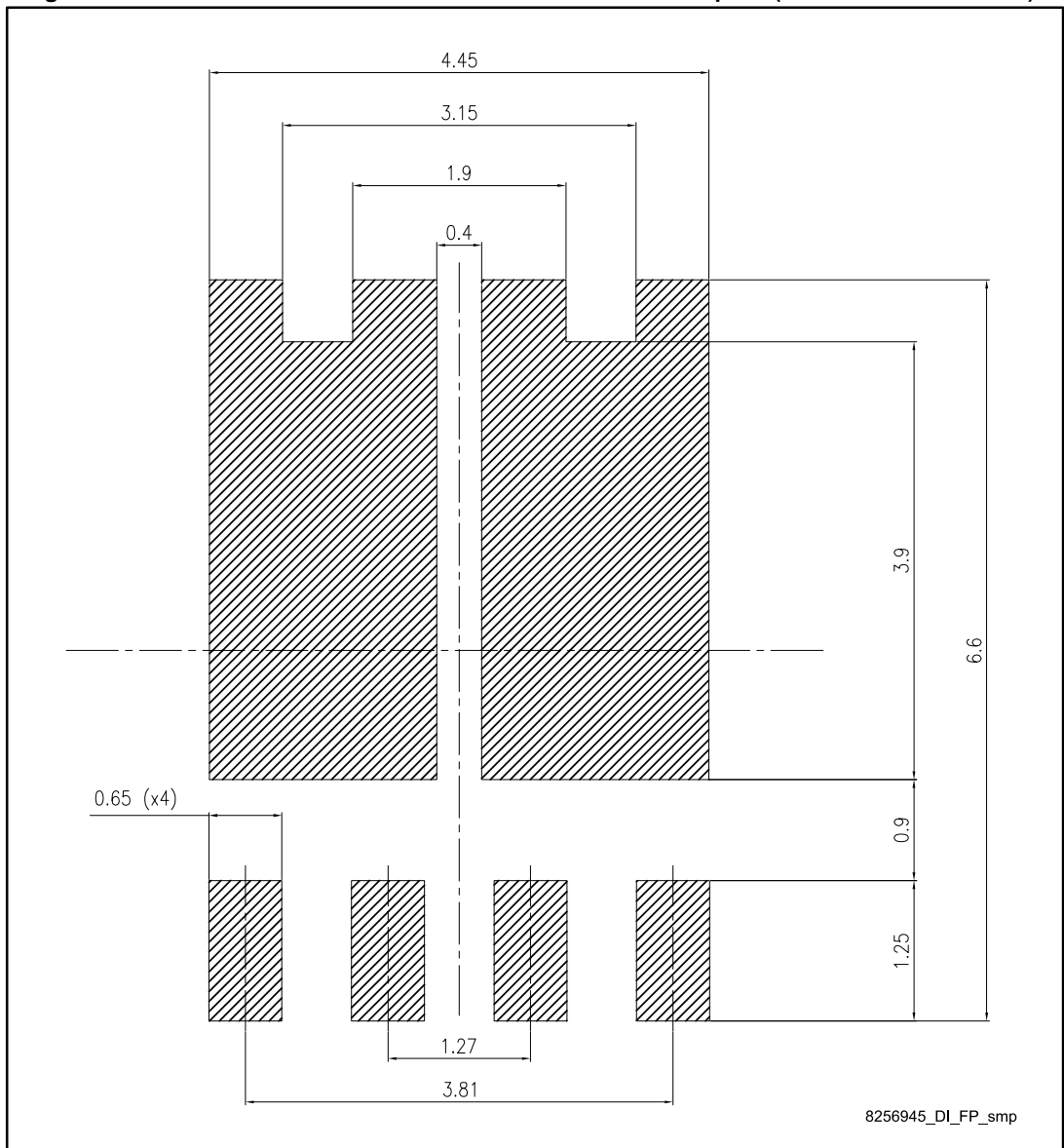


Table 8: PowerFLAT™ 5x6 double island type R mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.80	6.00	6.20
D	5.00	5.20	5.40
D2	1.68		1.88
D3	4.80	5.00	5.20
D4	4.05	4.20	4.35
D5	0.25	0.40	0.55
D6	0.15	0.30	0.45
e		1.27	
E	5.95	6.15	6.35
E2	3.50		3.70
E3	0.20	0.325	0.45
E4	0.55		0.75
E5	0.08		0.28
E6	2.35		2.55
E7	0.40		0.60
E8	0.75	0.90	1.05
L	0.60		0.80
L1	0.05	0.15	0.25
K	1.275		1.575
θ	0°		12°

Figure 20: PowerFLAT™ 5x6 double island recommended footprint (dimensions are in mm)



4.2 PowerFLAT™ 5x6 packing information

Figure 21: PowerFLAT™ 5x6 tape (dimensions are in mm)

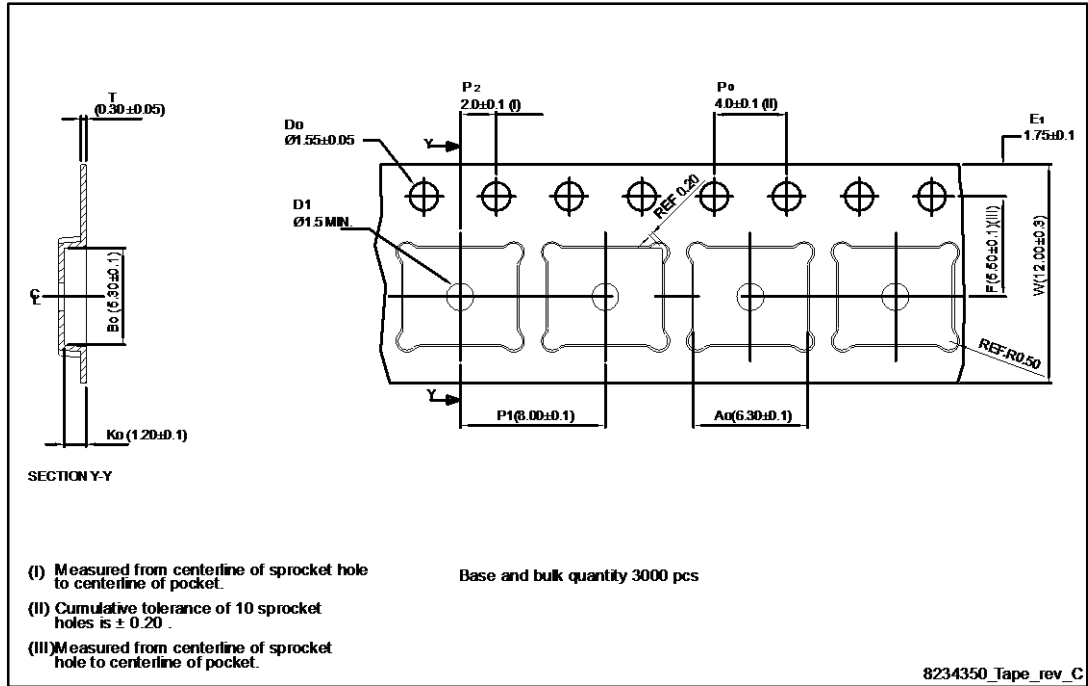


Figure 22: PowerFLAT™ 5x6 package orientation in carrier tape

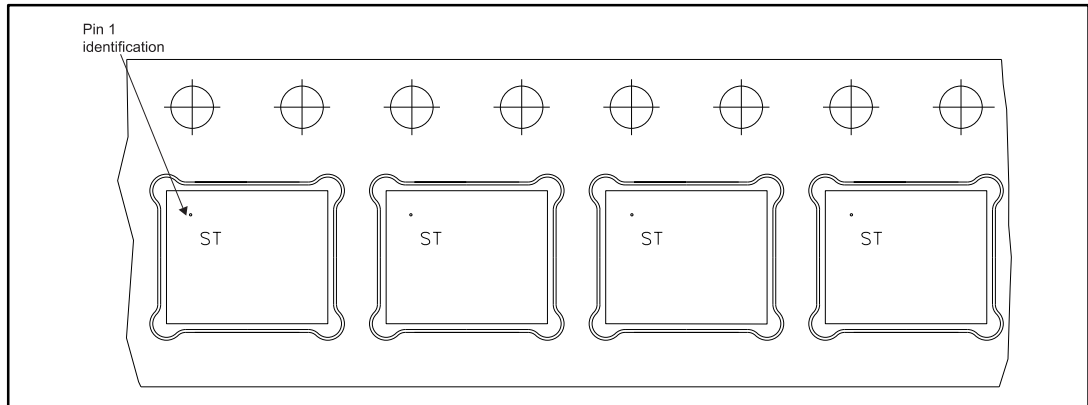
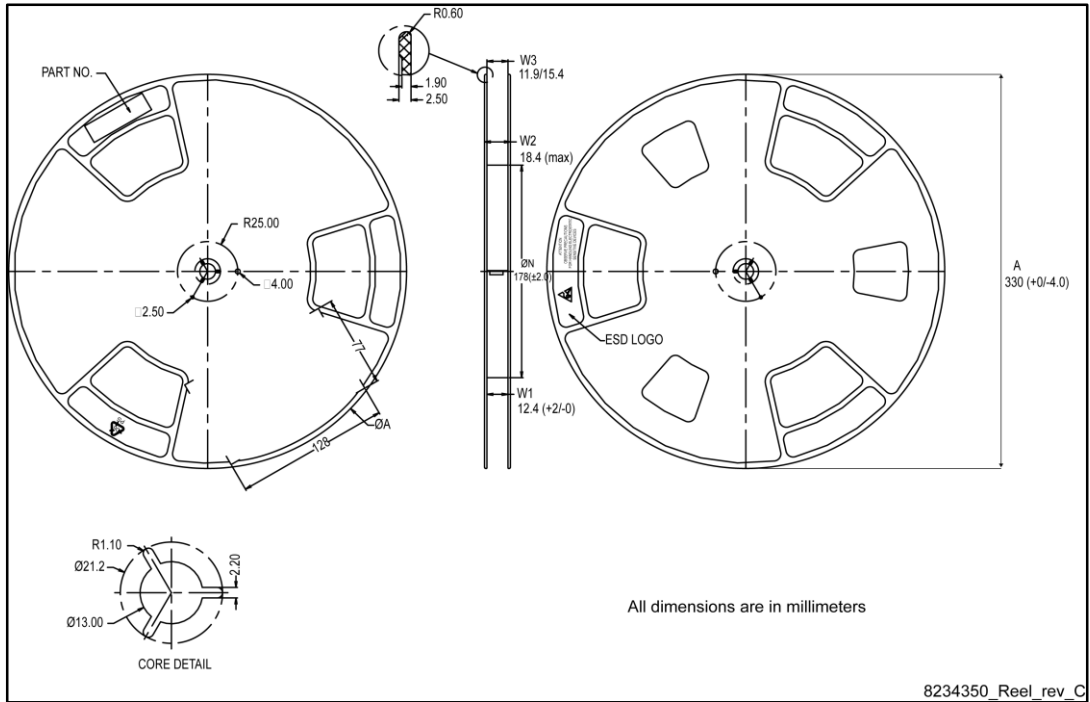


Figure 23: PowerFLAT™ 5x6 reel



5 Revision history

Table 9: Document revision history

Date	Revision	Changes
17-Jul-2015	1	First release.
13-Nov-2015	2	Document status promoted from preliminary to production data. Updated title and features in cover page. Updated <i>Table 2: "Absolute maximum ratings"</i> and <i>Section 4: "Electrical characteristics"</i> . Added <i>Section 4.1: "Electrical characteristics(curve)"</i> Minor text changes.

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