



STL51N3LLH5

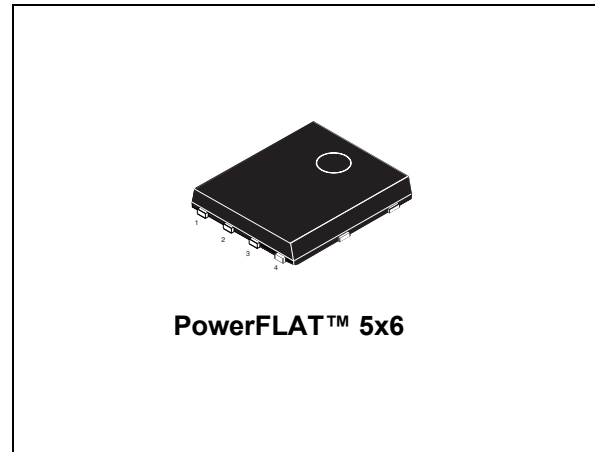
N-channel 30 V, 0.0105 Ω , 51 A, PowerFLAT™ 5x6
STripFET™ V Power MOSFET

Features

| Type | V _{DSS} | R _{DS(on) max} | I _D |
|-------------|------------------|-------------------------|---------------------|
| STL51N3LLH5 | 30 V | < 0.0145 Ω | 51 A ⁽¹⁾ |

1. The value is rated according R_{thj-pcb}

- R_{DS(on)} * Q_g industry benchmark
- Extremely low on-resistance R_{DS(on)}
- Very low switching gate charge
- High avalanche ruggedness
- Low gate drive power losses



Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using STMicroelectronics' STripFET™V technology. The device has been optimized to achieve very low on-state resistance, contributing to an FOM that is among the best in its class.

Figure 1. Internal schematic diagram

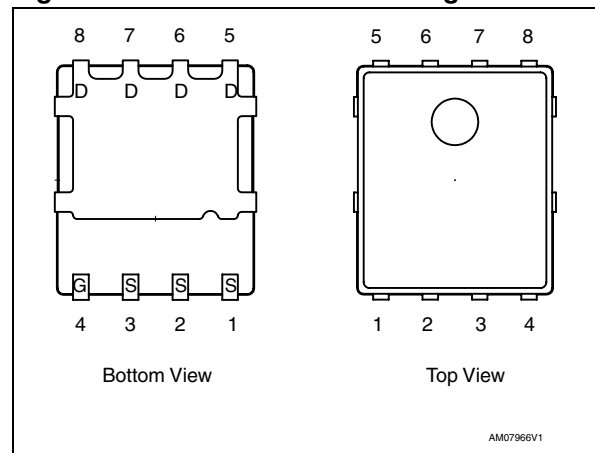


Table 1. Device summary

| Order code | Marking | Package | Packaging |
|-------------|----------|----------------|---------------|
| STL51N3LLH5 | 51N3LLH5 | PowerFLAT™ 5x6 | Tape and reel |

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1 Electrical ratings

Table 2. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|-----------------|---|--------------|---------------------|
| V_{DS} | Drain-source voltage ($V_{GS} = 0$) | 30 | V |
| V_{GS} | Gate-source voltage | $\pm 22/-22$ | V |
| $I_D^{(1)}$ | Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$ | 51 | A |
| $I_D^{(1)}$ | Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$ | 32.5 | A |
| $I_D^{(2)}$ | Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$ | 12.6 | A |
| $I_D^{(2)}$ | Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$ | 7.9 | A |
| $I_{DM}^{(3)}$ | Drain current (pulsed) | 50.4 | A |
| $P_{TOT}^{(1)}$ | Total dissipation at $T_C = 25\text{ }^\circ\text{C}$ | 62.5 | W |
| $P_{TOT}^{(2)}$ | Total dissipation at $T_C = 25\text{ }^\circ\text{C}$ | 4 | W |
| | Derating factor | 0.03 | W/ $^\circ\text{C}$ |
| T_J | Operating junction temperature | -55 to 150 | $^\circ\text{C}$ |
| T_{stg} | Storage temperature | | |

1. The value is rated according to R_{thj-c}
2. The value is rated according to $R_{thj-pcb}$
3. Pulse width limited by safe operating area

Table 3. Thermal resistance

| Symbol | Parameter | Value | Unit |
|---------------------|----------------------------------|-------|---------------------------|
| $R_{thj-case}$ | Thermal resistance junction-case | 2 | $^\circ\text{C}/\text{W}$ |
| $R_{thj-pcb}^{(1)}$ | Thermal resistance junction-pcb | 31.3 | $^\circ\text{C}/\text{W}$ |

1. When mounted on FR-4 board of 1inch², 2oz Cu, $t < 10$ sec

2 Electrical characteristics

($T_{CASE}=25\text{ °C}$ unless otherwise specified)

Table 4. On/off states

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------|--|---|------|------------------|------------------|--------------------------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage ($V_{GS}=0$) | $I_D = 250\ \mu\text{A}$ | 30 | | | V |
| I_{DSS} | Zero gate voltage drain current ($V_{GS}=0$) | $V_{DS} = 30\text{ V}$ $V_{DS} = 30\text{ V } T_C=125\text{ °C}$ | | | 1 10 | μA μA |
| I_{GSS} | Gate body leakage current ($V_{DS}=0$) | $V_{GS} = \pm 22/-20\text{ V}$ | | | ± 100 | nA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$ | 1 | | 2.5 | V |
| $R_{DS(on)}$ | Static drain-source on resistance | $V_{GS} = 10\text{ V}, I_D = 6.3\text{ A}$ $V_{GS} = 4.5\text{ V}, I_D = 6.3\text{ A}$ | | 0.0105 0.0145 | 0.0145 0.0175 | Ω Ω |

Table 5. Dynamic

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------|------------------------------|---|------|------|------|------|
| C_{iss} | Input capacitance | $V_{DS} = 25\text{ V}, f=1\text{ MHz},$ $V_{GS}=0$ | - | 724 | - | pF |
| C_{oss} | Output capacitance | | | 132 | | |
| C_{rss} | Reverse transfer capacitance | | | 20 | | |
| Q_g | Total gate charge | $V_{DD}=15\text{ V}, I_D = 12.6\text{ A}$ | - | 5 | - | nC |
| Q_{gs} | Gate-source charge | $V_{GS}=4.5\text{ V}$ | | 2 | | |
| Q_{gd} | Gate-drain charge | Figure 14 | | 2 | | |

Table 6. Switching times

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit | |
|--------------|---------------------|--|------|------|------|------|----|
| $t_{d(on)}$ | Turn-on delay time | $V_{DD}=15\text{ V}$, $I_D=6.3\text{ A}$, $R_G=4.7\ \Omega$, $V_{GS}=4.5\text{ V}$ <i>Figure 13</i> | | 4 | | ns | |
| t_r | Rise time | | | 4.2 | | ns | |
| $t_{d(off)}$ | Turn-off delay time | | | - | 2.1 | - | ns |
| t_f | Fall time | | | | 3.5 | | ns |

Table 7. Source drain diode

| Symbol | Parameter | Test conditions | Min | Typ. | Max | Unit | |
|-----------------|-------------------------------|--|-----|------|------|------|----|
| I_{SD} | Source-drain current | | - | | 12.6 | A | |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) | | - | | 50.4 | A | |
| $V_{SD}^{(2)}$ | Forward on voltage | $I_{SD} = 12.6\text{ A}$, $V_{GS}=0$ | - | | 1.1 | V | |
| t_{rr} | Reverse recovery time | $I_{SD} = 12.6\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD}=20\text{ V}$, $T_j=150\text{ }^\circ\text{C}$ | | 21 | | ns | |
| Q_{rr} | Reverse recovery charge | | | - | 10 | | nC |
| I_{RRM} | Reverse recovery current | | | | 1 | | A |

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

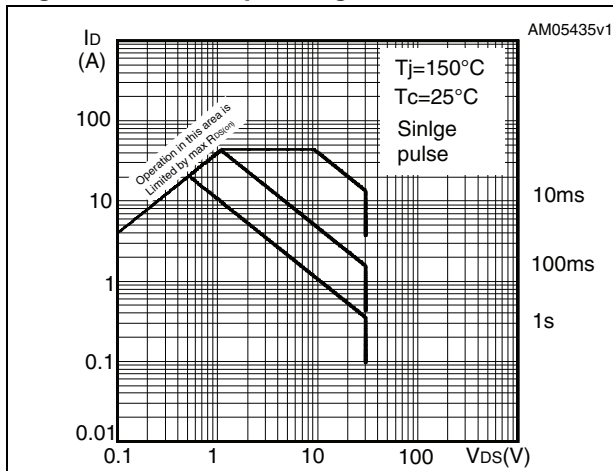


Figure 3. Thermal impedance

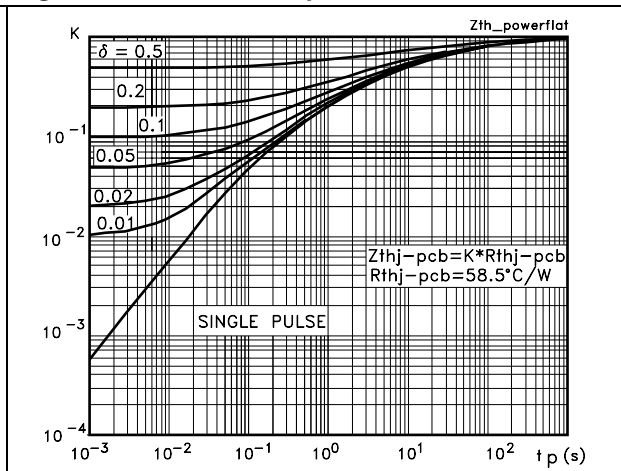


Figure 4. Output characteristics

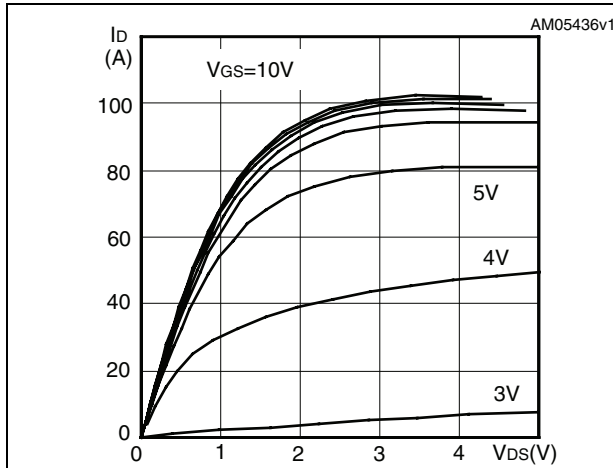


Figure 5. Transfer characteristics

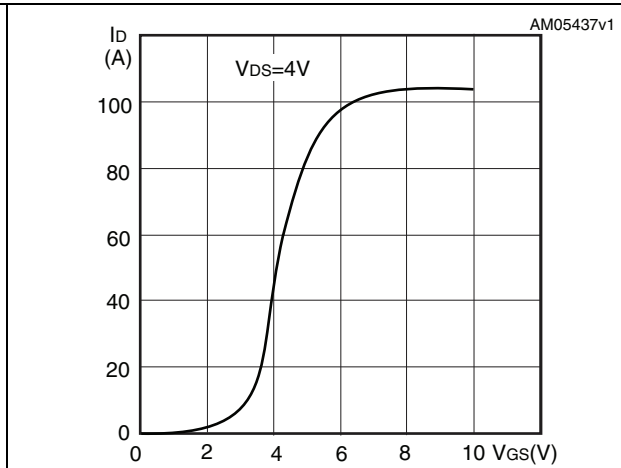


Figure 6. Normalized BV_{DSS} vs temperature

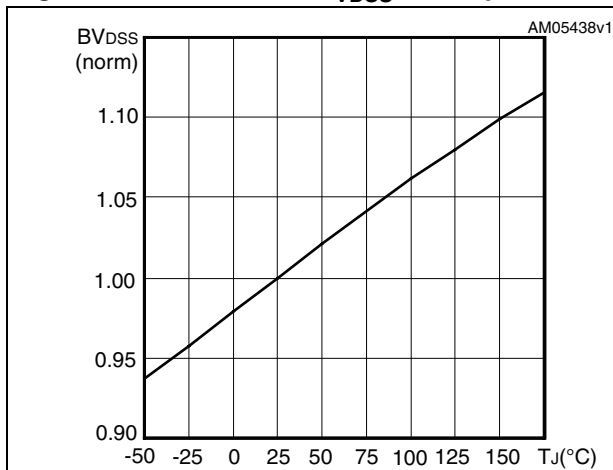


Figure 7. Static drain-source on resistance

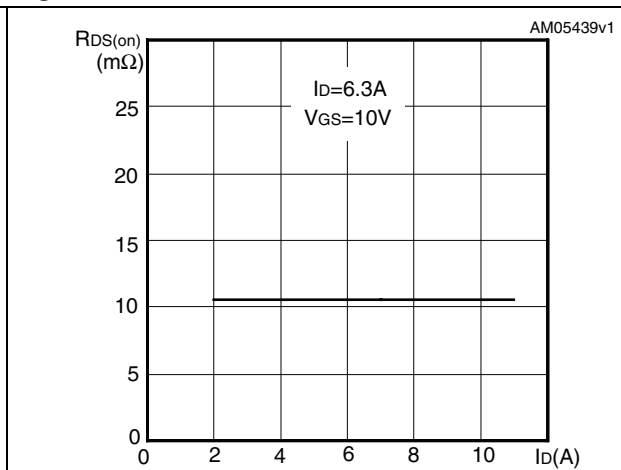


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

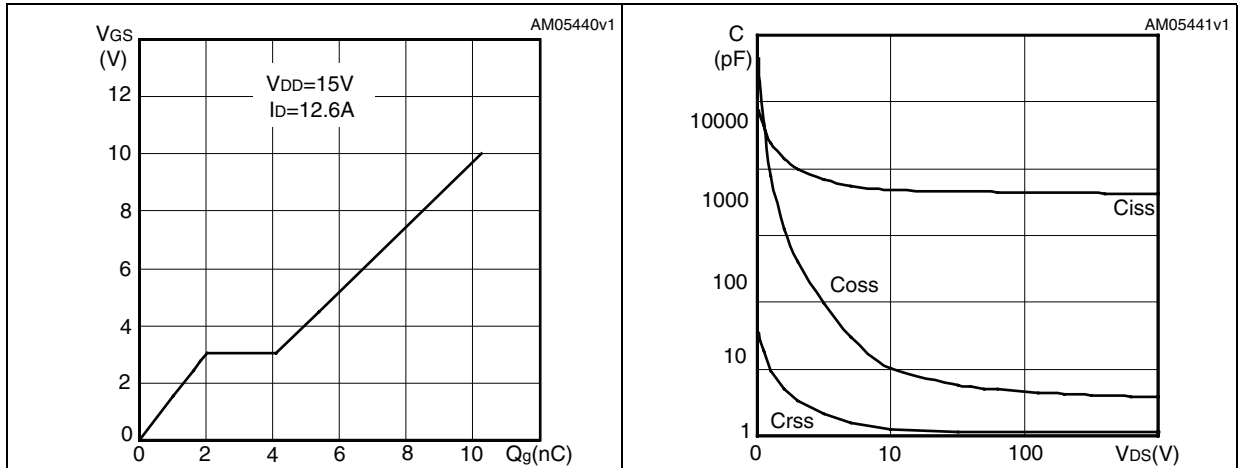


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on resistance vs temperature

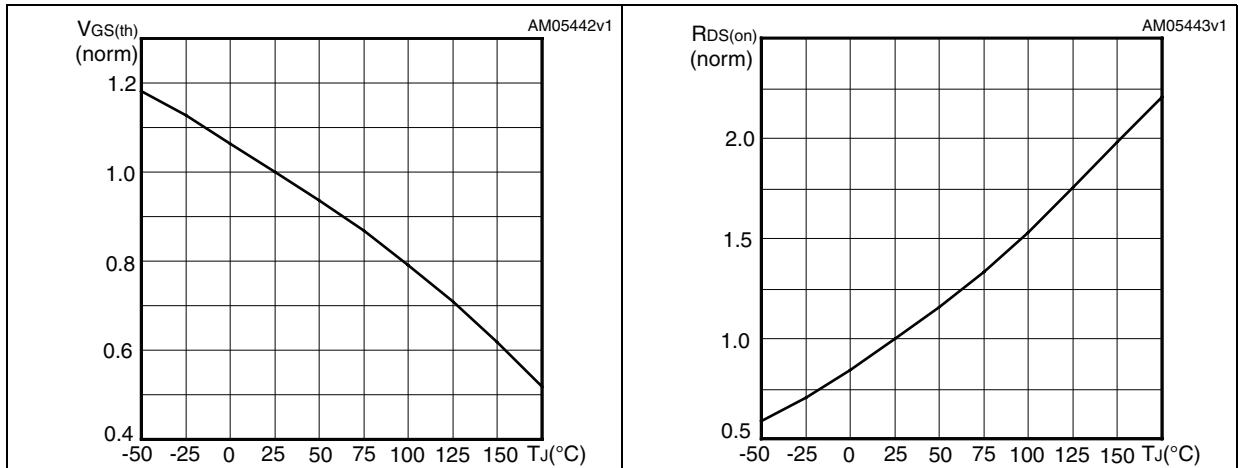
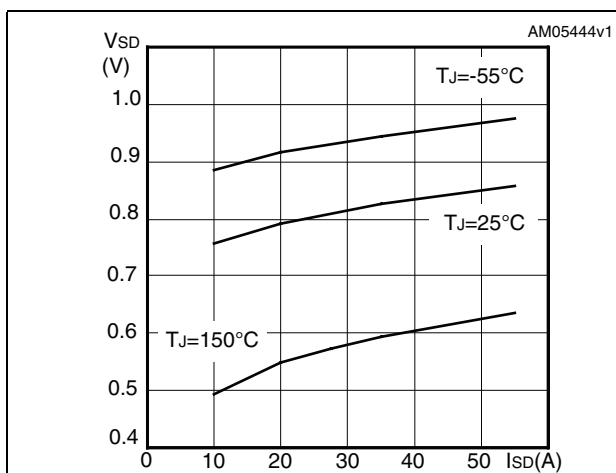


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

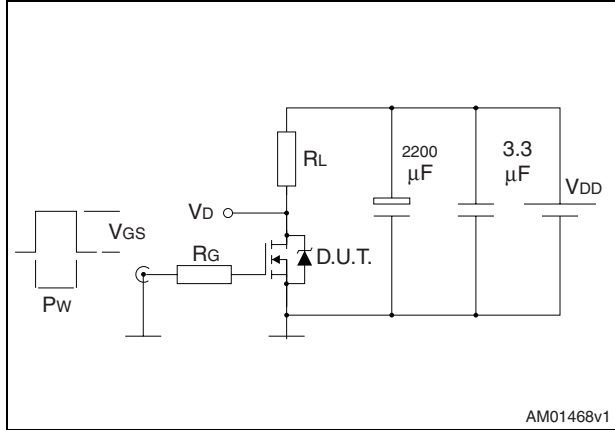


Figure 14. Gate charge test circuit

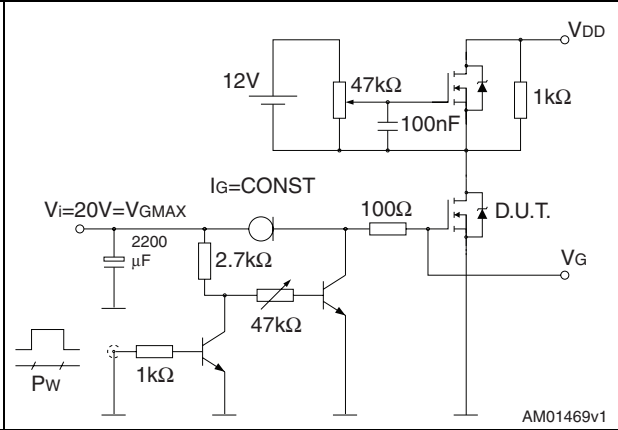


Figure 15. Test circuit for inductive load switching and diode recovery times

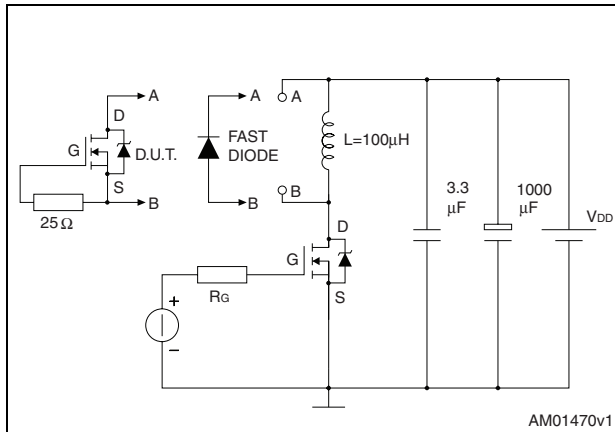


Figure 16. Unclamped inductive load test circuit

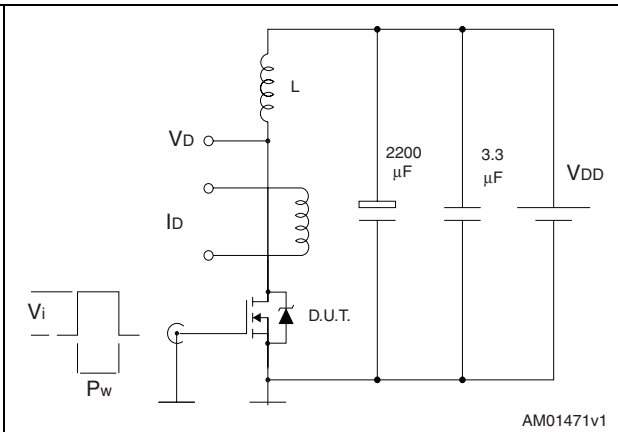


Figure 17. Unclamped inductive waveform

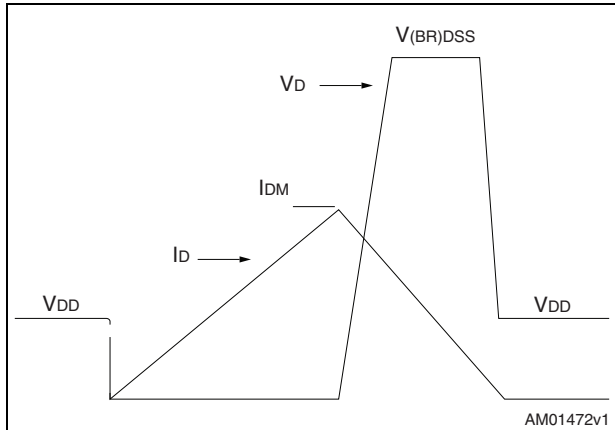
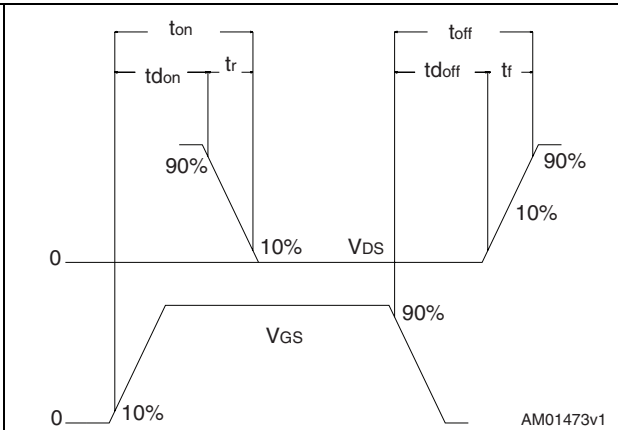


Figure 18. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 8. PowerFLAT 5x6 mechanical data

| Dim. | mm | | |
|------|-------|------|-------|
| | Min. | Typ. | Max. |
| A | 0.80 | | 1.00 |
| A1 | 0.02 | | 0.05 |
| A2 | | 0.25 | |
| b | 0.30 | | 0.50 |
| D | | 5.20 | |
| E | | 6.15 | |
| D2 | 4.11 | | 4.31 |
| E2 | 3.50 | | 3.70 |
| e | | 1.27 | |
| L | 0.50 | | 0.80 |
| K | 1.275 | | 1.575 |

Figure 19. PowerFLAT 5x6 drawing

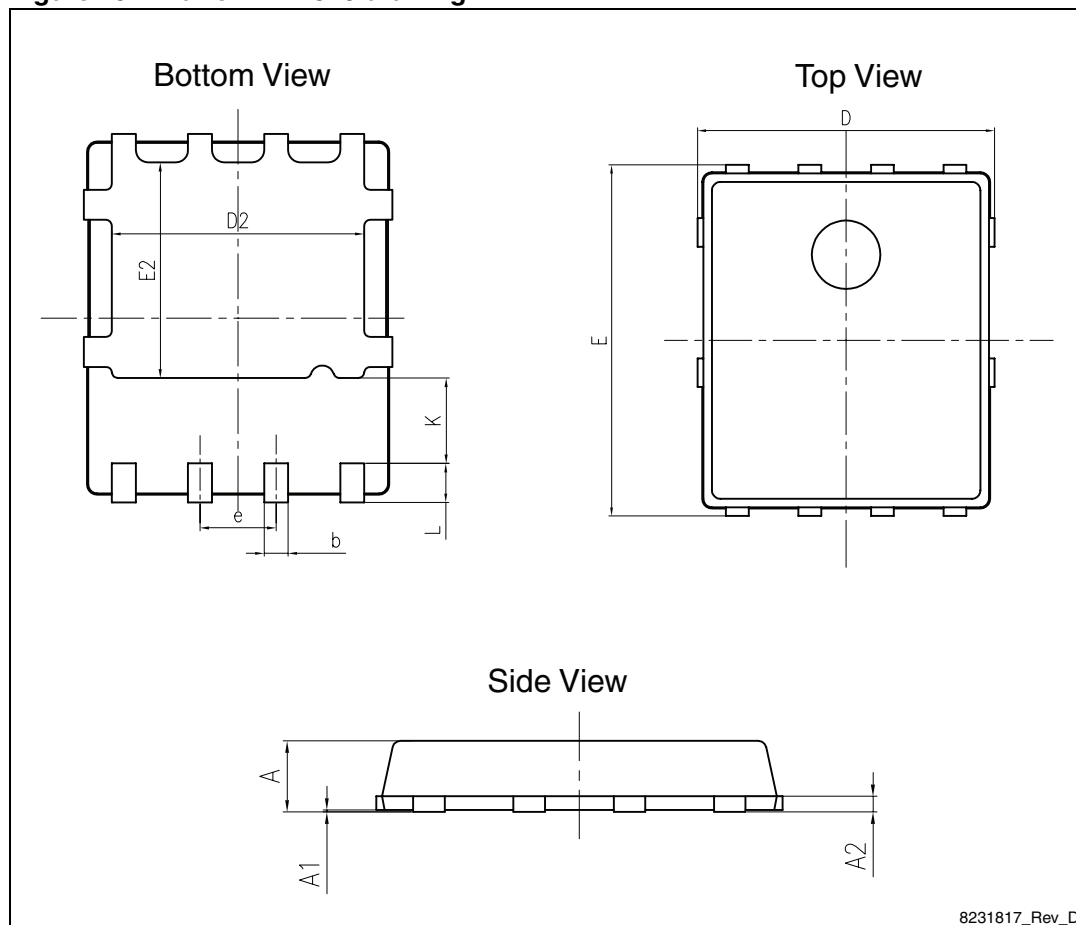
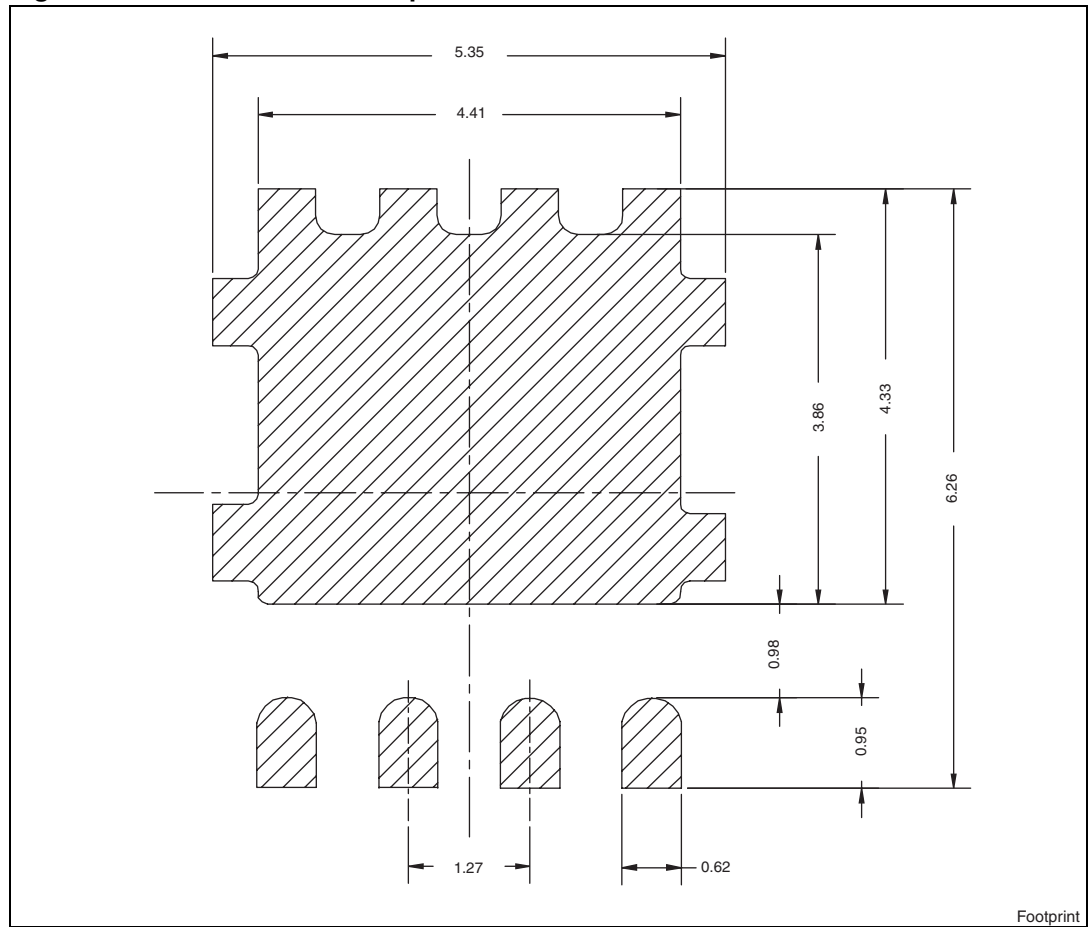


Figure 20. Recommended footprint



5 Revision history

Table 9. Document revision history

| Date | Revision | Changes |
|-------------|----------|---------------|
| 28-Jul-2011 | 1 | First release |

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