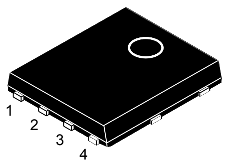
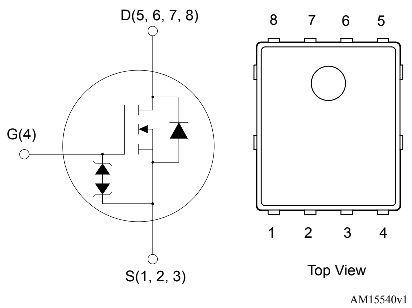
STL8N65M2

Datasheet

N-channel 650 V, 1 Ω typ., 4 A MDmesh M2 Power MOSFET in a PowerFLAT 5x6 HV package



PowerFLAT 5x6 HV



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STL8N65M2	650 V	1.25 Ω	4 A

- Extremely low gate charge
- Excellent output capacitance (C_{OSS}) profile
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using MDmesh M2 technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance and optimized switching characteristics, rendering it suitable for the most demanding high efficiency converters.

Product status link
STL8N65M2

Product summary	
Order code	STL8N65M2
Marking	8N65M2
Package	PowerFLAT 5x6 HV
Packing	Tape and reel

1 Electrical ratings

Table 1. **Absolute maximum ratings**

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±25	V
I_D	Drain current (continuous) at T_C = 25 °C	4	A
	Drain current (continuous) at T_C = 100 °C	2.6	A
I_{DM}	Drain current pulsed	16	A
P_{TOT}	Total power dissipation at T_C = 25 °C	48	W
I_{AR}	Avalanche current, repetitive or non-repetitive (pulse width limited by T_j max)	0.9	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	95	mJ
dv/dt (2)	Peak diode recovery voltage slope	15	V/ns
dv/dt (3)	MOSFET dv/dt ruggedness	50	
T_j	Operating junction temperature range	-55 to 150	°C
T_{stg}	Storage temperature range		

1. *Pulse width is limited by safe operating area.*
2. *I_{SD} ≤ 4 A, di/dt ≤ 400 A/μs; $V_{DS(peak)}$ < $V_{(BR)DSS}$, V_{DD} = 400 V*
3. *V_{DS} ≤ 480 V*

Table 2. **Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	2.6	°C/W
$R_{thj-pcb}$ (1)	Thermal resistance junction-pcb	59	°C/W

1. *When mounted on 1 inch² FR-4, 2 Oz copper board*

Table 3. **Thermal data**

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetetive or not repetetive (pulse width limited by T_{jmax})	0.5	°C/W
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}; V_{DD} = 50 V)	88	°C/W

2 Electrical characteristics

T_C = 25 °C unless otherwise specified

Table 4. On/off-state

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	650			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 650 V			1	µA
		V_{GS} = 0 V, V_{DS} = 650 V T_C = 125 °C (1)			100	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 2 A		1	1.25	Ω

1. *Defined by design, not subject to production test.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	270	-	pF
C_{oss}	Output capacitance		-	14.5	-	pF
C_{rss}	Reverse transfer capacitance		-	0.8	-	pF
$C_{oss\ eq.}$ (1)	Equivalent capacitance energy related	V_{DS} = 0 to 520 V, V_{GS} = 0 V	-	108	-	pF
R_g	Intrinsic gate resistance	f = 1 MHz open drain	-	7	-	Ω
Q_g	Total gate charge	V_{DD} = 520 V, I_D = 5 A V_{GS} = 0 to 10 V (see Figure 14. Test circuit for gate charge behavior)	-	9	-	nC
Q_{gs}	Gate-source charge		-	2.3	-	nC
Q_{gd}	Gate-drain charge		-	4.3	-	nC

1. *$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DS}.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 325 V, I_D = 2.5 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	7.7	-	ns
t_r	Rise time		-	20	-	ns
$t_{d(off)}$	Turn-off delay time		-	19.5	-	ns
t_f	Fall time		-	30	-	ns

Table 7. **Source-drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		4	A
I_{SDM} [1]	Source-drain current (pulsed)		-		16	A
V_{SD} [2]	Forward on voltage	I_{SD} = 4 A, V_{GS} = 0 V	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 5 A, di/dt = 100 A/µs, V_{DD} = 60 V (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	275		ns
Q_{rr}	Reverse recovery charge		-	1.62		µC
I_{RRM}	Reverse recovery current		-	11.8		A
t_{rr}	Reverse recovery time	I_{SD} = 5 A, di/dt = 100 A/µs, V_{DD} = 60 V, T_j = 150 °C (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	430		ns
Q_{rr}	Reverse recovery charge		-	2.54		µC
I_{RRM}	Reverse recovery current		-	11.9		A

1. *Pulse width is limited by safe operating area*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%*

2.1 Electrical characteristics curves

Figure 1. Safe operating area

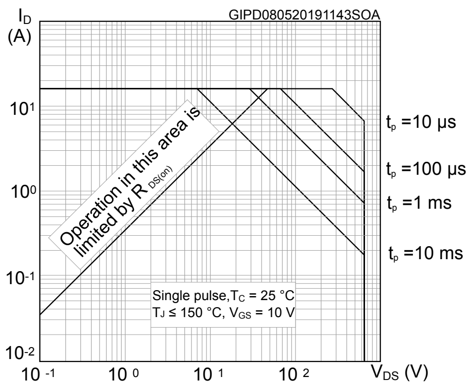


Figure 2. Thermal impedance

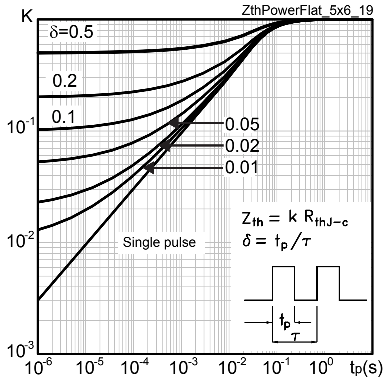


Figure 3. Output characteristics

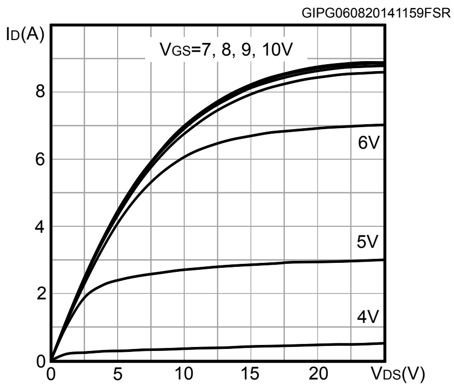


Figure 4. Transfer characteristics

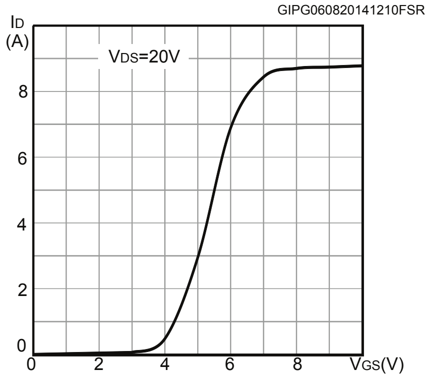


Figure 5. Normalized $V_{(BR)DSS}$ vs temperature

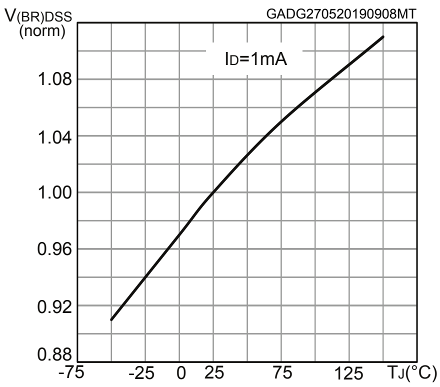


Figure 6. Source-drain diode forward characteristics

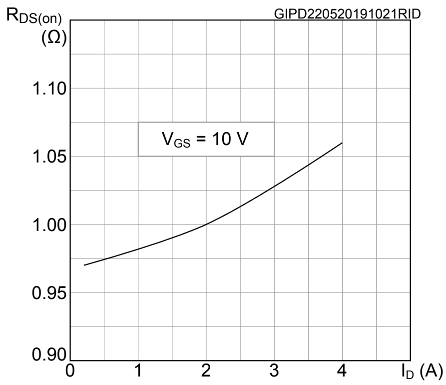


Figure 7. Gate charge vs gate-source voltage

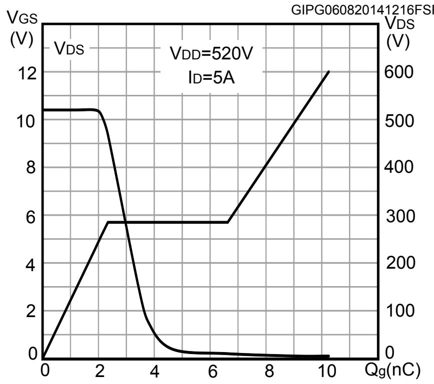


Figure 8. Capacitance variations

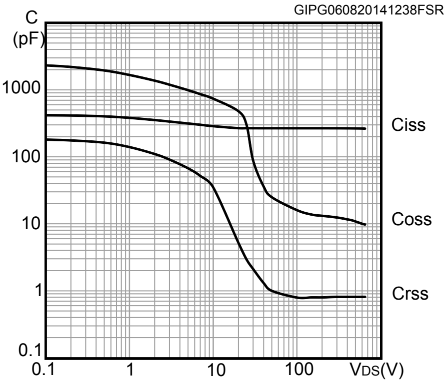


Figure 9. Normalized gate threshold voltage vs temperature

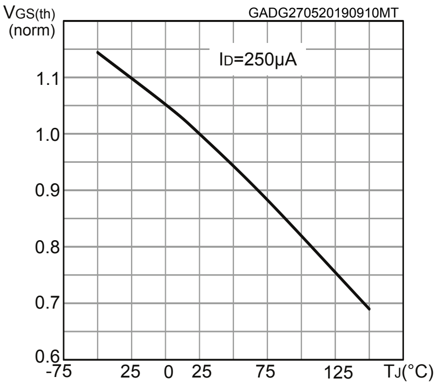


Figure 10. Normalized on-resistance vs temperature

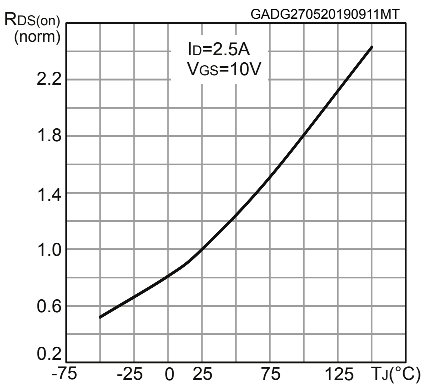


Figure 11. Source-drain diode forward characteristics

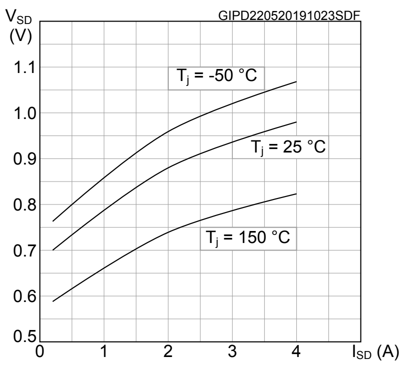
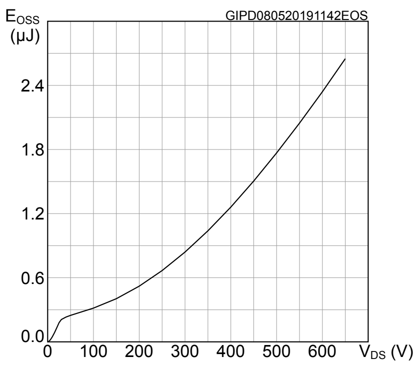


Figure 12. Output capacitance stored energy



3 Test circuits

Figure 13. Test circuit for resistive load switching times

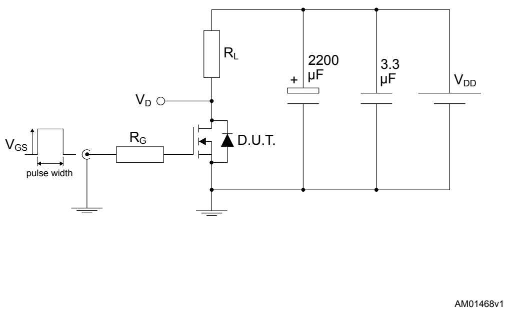


Figure 14. Test circuit for gate charge behavior

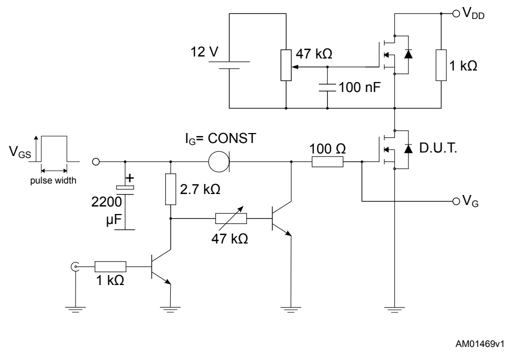


Figure 15. Test circuit for inductive load switching and diode recovery times

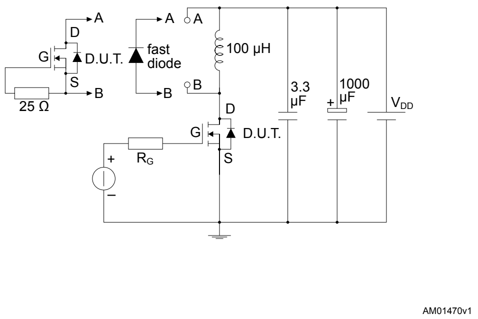


Figure 16. Unclamped inductive load test circuit

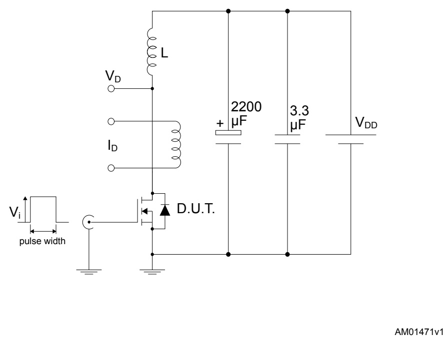


Figure 17. Unclamped inductive waveform

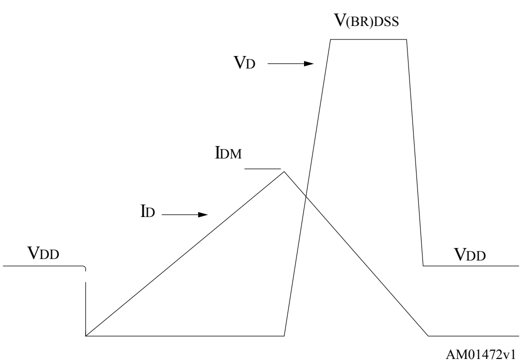
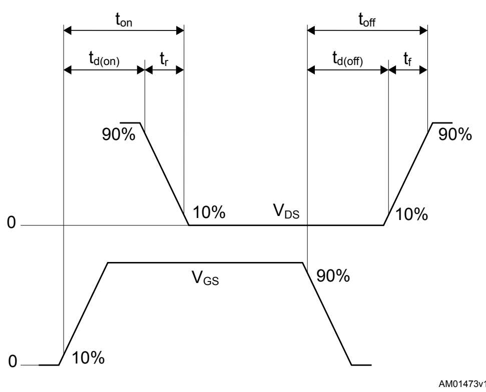


Figure 18. Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 PowerFLAT 5x6 HV package information

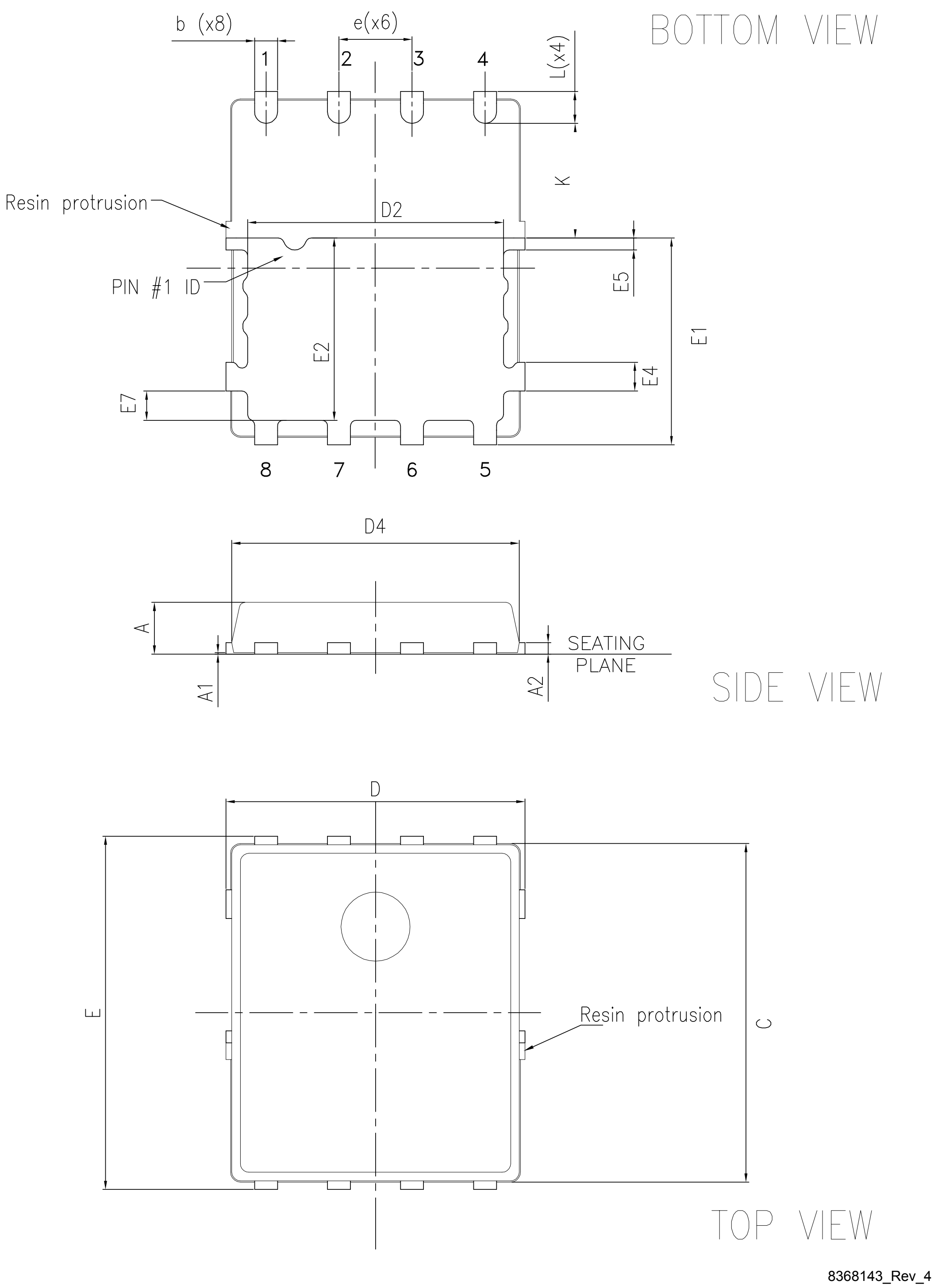
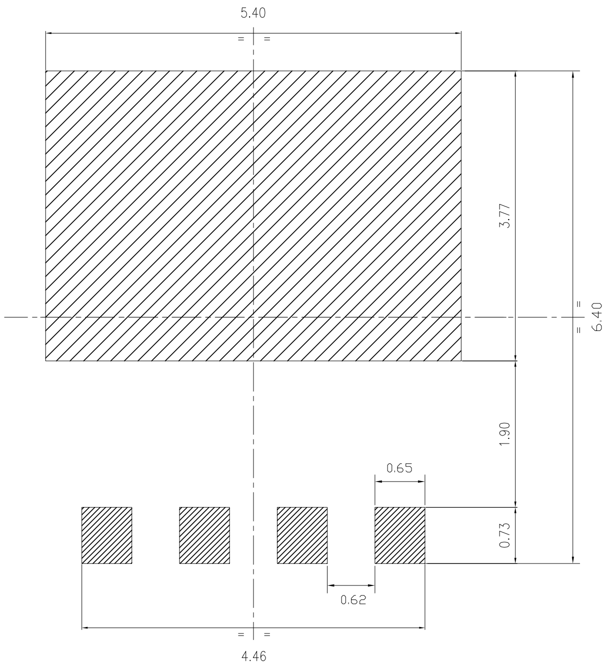


Figure 19. PowerFLAT 5x6 HV package outline

Table 8. PowerFLAT 5x6 HV mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.60	5.80	6.00
D	5.10	5.20	5.30
D2	4.30	4.40	4.50
D4	4.60	4.80	5.00
E	6.05	6.15	6.25
E1	3.50	3.60	3.70
E2	3.10	3.20	3.30
E4	0.40	0.50	0.60
E5	0.10	0.20	0.30
E7	0.40	0.50	0.60
e		1.27	
L	0.50	0.55	0.60
K	1.90	2.00	2.10

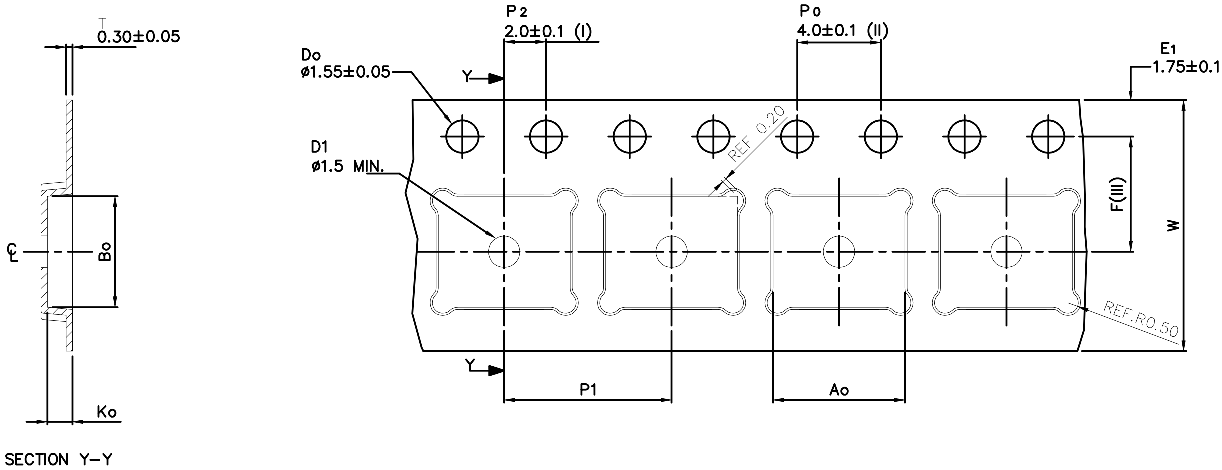
Figure 20. PowerFLAT™ 5x6 HV recommended footprint (dimensions are in mm)



8368143_Rev_4_footprint

4.2 PowerFLAT 5x6 packing information

Figure 21. PowerFLAT 5x6 tape (dimensions are in mm)



Ao	6.30 +/− 0.1
Bo	5.30 +/− 0.1
Ko	1.20 +/− 0.1
F	5.50 +/− 0.1
P1	8.00 +/− 0.1
W	12.00 +/− 0.3

(I) Measured from centreline of sprocket hole to centreline of pocket.

(II) Cumulative tolerance of 10 sprocket holes is ±0.20.

(III) Measured from centreline of sprocket hole to centreline of pocket

Base and bulk quantity 3000 pcs
All dimensions are in millimeters

8234350_Tape_rev_C

Figure 22. PowerFLAT 5x6 package orientation in carrier tape

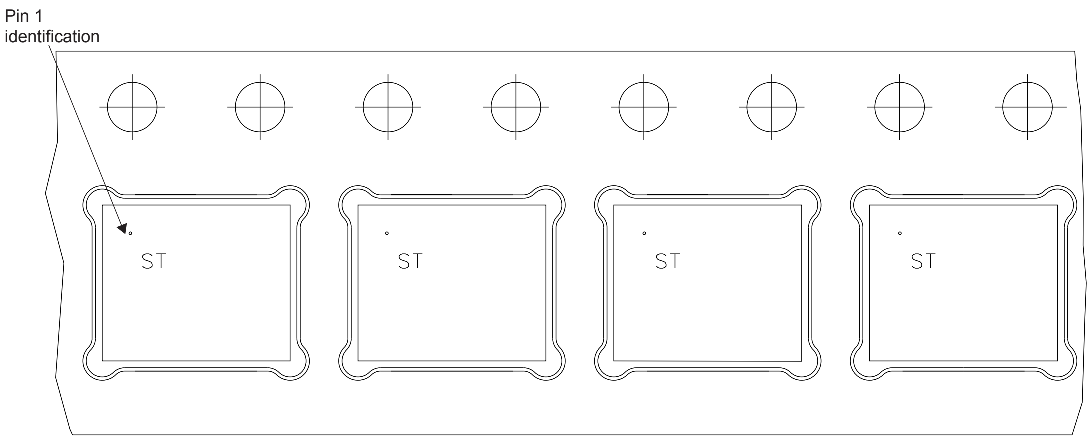
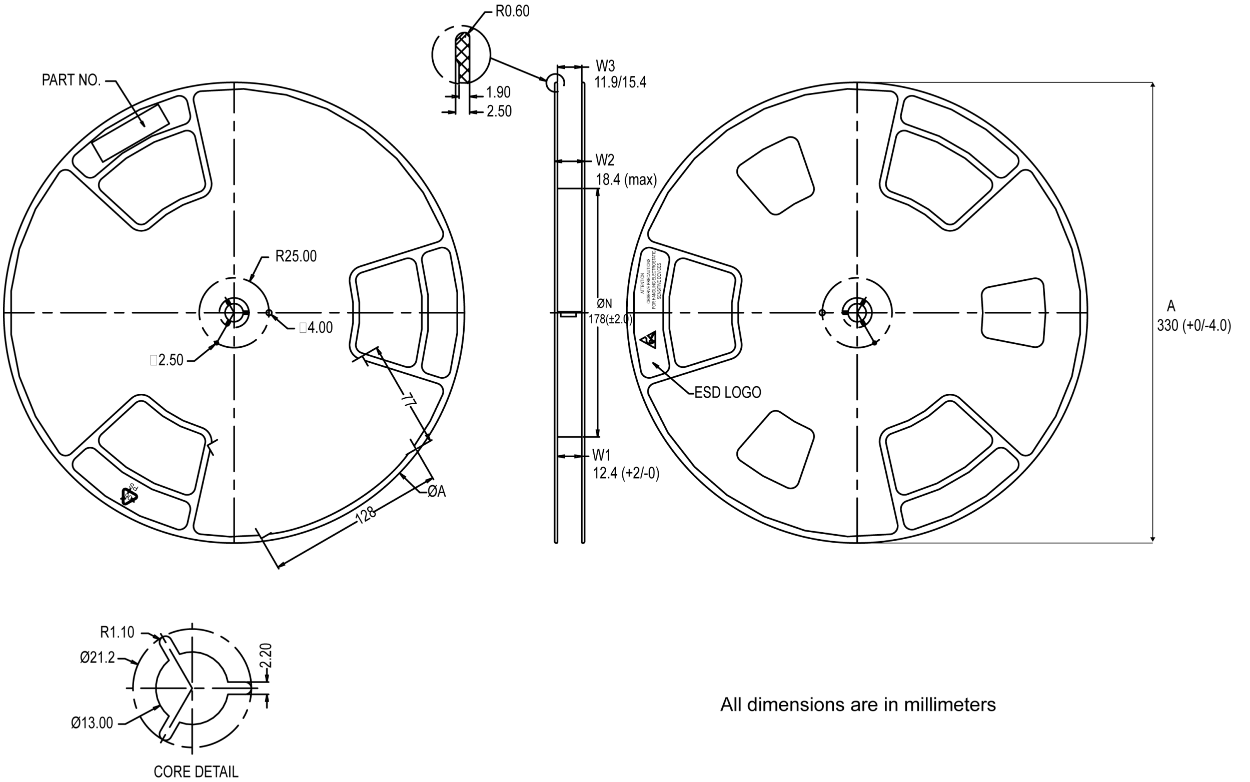


Figure 23. PowerFLAT 5x6 reel



8234350_Reel_rev_C

Revision history

Table 9. **Document revision history**

Date	Revision	Changes
30-May-2019	1	First release

Contents