

STL8N6LF6AG

Automotive-grade N-channel 60 V, 21 mΩ typ., 32 A STripFET™ F6 Power MOSFET in a PowerFLAT™ 5x6 package

Datasheet - production data

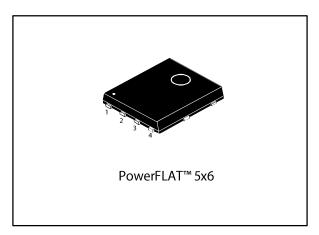
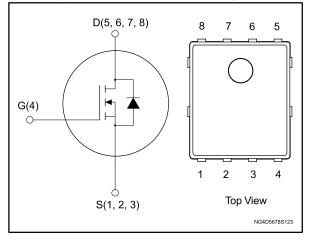


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	ΙD	Ртот
STL8N6LF6AG	60 V	27 mΩ	32 A	55 W

- Designed for automotive applications and AEC-Q101 qualified
- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss
- Wettable flank package

Applications

Switching applications

Description

This device is an N-channel Power MOSFET developed using the STripFET $^{\text{TM}}$ F6 technology with a new trench gate structure. The resulting Power MOSFET exhibits very low $R_{\text{DS(on)}}$ in all packages.

Table 1: Device summary

Order code	Marking	Package	Packing
STL8N6LF6AG	8N6LF6	PowerFLAT™ 5x6	Tape and reel

Contents STL8N6LF6AG

Contents

1	Electric	al ratings	3
2	Electric	al characteristics	4
	2.1	Electrical characteristics (curves)	5
3	Test cir	cuits	7
4	Packag	e information	8
	4.1	PowerFLAT™ 5x6 WF type R package information	8
	4.2	PowerFLAT™ 5x6 WF packing information	11
5	Revisio	n history	13

STL8N6LF6AG Electrical ratings

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit	
V _{DS}	Drain-source voltage	60	V	
V_{GS}	Gate-source voltage	±20	V	
1-	Drain current (continuous) at T _{case} = 25 °C	32	Α	
l _D	Drain current (continuous) at T _{case} = 100 °C	23	A	
I _D ⁽¹⁾	Drain current (continuous) at T _{pcb} = 25 °C		Α	
ID ^(*)	Drain current (continuous) at T _{pcb} = 100 °C		A	
I _{DM} ⁽¹⁾⁽²⁾	Drain current (pulsed)	38	Α	
I _{DM} ⁽²⁾	Drain current (pulsed)	128	Α	
Ртот	Total dissipation at T _{case} = 25 °C	55	W	
Ртот	Total dissipation at T _{pcb} = 25 °C	4.8	VV	
T_{stg}	Storage temperature	-55 to 175	°C	
Tj	Operating junction temperature	-55 (0 175	C	

Notes:

Table 3: Thermal data

Symbol	Parameter	Value	Unit
R _{thj-case}	Thermal resistance junction-case	2.7	°C/W
R _{thj-pcb} ⁽¹⁾	Thermal resistance junction-pcb	31.3	C/VV

Notes:

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
lav	Avalanche current, not repetitive	32	Α
E _{AS} ⁽¹⁾	Single pulse avalanche energy	120	mJ

Notes:

 $^{(1)}$ starting T_j = 25 °C, I_D = $I_{AV},\,V_{DD}$ = 43.5 V.

 $^{^{(1)}}$ When mounted on a 1-inch² FR-4, 2 Oz copper board, t < 10 s.

⁽²⁾ Pulse width is limited by safe operating area.

 $^{^{(1)}}$ When mounted on a 1-inch² FR-4, 2 Oz copper board, t < 10 s.

Electrical characteristics STL8N6LF6AG

2 Electrical characteristics

(T_{case} = 25 °C unless otherwise specified)

Table 5: Static

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	$V_{GS} = 0 \text{ V}, I_{D} = 250 \mu\text{A}$	60			V
IDSS	Zero gate voltage drain current	V _{GS} = 0 V, V _{DS} = 60 V			1	μΑ
I _{GSS}	Gate-body leakage current	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			±100	nA
V _{GS(th)}	Gate threshold voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	1		2.5	V
Б	Static duals assures as registers	V _{GS} = 10 V, I _D = 9.6 A		21	27	C
R _{DS(on)}	Static drain-source on-resistance	$V_{GS} = 4.5 \text{ V}, I_D = 9.6 \text{ A}$		25	31	mΩ

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
C _{iss}	Input capacitance		ı	1340	1	
Coss	Output capacitance VDS = 25 V, f = 1 MHz, VGS = 0 V		-	90	-	pF
Crss	Reverse transfer capacitance	V65 - V	ı	60	1	
Qg	Total gate charge $V_{DD} = 30 \text{ V}, I_D = 9.6 \text{ A},$		ı	27	1	
Q_{gs}	Gate-source charge	V _{GS} = 10 V (see Figure 14: "Test circuit for gate charge	-	4.6	-	nC
Q _{gd}	Gate-drain charge	behavior")	-	4.3	-	

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t _{d(on)}	Turn-on delay time	$V_{DD} = 30 \text{ V}, I_D = 12.5 \text{ A R}_G = 4.7 \Omega,$	ı	9.6	ı	
t _r	Rise time	V _{GS} = 10 V (see Figure 13: "Test circuit for resistive load switching	1	20	-	
t _{d(off)}	Turn-off delay time	times" and Figure 18: "Switching	-	56	-	ns
t _f	Fall time	time waveform")	1	7	-	

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I _{SD}	Source-drain current		-		9.6	Α
I _{SDM} ⁽¹⁾	Source-drain current (pulsed)		-		38	Α
V _{SD} ⁽²⁾	Forward on voltage $V_{GS} = 0 \text{ V}, I_{SD} = 9.6 \text{ A}$ -			1.3	V	
t _{rr}	Reverse recovery time	$I_{SD} = 25 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s},$	-	22.5		ns
Qrr	Reverse recovery charge	V _{DD} = 48 V (see Figure 15: "Test circuit for inductive	-	22.2		nC
I _{RRM}	"I est circuit to		-	2.0		Α

Notes:

⁽¹⁾ Pulse width is limited by safe operating area.

 $^{^{(2)}}$ Pulse test: pulse duration = 300 $\mu s,$ duty cycle 1.5%.

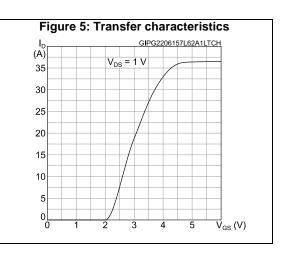
2.1 Electrical characteristics (curves)

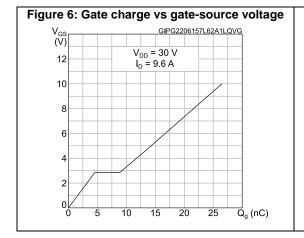
Figure 2: Safe operating area GIPD041120151150SQA (A) Operation in this area is limited by $R_{DS(on)}$ t_p = $10\mu s$ t_p = $100\mu s$ t_p = $100\mu s$ t_p = 100m s t_p

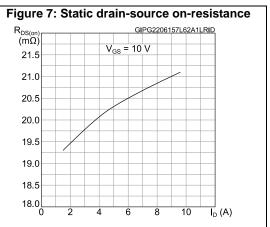
10⁻¹

10

Figure 3: Thermal impedance GIPD041120151150ZTH δ=0.5 0.2 0.1 10 0.05 0.02 $Z_{th}=k^*R_{thj-c}$ $\delta=tp/T$ Single pulse $-t_{p}T$ 10⁻² 10-4 10⁻² t_p (s) 10⁻⁵ 10-3

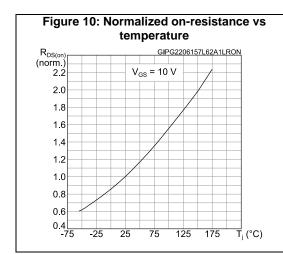


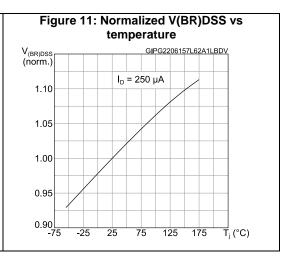


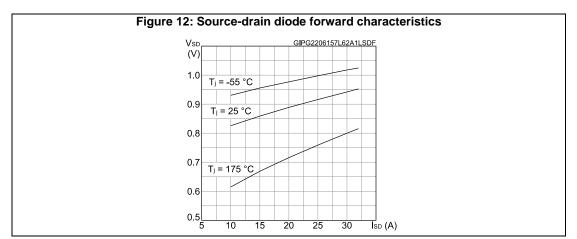


Ü_{DS} (V)

Figure 9: Normalized gate threshold voltage vs temperature V_{GS(th)} (norm.) GIPG2206157L62A1LVTH I_D = 250 μA 1.2 1.0 0.8 0.6 0.4 -75 -25 25 75 125 175 T_i (°C)







STL8N6LF6AG Test circuits

3 Test circuits

Figure 13: Test circuit for resistive load switching times

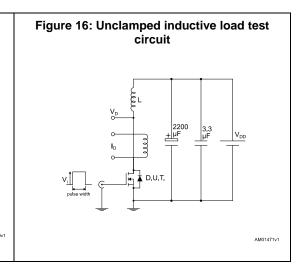
Figure 14: Test circuit for gate charge behavior

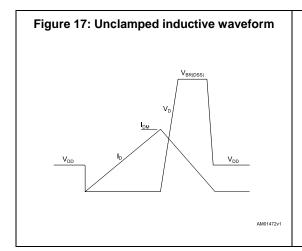
12 V 47 kΩ 100 nF D.U.T.

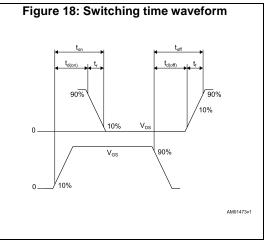
2200 V_G 47 kΩ 0 V_G

AM01489v1

Figure 15: Test circuit for inductive load switching and diode recovery times







4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: **www.st.com**. ECOPACK® is an ST trademark.

4.1 PowerFLAT™ 5x6 WF type R package information

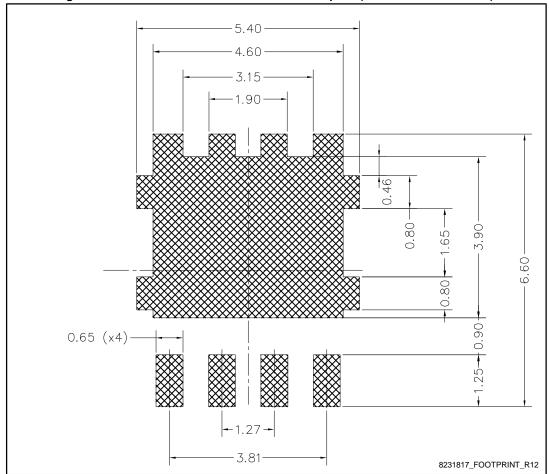
BOTTOM VIEW D3 5 8 6 E7Detail A Scale 3:1 0.08 E3 £2, L(x4) e(x6) b(x8) D5(x4) SIDE VIEW A Detail A ŏ TOP A0Y5_8231817_R_WF_Rev_12

Figure 19: PowerFLAT™ 5x6 WF type R package outline

Table 9: PowerFLAT™ 5x6 WF type R mechanical data

		mm	
Dim.	Min.	Тур.	Max.
А	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
С	5.80	6.00	6.20
D	5.00	5.20	5.40
D2	4.15		4.45
D3	4.05	4.20	4.35
D4	4.80	5.0	5.20
D5	0.25	0.4	0.55
D6	0.15	0.3	0.45
е		1.27	
E	6.20	6.40	6.60
E2	3.50		3.70
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28
E6	0.175	0.325	0.450
E7	0.85	1.00	1.15
К	1.275		1.575
L	0.725	0.825	0.925
L1	0.175	0.275	0.375
θ	0°		12°





STL8N6LF6AG Package information

4.2 PowerFLAT™ 5x6 WF packing information

Figure 21: PowerFLAT™ 5x6 WF tape

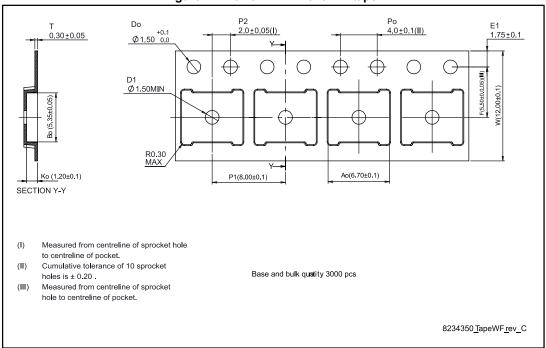
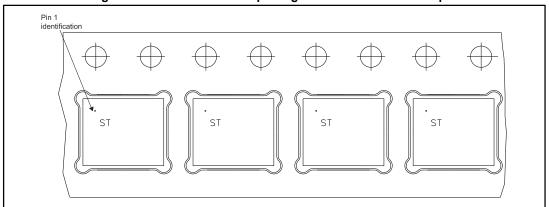


Figure 22: PowerFLAT™ 5x6 package orientation in carrier tape



R1.10
R1.10
R1.10
R1.10
R1.10
R25.00
R1.10

STL8N6LF6AG Revision history

5 Revision history

Table 10: Document revision history

Date	Revision	Changes
06-Jul-2015	1	First release.
07-Jan-2016	2	Updated title and features in cover page. Updated Section 1: "Electrical ratings", Section 2: "Electrical characteristics" and Section 4.1: "PowerFLAT™ 5x6 WF type R package information".

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