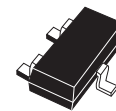




### Features

- Precision monitoring of 3 V, 3.3 V, and 5 V supply voltages
- Open drain  $\overline{\text{RST}}$  output
- 30 ms or 140 ms reset pulse width (min)
- Low supply current - 6  $\mu\text{A}$  (typ)
- Guaranteed  $\overline{\text{RST}}$  assertion down to  $V_{\text{CC}} = 1.0 \text{ V}$
- Operating temperature:
  - $-40 \text{ }^\circ\text{C}$  to  $85 \text{ }^\circ\text{C}$  (industrial grade)
- Lead-free, small SOT23 package



SOT23-3 (WX)

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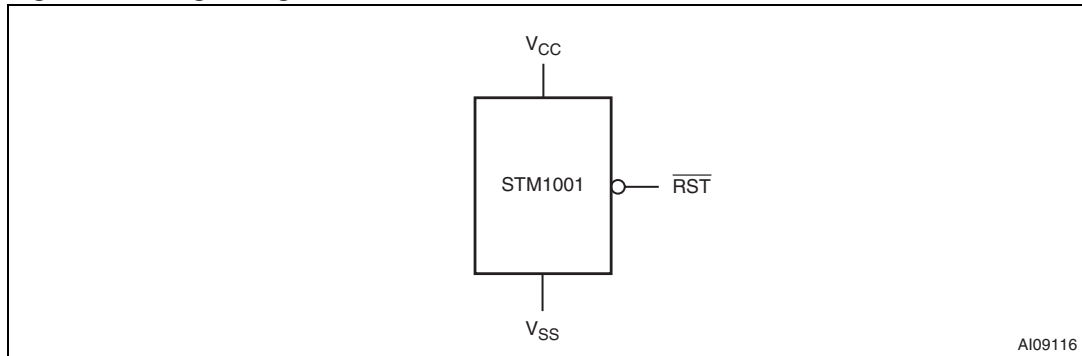
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# 1 Description

The STM1001 microprocessor reset circuit is a low-power supervisory device used to monitor power supplies. It performs a single function: asserting a reset signal whenever the  $V_{CC}$  supply voltage drops below a preset value and keeping it asserted until  $V_{CC}$  has risen above the preset threshold for a minimum period of time ( $t_{rec}$ ).

**Figure 1. Logic diagram**

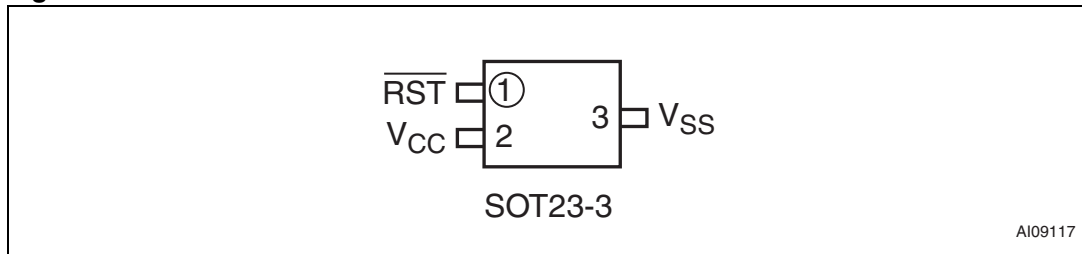


AI09116

**Table 1. Signal names**

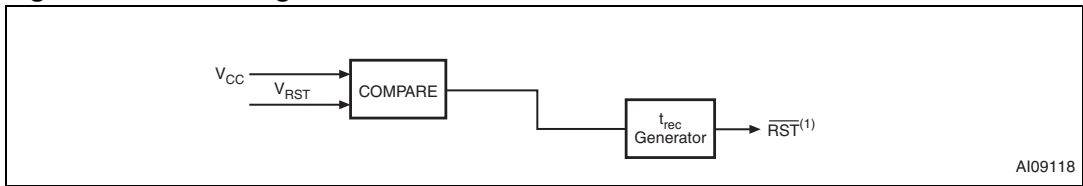
$V_{SS}$	Ground
RST	Active-low reset output (open drain)
$V_{CC}$	Supply voltage

**Figure 2. Connections**



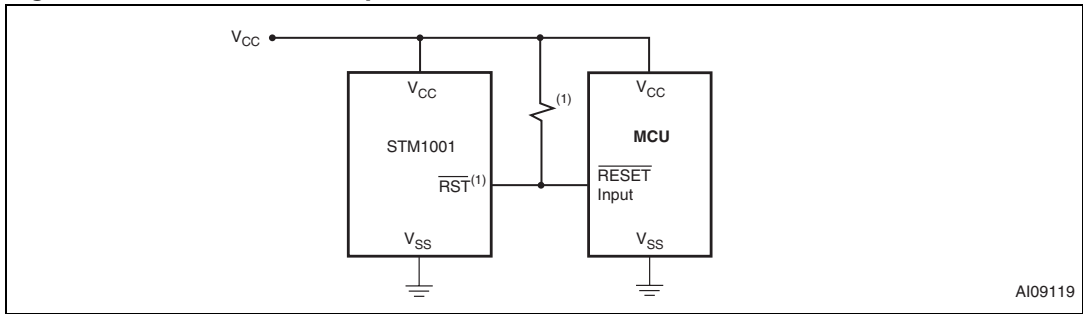
AI09117

Figure 3. Block diagram



- 1. Open drain

Figure 4. Hardware hookup



- 1.  $\overline{RST}^{(1)}$  output requires pull-up resistor.

## 2 Operation

### 2.1 Reset output

The STM1001 microprocessor reset circuit asserts a reset signal to the MCU whenever  $V_{CC}$  goes below the reset threshold ( $V_{RST}$ ).  $\overline{RST}$  is guaranteed valid down to  $V_{CC} = 1\text{ V}$  ( $0^\circ$  to  $70^\circ\text{C}$ ).

During power-up, once  $V_{CC}$  exceeds the reset threshold an internal timer keeps  $\overline{RST}$  low for the reset time-out period,  $t_{rec}$ . After this interval,  $\overline{RST}$  returns high.

If  $V_{CC}$  drops below the reset threshold,  $\overline{RST}$  goes low. Each time  $\overline{RST}$  is asserted, it stays low for at least the reset time-out period. Any time  $V_{CC}$  goes below the reset threshold, the internal timer clears. The reset timer starts when  $V_{CC}$  returns above the reset threshold. The active-low reset ( $\overline{RST}$ ) is an open drain output.

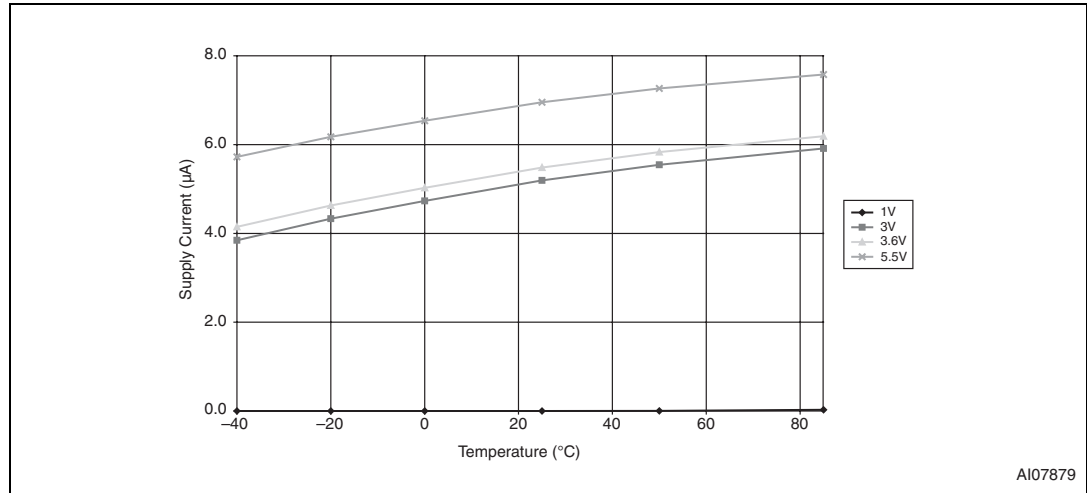
### 2.2 Negative-going $V_{CC}$ transients

The STM1001 is relatively immune to negative-going  $V_{CC}$  transients (glitches). [Figure 10 on page 10](#) shows typical transient duration versus reset comparator overdrive (for which the STM1001 will NOT generate a reset pulse). The graph was generated using a negative pulse applied to  $V_{CC}$ , starting at 0.5 V above the actual reset threshold and ending below it by the magnitude indicated (comparator overdrive). The graph indicates the maximum pulse width a negative  $V_{CC}$  transient can have without causing a reset pulse. As the magnitude of the transient increases (further below the threshold), the maximum allowable pulse width decreases. Any combination of duration and overdrive which lies under the curve will NOT generate a reset signal. Typically, a  $V_{CC}$  transient that goes 100 mV below the reset threshold and lasts 20  $\mu\text{s}$  or less will not cause a reset pulse. A 0.1  $\mu\text{F}$  bypass capacitor mounted as close as possible to the  $V_{CC}$  pin provides additional transient immunity.

### 3 Typical operating characteristics

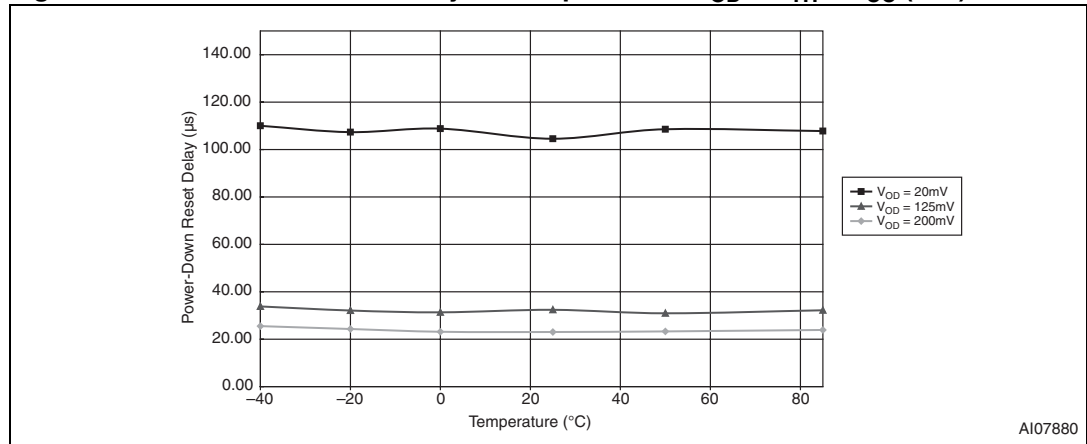
Note: Typical values are at  $T_A = 25\text{ }^\circ\text{C}$ ,  $V_{CC} = 5\text{ V}$  for L/M versions,  $V_{CC} = 3.3\text{ V}$  for T/S versions, and  $V_{CC} = 3.0\text{ V}$  for R versions.

Figure 5. Supply current vs. temperature, L/M/R/S/T (no load)



AI07879

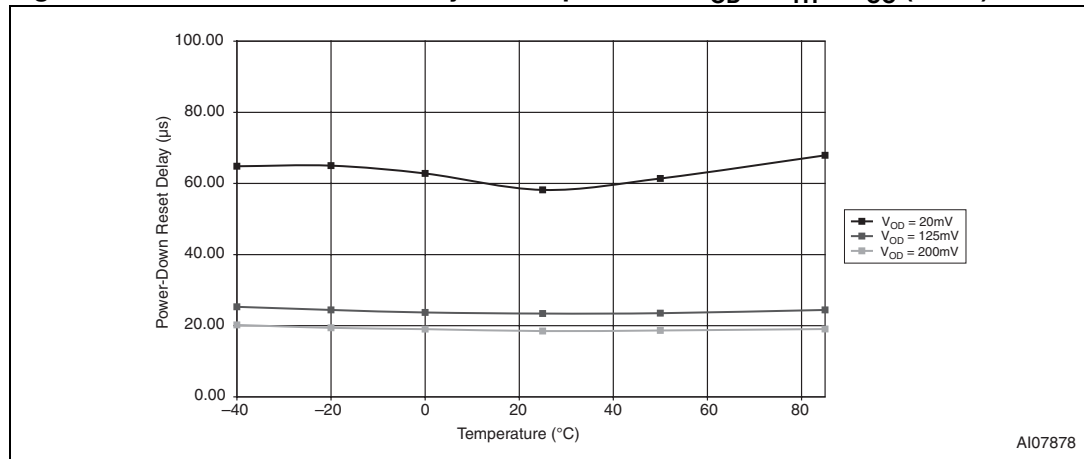
Figure 6. Power-down reset delay vs. temperature -  $V_{OD} = V_{TH} - V_{CC}$  (L/M)



AI07880

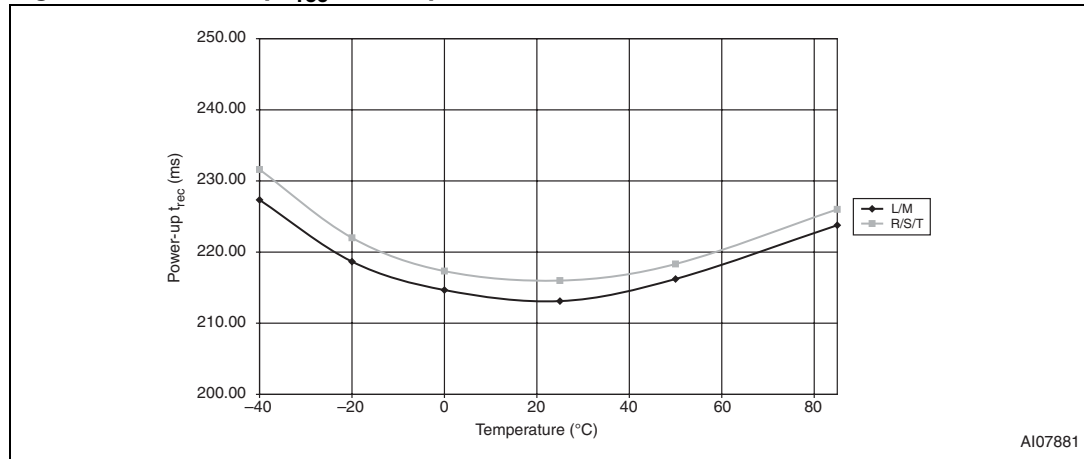


Figure 7. Power-down reset delay vs. temperature -  $V_{OD} = V_{TH} - V_{CC}$  (R/S/T)



AI07878

Figure 8. Power-up  $t_{rec}$  vs. temperature



AI07881

Note: Valid for  $t_{rec} = 210\text{ ms}$  (typ).

Figure 9. Normalized reset threshold vs. temperature

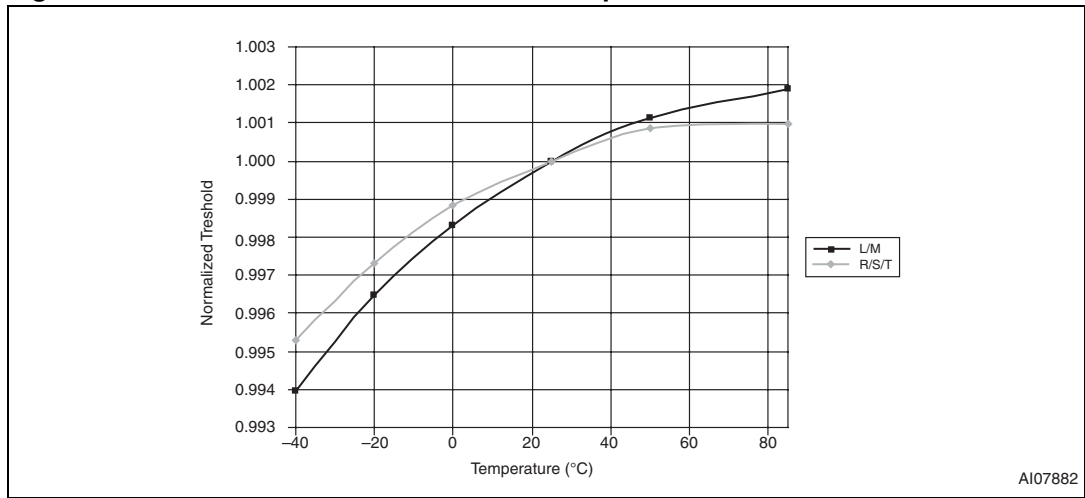
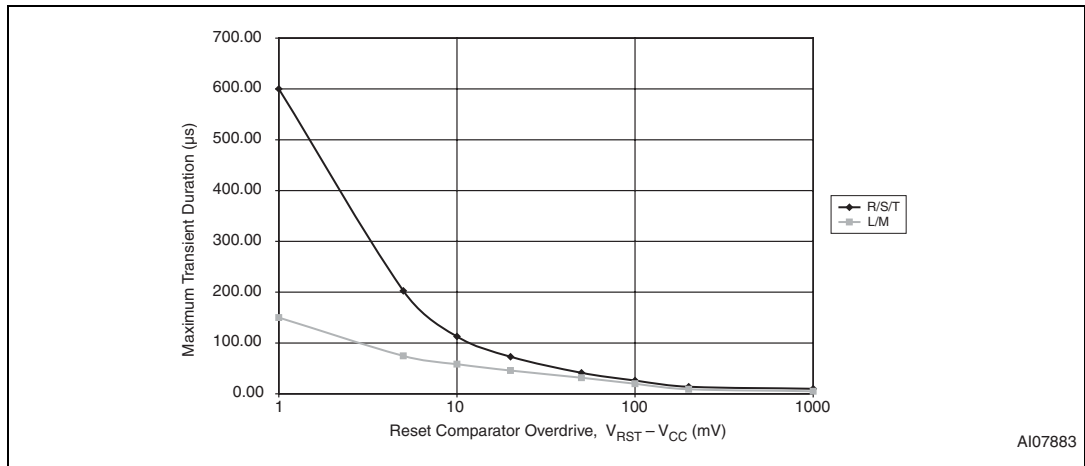


Figure 10. Max transient duration not causing reset pulse vs. reset comparator overdrive



## 4 Maximum ratings

Stressing the device above the rating listed in the absolute maximum ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$T_{STG}$	Storage temperature ( $V_{CC}$ off)	-55 to 150	°C
$T_{SLD}^{(1)}$	Lead solder temperature for 10 seconds	260	°C
$V_{IO}$	Input or output voltage	-0.3 to $V_{CC} + 0.3$	V
$V_{CC}$	Supply voltage	-0.3 to 7.0	V
$I_O$	Output current	20	mA
$P_D$	Power dissipation	320	mW

1. Reflow at peak temperature of 260 °C. The time above 255 °C must not exceed 30 seconds.

## 5 DC and AC parameters

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics tables that follow, are derived from tests performed under the measurement conditions summarized in [Table 3: Operating and AC measurement conditions](#). Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

**Table 3. Operating and AC measurement conditions**

Parameter	STM1001	Unit
V <sub>CC</sub> supply voltage	1.0 to 5.5	V
Ambient operating temperature (T <sub>A</sub> )	-40 to 85	°C
Input rise and fall times	≤ 5	ns
Input pulse voltages	0.2 to 0.8 V <sub>CC</sub>	V
Input and output timing ref. voltages	0.3 to 0.7 V <sub>CC</sub>	V

**Figure 11. AC testing input/output waveforms**

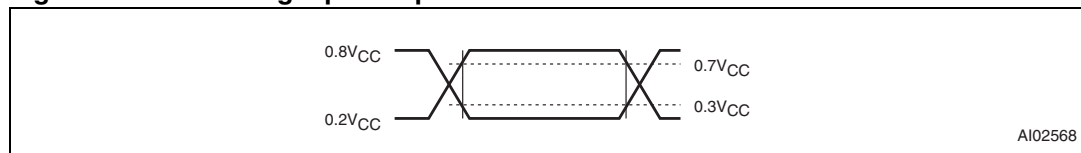


Table 4. DC and AC characteristics

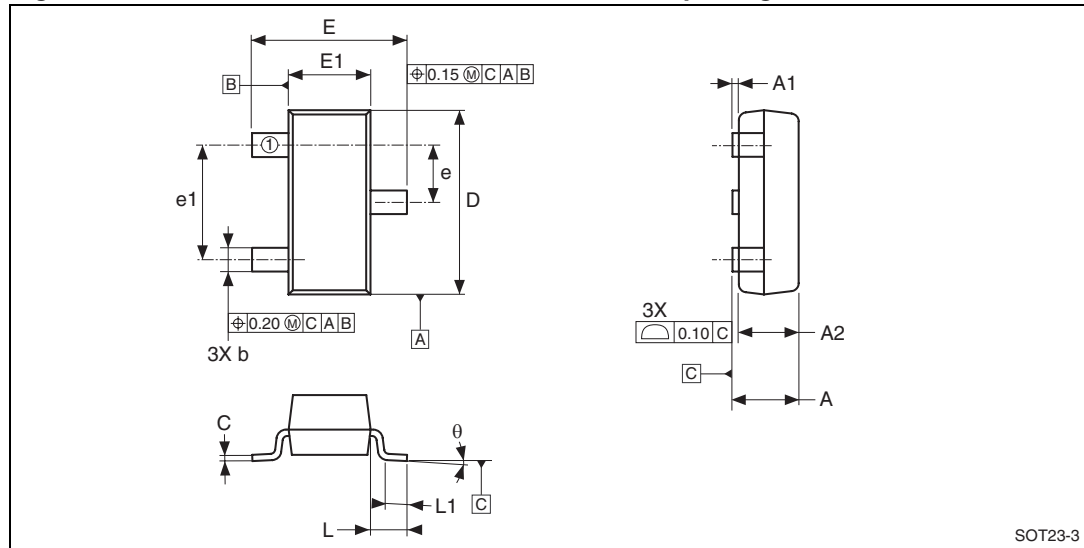
Sym	Description	Test condition <sup>(1)</sup>	Min	Typ	Max	Unit		
V <sub>CC</sub>	Operating voltage	T <sub>A</sub> = -40 to +85 °C	1.2		5.5	V		
		T <sub>A</sub> = 0 to +70 °C	1.0		5.5	V		
I <sub>CC</sub>	V <sub>CC</sub> supply current	V <sub>CC</sub> < 3.6 V		5.5	10	μA		
		V <sub>CC</sub> < 5.5 V		7	15	μA		
I <sub>LO</sub>	Open drain reset output leakage current	V <sub>CC</sub> > V <sub>RST</sub> Reset not asserted	-1		+1	μA		
V <sub>OL</sub>	$\overline{\text{RST}}$ output low voltage	STM1001R/S/T only, I <sub>OL</sub> = 1.2 mA V <sub>CC</sub> = V <sub>RST</sub> (min)			0.3	V		
		STM1001L/M only, I <sub>OL</sub> = 3.2 mA V <sub>CC</sub> = V <sub>RST</sub> (min)			0.4	V		
V <sub>OL</sub>	$\overline{\text{RST}}$ output low voltage	I <sub>OL</sub> = 50 μA; V <sub>CC</sub> > 1.0 V			0.3	V		
<b>RESET thresholds</b>								
V <sub>RST</sub>	Reset threshold	STM1001L	25 °C	4.56	4.63	4.70	V	
			-40 to 85 °C	4.50		4.75	V	
		STM1001M	25 °C	4.31	4.38	4.45	V	
			-40 to 85 °C	4.25		4.50	V	
		STM1001T	25 °C	3.04	3.08	3.11	V	
			-40 to 85 °C	3.00		3.15	V	
		STM1001S	25 °C	2.89	2.93	2.96	V	
			-40 to 85 °C	2.85		3.00	V	
		STM1001R	25 °C	2.59	2.63	2.66	V	
			-40 to 85 °C	2.55		2.70	V	
			V <sub>RST</sub> temperature coefficient	V <sub>CC</sub> = 3.3 V		45		ppm/°C
			V <sub>CC</sub> to $\overline{\text{RST}}$ delay	V <sub>CC</sub> = V <sub>RST</sub> to (V <sub>RST</sub> - 100 mV)	STM1001L/M	40		μs
STM1001R/S/T	20				μs			
t <sub>rec</sub>	$\overline{\text{RST}}$ pulse width	Option B (refer to <a href="#">Table 6</a> )	20	30	40	ms		
		Option "Blank" (refer to <a href="#">Table 6</a> )	140	210	280			

1. Valid for ambient operating temperature: T<sub>A</sub> = -40 to 85 °C; V<sub>CC</sub> = 1.2 V to 5.5 V (except where noted).

## 6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

**Figure 12. SOT23-3 – 3-lead small outline transistor package outline**



Note: Drawing is not to scale.

**Table 5. SOT23-3 – 3-lead small outline transistor package mechanical data**

Symbol	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		0.89	1.12		0.035	0.044
A1		0.01	0.10		0.001	0.004
A2		0.88	1.02		0.035	0.042
b		0.30	0.50		0.012	0.020
C		0.08	0.20		0.003	0.008
D		2.80	3.04		0.110	0.120
E		2.10	2.64		0.083	0.104
E1		1.20	1.40		0.047	0.055
e		0.89	1.03		0.035	0.041
e1		1.78	2.05		0.070	0.081
L	0.54			0.021		
L1		0.40	0.60		0.016	0.024
Q		0°	8°		0°	8°
N		3			3	

# 7 Part numbering

**Table 6. Ordering information scheme**

Example:	STM1001	S	B	WX	6	F
<b>Device type</b>						
STM1001						
<b>Reset threshold voltage</b>						
L = $V_{RST} = 4.50\text{ V to }4.75\text{ V}$						
M = $V_{RST} = 4.25\text{ V to }4.50\text{ V}$						
T = $V_{RST} = 3.00\text{ V to }3.15\text{ V}$						
S = $V_{RST} = 2.85\text{ V to }3.00\text{ V}$						
R = $V_{RST} = 2.55\text{ V to }2.70\text{ V}$						
<b>RST pulse width (<math>t_{rec}</math>)</b>						
B = 20 to 40 ms						
Blank = 140 to 280 ms						
<b>Package</b>						
WX = SOT23-3						
<b>Temperature range</b>						
6 = -40 to 85 °C						
<b>Shipping method</b>						
F = ECOPACK® package, tape & reel						

For other options, or for more information on any aspect of this device, please contact the ST sales office nearest you.

**Table 7. Marking description**

Part number	Reset threshold	Output	Topside marking <sup>(1)</sup>
STM1001LWX6F	4.63 V	Open drain $\overline{\text{RST}}$	8BAx
STM1001MWX6F	4.38 V	Open drain $\overline{\text{RST}}$	8BBx
STM1001TWX6F	3.08 V	Open drain $\overline{\text{RST}}$	8BCx
STM1001SWX6F	2.93 V	Open drain $\overline{\text{RST}}$	8BDx
STM1001RWX6F	2.63 V	Open drain $\overline{\text{RST}}$	8BEx
STM1001SBWX6F	2.93 V	Open drain $\overline{\text{RST}}$	8BMx

1. Lowercase "x" indicates date code.



## 8 Revision history

**Table 8. Document revision history**

Date	Revision	Changes
09-Dec-2003	1	First edition
19-Feb-2004	2	Part number changed from STM6301
22-Mar-2004	2.1	Update DC characteristics ( <a href="#">Table 4</a> )
09-Apr-2004	3	Device promoted; reformatted; marking updated ( <a href="#">Table 7</a> )
19-Nov-2004	4	Update dimensions ( <a href="#">Table 5</a> ).
19-Sep-2005	5	Remove "Valid RST Output Down to V <sub>CC</sub> ..." text
17-Feb-2010	6	Updated <a href="#">Features</a> ; footnote in <a href="#">Table 2</a> ; <a href="#">Table 4</a> ; <a href="#">Table 6</a> ; <a href="#">Table 7</a> ; text in <a href="#">Section 6</a> ; added note to <a href="#">Figure 8</a> ; reformatted document.

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