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STM32L552xx

Ultra-low-power Arm® Cortex®-M33 32-bit MCU+TrustZone®+FPU, 165 DMIPS, up to 512 KB Flash memory, 256 KB SRAM, SMPS

Datasheet - production data

Features

Ultra-low-power with FlexPowerControl

- 1.71 V to 3.6 V power supply
- -40 °C to 85/125 °C temperature range
- Batch acquisition mode (BAM)
- 187 nA in VBAT mode: supply for RTC and 32x32-bit backup registers
- 17 nA Shutdown mode (5 wakeup pins)
- 108 nA Standby mode (5 wakeup pins)
- 222 nA Standby mode with RTC
- 3.16 µA Stop 2 with RTC
- 106 µA/MHz Run mode (LDO mode)
- 62 µA/MHz Run mode @ 3 V (SMPS step-down converter mode)
- 5 µs wakeup from Stop mode
- Brownout reset (BOR) in all modes except Shutdown

Core

- Arm® 32-bit Cortex®-M33 CPU with TrustZone® and FPU

ART Accelerator

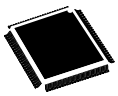
- 8-Kbyte instruction cache allowing 0-wait-state execution from Flash memory and external memories; frequency up to 110 MHz, MPU, 165 DMIPS and DSP instructions

Performance benckmark

- 1.5 DMIPS/MHz (Drystone 2.1)
- 442 CoreMark® (4.02 CoreMark®/MHz)

Energy benchmark

- 370 ULPMark-CP® score
- 54 ULPMark-PP® score
- 27400 SecureMark-TLS® score



LQFP48 (7 x 7 mm)
LQFP64 (10 x 10 mm)
LQFP100(*) (14 x14 mm)
LQFP144 (20 x 20mm)

UFQFPN48 (7 x 7 mm)

UFBGA132 (7 x 7 mm)

WLCSP81 (4.36 x 4.07 mm)

(*): Silhouette shown above.

Memories

- Up to 512-Kbyte Flash, two banks read-while-write
- 256 Kbytes of SRAM including 64 Kbytes with hardware parity check
- External memory interface supporting SRAM, PSRAM, NOR, NAND and FRAM memories
- OCTOSPI memory interface

Security

- Arm® TrustZone® and securable I/Os, memories and peripherals
- Flexible life cycle scheme with RDP (readout protection)
- Root of trust thanks to unique boot entry and hide protection area (HDP)
- SFI (secure firmware installation) thanks to embedded RSS (root secure services)
- Secure firmware upgrade support with TF-M
- HASH hardware accelerator
- Active tamper and protection against temperature, voltage and frequency attacks
- True random number generator NIST SP800-90B compliant
- 96-bit unique ID

- 512-byte OTP (one-time programmable) for user data

General-purpose input/outputs

- Up to 114 fast I/Os with interrupt capability most 5 V-tolerant and up to 14 I/Os with independent supply down to 1.08 V

Power management

- Embedded regulator (LDO) with three configurable range output to supply the digital circuitry
- Embedded SMPS step-down converter
- External SMPS support

Clock management

- 4 to 48 MHz crystal oscillator
- 32 kHz crystal oscillator for RTC (LSE)
- Internal 16 MHz factory-trimmed RC (±1%)
- Internal low-power 32 kHz RC (±5%)
- Internal multispeed 100 kHz to 48 MHz oscillator, auto-trimmed by LSE (better than ±0.25% accuracy)
- Internal 48 MHz with clock recovery
- 3 PLLs for system clock, USB, audio, ADC

Up to 16 timers and 2 watchdogs

- 16x timers: 2 x 16-bit advanced motor-control, 2 x 32-bit and 5 x 16-bit general purpose, 2x 16-bit basic, 3x low-power 16-bit timers (available in Stop mode), 2x watchdogs, 2x SysTick timer
- RTC with hardware calendar, alarms and calibration

Up to 19 communication peripherals

- 1x USB Type-C™/ USB power delivery controller
- 1x USB 2.0 full-speed crystal less solution, LPM and BCD
- 2x SAIs (serial audio interface)
- 4x I2C FM+(1 Mbit/s), SMBus/PMBus™
- 6x USARTs (ISO 7816, LIN, IrDA, modem)
- 3x SPIs (7x SPIs with USART and OCTOSPI in SPI mode)
- 1x FDCAN controller
- 1x SDMMC interface

2 DMA controllers

- 14 DMA channels

Up to 22 capacitive sensing channels

- Support touch key, linear and rotary touch sensors

Rich analog peripherals (independent supply)

- 2x 12-bit ADC 5 Msps, up to 16-bit with hardware oversampling, 200 µA/Msps
- 2x 12-bit DAC outputs, low-power sample and hold
- 2x operational amplifiers with built-in PGA
- 2x ultra-low-power comparators
- 4x digital filters for sigma delta modulator

CRC calculation unit

Debug

- Development support: serial wire debug (SWD), JTAG, Embedded Trace Macrocell™ (ETM)

Table 1. Device summary

Reference	Part numbers
STM32L552xx	STM32L552CC, STM32L552CE, STM32L552ME, STM32L552QC, STM32L552QE, STM32L552RC, STM32L552RE, STM32L552VC, STM32L552VE, STM32L552ZC, STM32L552ZE

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1 Introduction

This document provides the ordering information and mechanical device characteristics of the STM32L552xx microcontrollers.

This document should be read in conjunction with the STM32L552xx and STM32L562xx reference manual (RM0438).

For information on the Arm®(a) Cortex®-M33 core, refer to the Cortex®-M33 Technical Reference Manual, available from the www.arm.com website.

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2 Description

The STM32L552xx devices are an ultra-low-power microcontrollers family (STM32L5 Series) based on the high-performance Arm® Cortex®-M33 32-bit RISC core. They operate at a frequency of up to 110 MHz.

The Cortex®-M33 core features a single-precision floating-point unit (FPU), which supports all the Arm® single-precision data-processing instructions and all the data types. The Cortex®-M33 core also implements a full set of DSP (digital signal processing) instructions and a memory protection unit (MPU) which enhances the application's security.

These devices embed high-speed memories (512 Kbytes of Flash memory and 256 Kbytes of SRAM), a flexible external memory controller (FSMC) for static memories (for devices with packages of 100 pins and more), an Octo-SPI Flash memories interface (available on all packages) and an extensive range of enhanced I/Os and peripherals connected to two APB buses, two AHB buses and a 32-bit multi-AHB bus matrix.

The STM32L5 Series devices offer security foundation compliant with the trusted based security architecture (TBSA) requirements from Arm. They embed the necessary security features to implement a secure boot, secure data storage, secure firmware installation and secure firmware upgrade. Flexible life cycle is managed thanks to multiple levels of readout protection. Firmware hardware isolation is supported thanks to securable peripherals, memories and I/Os, and also to the possibility to configure the peripherals and memories as "privilege".

The STM32L552xx devices embed several protection mechanisms for embedded Flash memory and SRAM: readout protection, write protection, secure and hidden protection areas.

The STM32L552xx devices embed peripherals reinforcing security:

- One HASH hardware accelerator

- One true random number generator

The STM32L5 Series devices offer active tamper detection and protection against transient and environmental perturbation attacks thanks to several internal monitoring which generate secret data erase in case of attack. This helps to fit the PCI requirements for point of sales applications. These devices offer two fast 12-bit ADC (5 Msps), two comparators, two operational amplifiers, two DAC channels, an internal voltage reference buffer, a low-power RTC, two general-purpose 32-bit timer, two 16-bit PWM timers dedicated to motor control, seven general-purpose 16-bit timers, and two 16-bit low-power timers. The devices support four digital filters for external sigma delta modulators (DFSDM). In addition, up to 22 capacitive sensing channels are available.

STM32L5 Series also feature standard and advanced communication interfaces such as:

- Four I2Cs

- Three SPIs

- Three USARTs, two UARTs and one low-power UART

- Two SAIs

- One SDMMC

- One FDCAN

- USB device FS

- USB Type-C / USB power delivery controller

The devices operate in the -40 to +85 °C (+105 °C junction) and -40 to +125 °C (+130 °C junction) temperature ranges from a 1.71 to 3.6 V power supply. A comprehensive set of power-saving modes allows the design of low-power applications.

Some independent power supplies are supported like an analog independent supply input for ADC, DAC, OPAMPs and comparators, a 3.3 V dedicated supply input for USB and up to 14 I/Os, which can be supplied independently down to 1.08 V. A VBAT input allows the backup of the RTC and the backup of the registers.

The STM32L552xx devices offer seven packages from 48-pin to 144-pin.

Table 2. STM32L552xx features and peripheral counts

Peripherals		STM32L552CE, STM32L552CC/ STM32L552CExxP	STM32L552RE, STM32L552RC/ STM32L552RExxP/ STM32L552RExxQ	STM32L552MExxP/ STM32L552MExxQ	STM32L552VE/ STM32L552VExxQ, STM32L552VCxxQ	STM32L552QExxP/ STM32L552QExxQ, STM32L552QCxxQ	STM32L552ZE/ STM32L552ZExxQ, STM32L552ZCxxQ
Flash memory (Kbyte)		512/256					
SRAM	System (Kbyte)	256 (192+64)					
	Backup (byte)	128					
External memory controller for static memories (FSMC)		No			Yes		
OCTOSPI		1					
Timers	Advanced control	2 (16-bit)					
	General purpose	5 (16-bit) 2 (32-bit)					
	Basic	2 (16-bit)					
	Low power	3 (16-bit)					
	SysTick timer	1					
	Watchdog timers (independent, window)	2					

Table 2. STM32L552xx features and peripheral counts (continued)

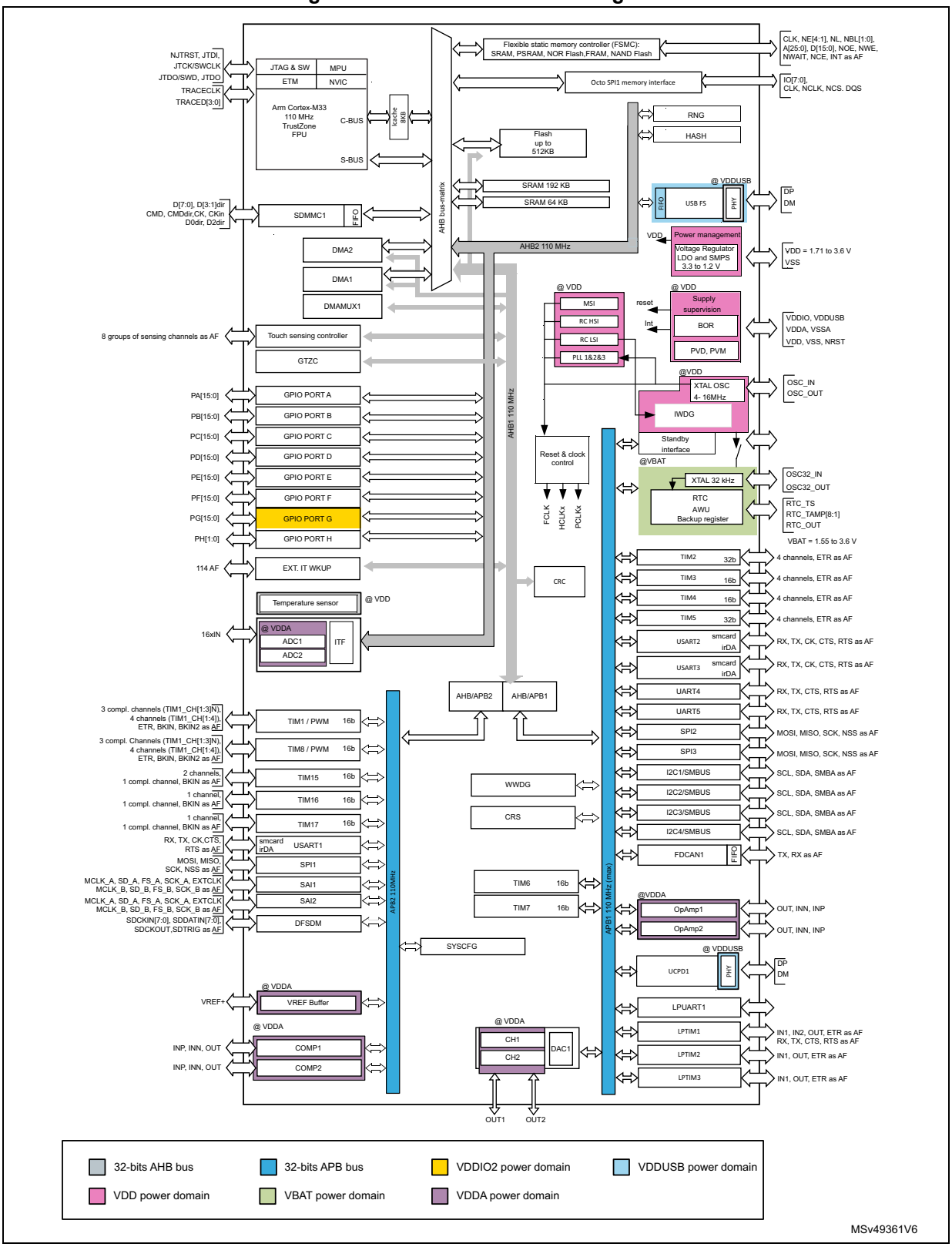
Peripherals		STM32L552CE, STM32L552CC/ STM32L552CExxP	STM32L552RE, STM32L552RC/ STM32L552RExxP/ STM32L552RExxQ	STM32L552MExxP/ STM32L552MExxQ	STM32L552VE/ STM32L552VExxQ, STM32L552VCxxQ	STM32L552QExxP/ STM32L552QExxQ, STM32L552QCxxQ	STM32L552ZE/ STM32L552ZExxQ, STM32L552ZCxxQ
Communication interfaces	SPI	3					
	I2C	4					
	USART(1)/UART UART LPUART	3/2 (2) 2 1					
	SAI	2					
	FDCAN	1					
	USB FS	Yes					
	SDMMC	No	Yes/No/Yes	Yes			
Digital filters for sigma-delta modulators		Yes (4 filters)					
Number of channels		8					
Real time clock (RTC)		Yes					
Tamper pins		3	4/4/3	3	5/4	5	8/7
True random number generator		Yes					
HASH (SHA-256)		Yes					
GPIOs Wakeup pins Nb of I/Os down to 1.08 V		38/36 3 0	52/50/47 4/3/3 0	54/51 3 6	83/79 5/4 0	108/105 5 13/10	115 /111 5/4 14/13
Capacitive sensing Number of channels		5	10/10/9	10	19/18	22	22/21
ADC	12-bit ADC	2					
	Number of channels	9	16/16/15	16/15	16/14	16	16/14
DAC	12-bit DAC	1					
	Number of channels	2					
Internal voltage reference buffer		Yes					
Analog comparator		2					
Operational amplifiers		2					
Max. CPU frequency		110 MHz					

Table 2. STM32L552xx features and peripheral counts (continued)

Peripherals	STM32L552CE, STM32L552CC/ STM32L552CExxP	STM32L552RE, STM32L552RC/ STM32L552RExxP/ STM32L552RExxQ	STM32L552MExxP/ STM32L552MExxQ	STM32L552VE/ STM32L552VExxQ, STM32L552VCxxQ	STM32L552QExxP/ STM32L552QExxQ, STM32L552QCxxQ	STM32L552ZE/ STM32L552ZExxQ, STM32L552ZCxxQ
Operating voltage	1.71 to 3.6 V					
Operating temperature	Ambient operating temperature: -40 to 85 °C / -40 to 125 °C Junction temperature: -40 to 105 °C / -40 to 130 °C					
Package	LQFP48, UFQFPN48	LQFP64	WLCSP81	LQFP100(2)	UFBGA132	LQFP144

1. USART3 is not available on STM32L552CExxP devices.
2. For the LQFP100 package, only FSMC Bank1 is available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 Chip Select.

Figure 1. STM32L552xx block diagram



1. AF: alternate function on I/O pins.

3 Functional overview

3.1 Arm® Cortex®-M33 core with TrustZone® and FPU

The Cortex®-M33 with TrustZone and FPU is a highly energy efficient processor designed for microcontrollers and deeply embedded applications, especially those requiring efficient security.

The Cortex®-M33 processor delivers a high computational performance with low-power consumption and an advanced response to interrupts. it features:

- Arm® TrustZone® technology, using the Armv8-M main extension supporting secure and non-secure states
- Memory protection units (MPUs), 8 regions for secure and 8 regions for non secure
- Configurable secure attribute unit (SAU) supporting up to 8 memory regions
- Floating-point arithmetic functionality with support for single precision arithmetic

The processor supports a set of DSP instructions that allows an efficient signal processing and a complex algorithm execution.

The Cortex®-M33 processor supports the following bus interfaces:

- System AHB bus:
  The System AHB (S-AHB) bus interface is used for any instruction fetch and data access to the memory-mapped SRAM, peripheral, external RAM and external device, or Vendor_SYS regions of the Armv8-M memory map.
- Code AHB bus
  The Code AHB (C-AHB) bus interface is used for any instruction fetch and data access to the code region of the Armv8-M memory map.

Figure 1 shows the general block diagram of the STM32L552xx family devices.

3.2 Art Accelerator – instruction cache (ICACHE)

The instruction cache (ICACHE) is introduced on C-AHB code bus of Cortex®-M33 processor to improve performance when fetching instruction (or data) from both internal and external memories.

ICACHE offers the following features:

- Multi-bus interface:
  - slave port receiving the memory requests from the Cortex®-M33 C-AHB code execution port
  - master1 port performing refill requests to internal memories (FLASH and SRAMs)
  - master2 port performing refill requests to external memories (external FLASH/RAMs through Octo-SPI/FMC interfaces)
  - a second slave port dedicated to ICACHE registers access.
- Close to zero wait states instructions/data access performance:
  - 0 wait-state on cache hit
  - hit-under-miss capability, allowing to serve new processor requests while a line refill (due to a previous cache miss) is still ongoing
  - critical-word-first refill policy, minimizing processor stalls on cache miss
  - hit ratio improved by 2-ways set-associative architecture and pLRU-t replacement policy (pseudo-least-recently-used, based on binary tree), algorithm with best complexity/performance balance
  - dual master ports allowing to decouple internal and external memory traffics, on Fast and Slow buses, respectively; also minimizing impact on interrupt latency
  - optimal cache line refill thanks to AHB burst transactions (of the cache line size).
  - performance monitoring by means of a hit counter and a miss counter.
- Extension of cacheable region beyond Code memory space, by means of address remapping logic that allows to define up to 4 cacheable external regions
- Power consumption reduced intrinsically (most accesses to cache memory rather to bigger main memories); even improved by configuring ICACHE as direct mapped (rather than the default 2-ways set-associative mode)
- TrustZone® security support
- Maintenance operation for software management of cache coherency
- Error management: detection of unexpected cacheable write access, with optional interrupt raising.

3.3 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to the memory and to prevent one task to accidentally corrupt the memory or the resources used by any other active task. This memory area is organized into up to 8 regions for secure and 8 regions for non secure state.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

3.4 Embedded Flash memory

The devices feature 512 Kbytes of embedded Flash memory which is available for storing programs and data.

The Flash interface features:

- Single or dual bank operating modes
- Read-while-write (RWW) in dual bank mode

This feature allows a read operation to be performed from one bank while an erase or program operation is performed to the other bank. The dual bank boot is also supported. Each bank contains 128 pages of 2 or 4 Kbytes (depending on the read access width). The Flash memory also embeds 512 bytes OTP (one-time programmable) for user data.

Flexible protections can be configured thanks to the option bytes:

- Readout protection (RDP) to protect the whole memory. Four levels of protection are available:
  - Level 0: no readout protection
  - Level 0.5: available only when TrustZone is enabled
    All read/write operations (if no write protection is set) from/to the non-secure Flash memory are possible. The Debug access to secure area is prohibited. Debug access to non-secure area remains possible.
  - Level 1: memory readout protection; the Flash memory cannot be read from or written to if either the debug features are connected or the boot in RAM or bootloader are selected. If TrustZone is enabled, the non-secure debug is possible and the boot in SRAM is not possible.
  - Level 2: chip readout protection; the debug features (Cortex®-M33 JTAG and serial wire), the boot in RAM and the bootloader selection are disabled (JTAG fuse). This selection is irreversible.
- Write protection (WRP): the protected area is protected against erasing and programming:
  - In single bank mode, four areas can be selected with 4-Kbyte granularity.
  - In dual bank mode, two areas per bank can be selected with 2-Kbyte granularity.

The whole non-volatile memory embeds the error correction code (ECC) feature supporting:

- Single error detection and correction
- Double error detection
- The address of the ECC fail can be read in the ECC register.

TrustZone security

When the TrustZone security is enabled, the whole Flash is secure after reset and the following protections are available:

- Non-volatile watermark-based secure Flash area: the secure area can be accessed only in secure mode.
  - In single bank mode, four areas can be selected with a page granularity.
  - In dual bank mode, one area per bank can be selected with a page granularity.
- Secure hidden protection area: it is part of the Flash secure area and it can be protected to deny an access to this area by any data read, write and instruction fetch.

For example, a software code in the secure Flash memory hidden protection area can be executed only once and deny any further access to this area until next system reset.

- Volatile block-based secure Flash area. In a block-based secure area, each page can be programmed on-the-fly as secure or non-secure.

3.5 Embedded SRAM

The devices feature 256 Kbytes of embedded SRAM. This SRAM is split into three blocks:

- 192 Kbytes mapped at address 0x2000 0000 (SRAM1).
- 64 Kbytes located at address 0x0A03 0000 with hardware parity check (SRAM2). This memory is also mapped at address 0x2003 0000 offering a contiguous address space with the SRAM1.
  This block is accessed through the C-bus for maximum performance. Either 64 Kbytes or upper 4 Kbytes of SRAM2 can be retained in Standby mode.
  The SRAM2 can be write-protected with 1 Kbyte granularity.

The memory can be accessed in read/write at CPU clock speed with 0 wait states.

TrustZone security

When the TrustZone security is enabled, all SRAMs are secure after reset. The SRAM can be programmed as non-secure by block based using the MPCBB (memory protection controller block based) in GTZC controller. The granularity of SRAM secure block based is a page of 256 bytes.

3.6 Boot modes

At startup, a BOOT0 pin, nBOOT0 and NSBOOTADDx[24:0] / SECBOOTADD0[24:0] option bytes are used to select the boot memory address which includes:

- Boot from any address in user Flash
- Boot from system memory bootloader
- Boot from any address in embedded SRAM
- Boot from Root Security service (RSS)

The BOOT0 value may come from the PH3-BOOT0 pin or from an option bit depending on the value of a user option bit to free the GPIO pad if needed.

The boot loader is located in the system memory. It is used to reprogram the Flash memory by using USART, I2C, SPI, FDCAN or USB FS in device mode through the DFU (device firmware upgrade).

The bootloader is available on all devices. Refer to the application note *STM32 microcontroller system memory boot mode* (AN2606) for more details.

The root secure services (RSS) are embedded in a Flash memory area named secure information block, programmed during ST production.

The RSS enables for example the secure firmware installation (SFI) thanks to the RSS extension firmware (RSSe SFI).

This feature allows the customers to protect the confidentiality of the firmware to be provisioned into the STM32 device when the production is subcontracted to a third party.

The RSS is available on all devices, after enabling the TrustZone through the TZEN option bit.

Refer to the application note *Overview secure firmware install (SFI)* (AN4992) for more details.

Refer to *Table 3* and *Table 4* for boot modes when TrustZone is disabled and enabled respectively.

Table 3. Boot modes when TrustZone is disabled (TZEN=0)

nBOOT0 FLASH_ OPTR[27]	BOOT0 pin PH3	nSWBOOT0 FLASH_ OPTR[26]	Boot address option-bytes selection	Boot area	ST programmed default value
-	0	1	NSBOOTADD0[24:0]	Boot address defined by user option bytes NSBOOTADD0[24:0]	Flash: 0x0800 0000
-	1	1	NSBOOTADD1[24:0]	Boot address defined by user option bytes NSBOOTADD1[24:0]	System bootloader: 0x0BF9 0000
1	-	0	NSBOOTADD0[24:0]	Boot address defined by user option bytes NSBOOTADD0[24:0]	Flash: 0x0800 0000
0	-	0	NSBOOTADD1[24:0]	Boot address defined by user option bytes NSBOOTADD1[24:0]	System bootloader: 0x0BF9 0000

When TrustZone is enabled by setting the TZEN option bit, the boot space must be in secure area. The SECBOOTADD0[24:0] option bytes are used to select the boot secure memory address.

A unique boot entry option can be selected by setting the BOOT_LOCK option bit, allowing to boot always at the address selected by SECBOOTADD0[24:0] option bytes. All other boot options are ignored.

Table 4. Boot modes when TrustZone is enabled (TZEN=1)

BOOT_LOCK	nBOOT0 FLASH_OPTR[27]	BOOT0 pin PH3	nSWBOOT0 FLASH_OPTR[26]	RSS command	Boot address option-bytes selection	Boot area	ST programmed default value
0	-	0	1	0	SECBOOTADD0[24:0]	Secure boot address defined by user option bytes SECBOOTADD0[24:0]	Flash: 0x0C00 0000
	-	1	1	0	N/A	RSS: 0x0FF8 0000	RSS: 0x0FF8 0000
	1	-	0	0	SECBOOTADD0[24:0]	Secure boot address defined by user option bytes SECBOOTADD0[24:0]	Flash: 0x0C00 0000
	0	-	0	0	N/A	RSS: RSS: 0x0FF8 0000	RSS: 0x0FF8 0000
	-	-	-	≠ 0	N/A	RSS: RSS: 0x0FF8 0000	RSS: 0x0FF8 0000
1	-	-	-	-	SECBOOTADD0[24:0]	Secure boot address defined by user option bytes SECBOOTADD0[24:0]	Flash: 0x0C00 0000

The boot address option bytes enables the possibility to program any boot memory address. However, the allowed address space depends on Flash read protection RDP level.

If the programmed boot memory address is out of the allowed memory mapped area when RDP level is 0.5 or more, the default boot fetch address is forced to:

- 0x0800 0000 (when TZEN = 0)
- RSS (when TZEN = 1)

Refer to *Table 5*.

Table 5. Boot space versus RDP protection

RDP	TZEN = 1	TZEN = 0
0	Any boot address	Any boot address

Table 5. Boot space versus RDP protection (continued)

RDP	TZEN = 1	TZEN = 0
0.5	Boot address only in: – RSS – or secure Flash: 0x0C00 0000 - 0x0C07 FFFF Otherwise boot address forced to RSS	N/A
1		Any boot address
2		If boot is configured for NSBOOTADD0 and NSBOOTADD0 in the range 0x0800 0000 - 0x0807 FFFF: boot at the address stored in NSBOOTADD0 If boot is configured for NSBOOTADD1 and NSBOOTADD1 in the range 0x0800 0000 - 0x0807 FFFF: boot at the address stored in NSBOOTADD1 Otherwise boot address is forced at 0x0800 0000

3.7 Global TrustZone controller (GTZC)

The GTZC includes three different sub-blocks:

- **TZSC**: TrustZone® security controller
  This sub-block defines the secure/privilege state of slave/master peripherals. It also controls the non-secure area size for the watermark memory peripheral controller (MPCWM). The TZSC block informs some peripherals (such as RCC or GPIOs) about the secure status of each securable peripheral, by sharing with RCC and I/O logic.

1. **MPCBB**: block-based memory protection controller
   This sub-block controls secure states of all blocks (256-byte pages) of the associated SRAM.
2. **TZIC**: TrustZone illegal access controller
   This sub-block gathers all illegal access events in the system and generates a secure interrupt towards NVIC.

These sub-blocks are used to configure TrustZone and privileged attributes within the full system.

The GTZC main features are:

- 3 independent 32-bit AHB interface for TZSC, MPCBB and TZIC
- MPCBB and TZIC accessible only with secure transactions
- Secure and non-secure access supported for priv/non-priv part of TZSC
- Register set to define security settings:
  - Secure blocks for internal SRAM
  - Non-secure regions for external memories
  - Secure/privilege access mode for securable and TZ-aware peripherals
- Secure/privilege access mode for securable legacy masters.

3.8 TrustZone security architecture

The security architecture is based on Arm® TrustZone® with the Armv8-M Main Extension.

The TrustZone security is activated by the TZEN option bit in the FLASH_OPTR register.

When the TrustZone is enabled, the SAU (security attribution unit) and IDAU (implementation defined attribution unit) defines the access permissions based on secure and non-secure state.

- SAU: Up to 8 SAU configurable regions are available for security attribution.
- IDAU: It provides a first memory partition as non-secure or non-secure callable attributes. It is then combined with the results from the SAU security attribution and the higher security state is selected.

Based on IDAU security attribution, the Flash, system SRAMs and peripherals memory space is aliased twice for secure and non-secure state. However, the external memories space is not aliased.

Table 6 shows an example of typical SAU regions configuration based on IDAU regions. The user can split and choose the secure, non-secure or NSC regions for external memories as needed.

Table 6. Example of memory map security attribution vs SAU configuration regions(1) (2)

Region description	Address range	IDAU security attribution	SAU security attribution typical configuration	Final security attribution
Code - external memories	0x0000_0000 0x07FF_FFFF	Non-secure	Secure or non-secure or NSC	Secure or non-secure or NSC
Code - Flash and SRAM	0x0800_0000 0x0BFF_FFFF	Non-secure	Non-secure	Non-secure
	0x0C00_0000 0x0FFF_FFFF	NSC	Secure or NSC	Secure or NSC
Code - external memories	0x1000_0000 0x17FF_FFFF	Non-secure	Non-secure	
	0x1800_0000 0x1FFF_FFFF			
SRAM	0x2000_0000 0x2FFF_FFFF	Non-secure		
	0x3000_0000 0x3FFF_FFFF	NSC	Secure or NSC	Secure or NSC
Peripherals	0x4000_0000 0x4FFF_FFFF	Non-secure	Non-secure	Non-secure
	0x5000_0000 0x5FFF_FFFF	NSC	Secure or NSC	Secure or NSC
External memories	0x6000_0000 0xDFFF_FFFF	Non-secure	Secure or non-secure or NSC	Secure or non-secure or NSC

1. NSC = non-secure callable.

2. Different colors highlights the different configurations
Pink: Non-secure
Green: NSC (non-secure callable)
Lighter green: Secure or non-secure or NSC

3.8.1 TrustZone peripheral classification

When the TrustZone security is active, a peripheral can be either Securable or TrustZone-aware type as follows:

- Securable: a peripheral is protected by an AHB/APB firewall gate that is controlled from TZSC controller to define security properties.
- TrustZone-aware: a peripheral connected directly to AHB or APB bus and is implementing a specific TrustZone behavior such as a subset of registers being secure.

The tables below summarize the list of Securable and TrustZone aware peripherals within the system.

Table 7. Securable peripherals by TZSC

Bus	Peripheral
AHB3	OCTOSPI1 registers
	FMC registers
AHB 2	SDMMC1
	RNG
	ADC
AHB1	ICACHE registers
	TSC
	CRC
APB2	DFSDM1
	SAI2
	SAI1
	TIM17
	TIM16
	TIM15
	USART1
	TIM8
	SPI1
	TIM1
	COMP
	VREFBUF

Table 7. Securable peripherals by TZSC (continued)

Bus	Peripheral
APB1	UCPD1
	USB FS
	FDCAN1
	LPTIM3
	LPTIM2
	I2C4
	LPUART1
	LPTIM1
	OPAMP
	DAC1
	CRS
	I2C3
	I2C2
	I2C1
	UART5
	UART4
	USART3
	USART2
	SPI3
	SPI2
	IWDG
	WWDG
	TIM7
	TIM6
	TIM5
	TIM4
	TIM3
	TIM2

Table 8. TrustZone-aware peripherals

Bus	Peripheral
AHB2	GPIOH
	GPIOG
	GPIOF
	GPIOE
	GPIOD
	GPIOC
	GPIOB
	GPIOA
AHB1	MPCBB2
	MPCBB1
	MPCWM2
	MPCWM1
	TZIC
	TZSC
	EXTI
	Flash memory
	RCC
	DMAMUX1
	DMA2
	DMA1
APB2	SYSCFG
APB1	PWR
	RTC

Default TrustZone security state

The default system security state is:

- CPU:
  - Cortex®-M33 is in secure state after reset. The boot address must be in secure address.
- Memory map:
  - SAU: is fully secure after reset. Consequently, all memory map is fully secure. Up to 8 SAU configurable regions are available for security attribution.
- Flash:
  - Flash security area is defined by watermark user options.
  - Flash block based area is non-secure after reset.
- SRAMs:
  - All SRAMs are secure after reset. MPCBB (memory protection block based controller) is secure.
- External memories:
  - FSMC, OCTOSPI banks are secure after reset. MPCWMx (memory protection watermark based controller) are secure
- Peripherals
  - Securable peripherals are non-secure after reset.
  - TrustZone-aware peripherals (except the GPIO) are non-secure after reset. Their secure configuration registers are secure.

Note: Refer to Table 7 and Table 8 for a list of Securable and TrustZone-aware peripherals.

- All GPIO are secure after reset.
- Interrupts:
  - NVIC: All interrupts are secure after reset. NVIC is banked for secure and non-secure state.
  - TZIC: All illegal access interrupts are disabled after reset.

3.9 Power supply management

The power controller (PWR) main features are:

- Power supplies and supply domains
  - Core domains (VCORE)
  - VDD domain
  - Backup domain (VBAT)
  - Analog domain (VDDA)
  - VDDIO2 domain
  - VDDUSB for USB transceiver
- System supply voltage regulation
  - SMPS step down converter
  - Voltage regulator (LDO)
- Power supply supervision
  - POR/PDR monitor
  - BOR monitor
  - PVD monitor
  - PVM monitor (VDDA, VDDUSB, VDDIO2)
  - Temperature thresholds monitor
  - Upper VDD voltage threshold monitor
- Power management
  - Operating modes
  - Voltage scaling control
  - Low-power modes
- VBAT battery charging
- TrustZone security

3.9.1 Power supply schemes

The devices require a 1.71 V to 3.6 V V_{DD} operating voltage supply. Several independent supplies can be provided for specific peripherals:

- V_{DD} = 1.71 V to 3.6 V

  V_{DD} is the external power supply for the I/Os, the internal regulator and the system analog such as reset, power management and internal clocks. It is provided externally through the VDD pins.
- V_{DDA} = 1.62 V (ADCs/COMPs) / 1.8 V (DACs/OPAMPs) to 2.4 V (VREFBUF) to 3.6 V

  V_{DDA} is the external analog power supply for A/D converters, D/A converters, voltage reference buffer, operational amplifiers and comparators. The V_{DDA} voltage level is independent from the V_{DD} voltage and should preferably be connected to V_{DD} when these peripherals are not used.

- VDDSMPS = 1.71 V to 3.6 V
  VDDSMPS is the external power supply for the SMPS step down converter. It is provided externally through VDDSMPS supply pin, and shall be connected to the same supply as VDD.
- VLXSMPS is the switched SMPS step down converter output.
- V15SMPS are the power supply for the system regulator. It is provided externally through the SMPS step down converter VLXSMPS output.

Note: The SMPS power supply pins are available only on a specific package with SMPS step down converter option.

- VDD12 = 1.05 to 1.32 V
  VDD12 is the external power supply bypassing the internal regulator when connected to an external SMPS. It is provided externally through VDD12 pins and only available on packages with the external SMPS supply option. VDD12 does not require any external decoupling capacitance and cannot support any external load.
- VDDUSB = 3.0 V to 3.6 V
  VDDUSB is the external independent power supply for USB transceivers. The VDDUSB voltage level is independent from the VDD voltage and should preferably be connected to VDD when the USB is not used.
- VDDIO2 = 1.08 V to 3.6 V
- VDDIO2 is the external power supply for 14 I/Os (port G[15:2]). The VDDIO2 voltage level is independent from the VDD voltage and should preferably be connected to VDD when PG[15:2] are not used.
- V_{BAT} = 1.55 V to 3.6 V

  V_{BAT} is the power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.
- V_{REF-}, V_{REF+}

  V_{REF+} is the input reference voltage for ADCs and DACs. It is also the output of the internal voltage reference buffer when enabled.

  When V_{DDA} < 2 V V_{REF+} must be equal to V_{DDA}.

  When V_{DDA} ≥ 2 V V_{REF+} must be between 2 V and V_{DDA}.

  V_{REF+} can be grounded when ADC and DAC are not active.

  The internal voltage reference buffer supports two output voltages, which are configured with VRS bit in the VREFBUF_CSR register:

  – V_{REF+} around 2.048 V. This requires V_{DDA} equal to or higher than 2.4 V.
  – V_{REF+} around 2.5 V. This requires V_{DDA} equal to or higher than 2.8 V.

  VREF- and VREF+ pins are not available on all packages. When not available, they are bonded to VSSA and VDDA, respectively.
  When the VREF+ is double-bonded with VDDA in a package, the internal voltage reference buffer is not available and must be kept disabled (refer to datasheet for packages pinout description).
  V_{REF-} must always be equal to V_{SSA}.

An embedded linear voltage-regulator is used to supply the internal digital power V_{CORE}. V_{CORE} is the power supply for digital peripherals, SRAM1 and SRAM2. The Flash is supplied by V_{CORE} and V_{DD}.

Figure 2. STM32L552xx power supply overview

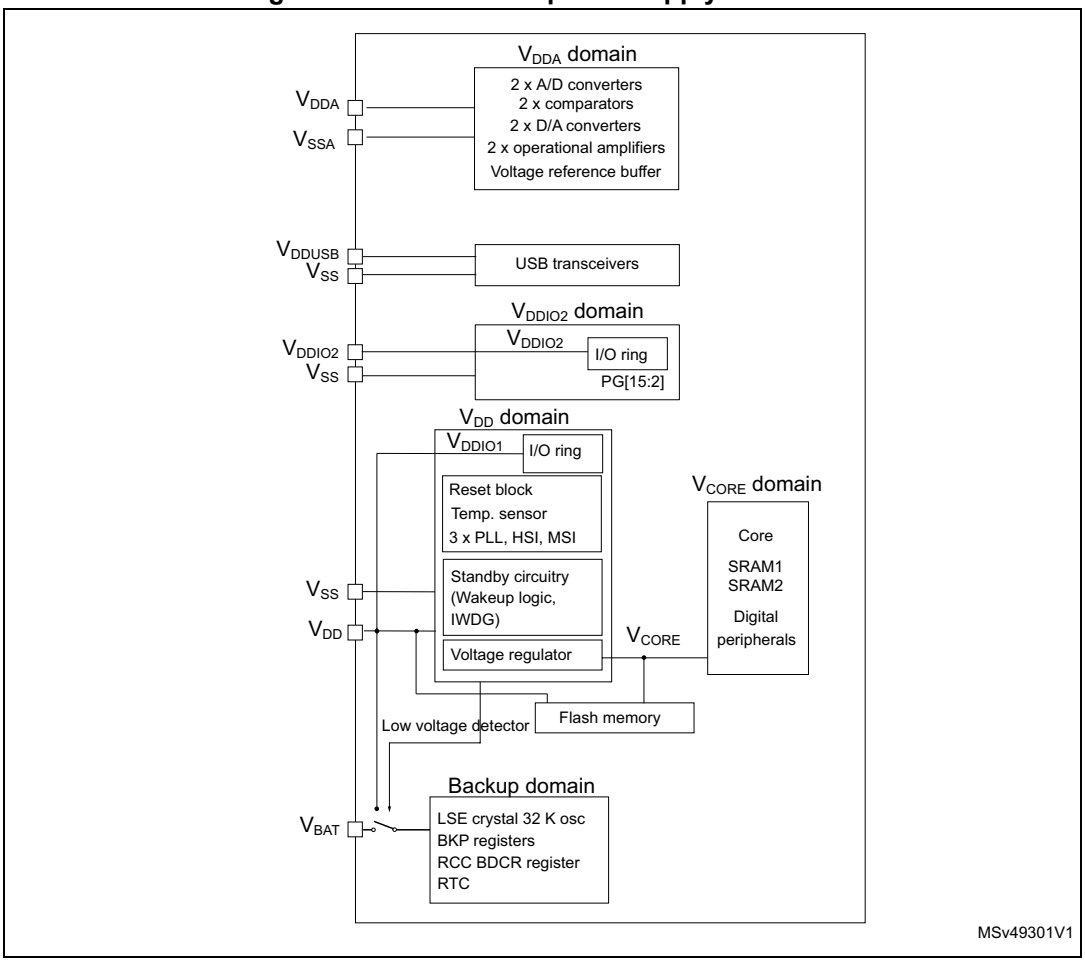


Figure 3. STM32L552xxxxP power supply overview

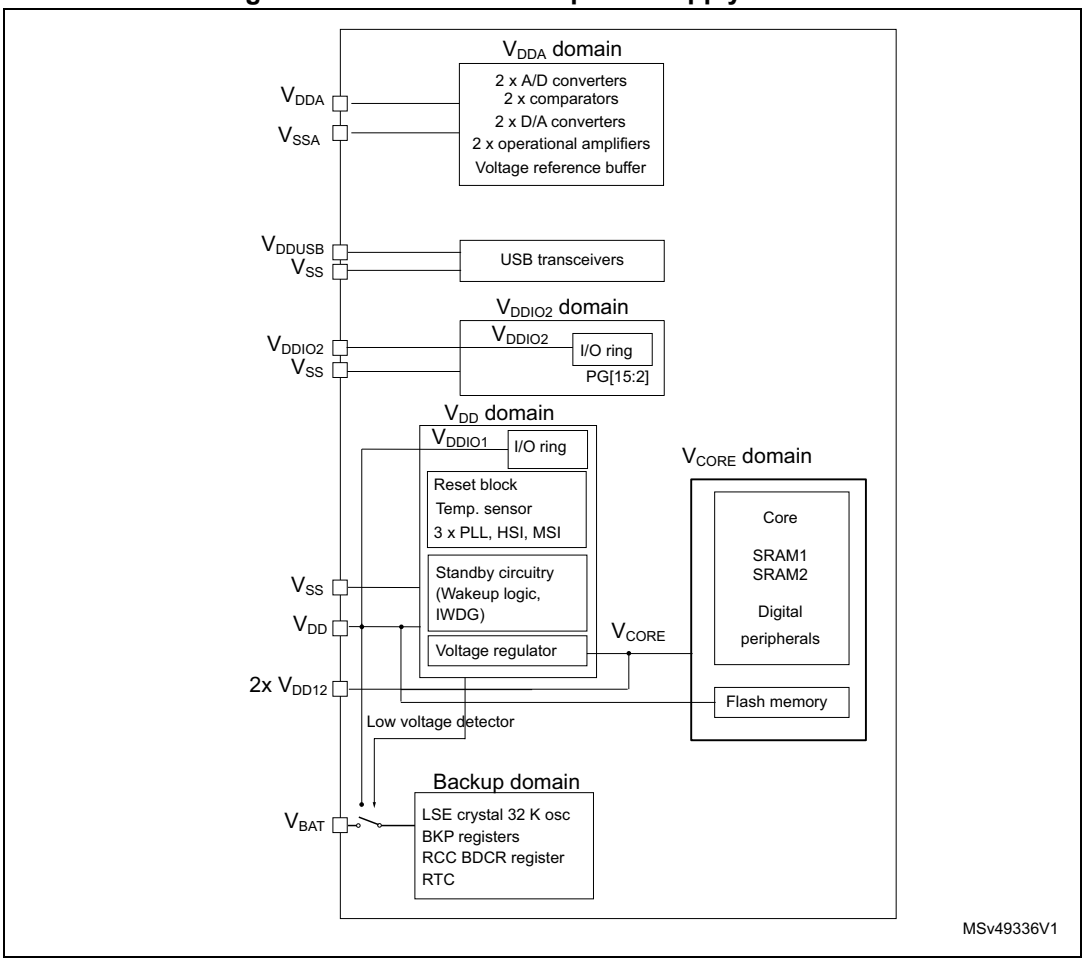
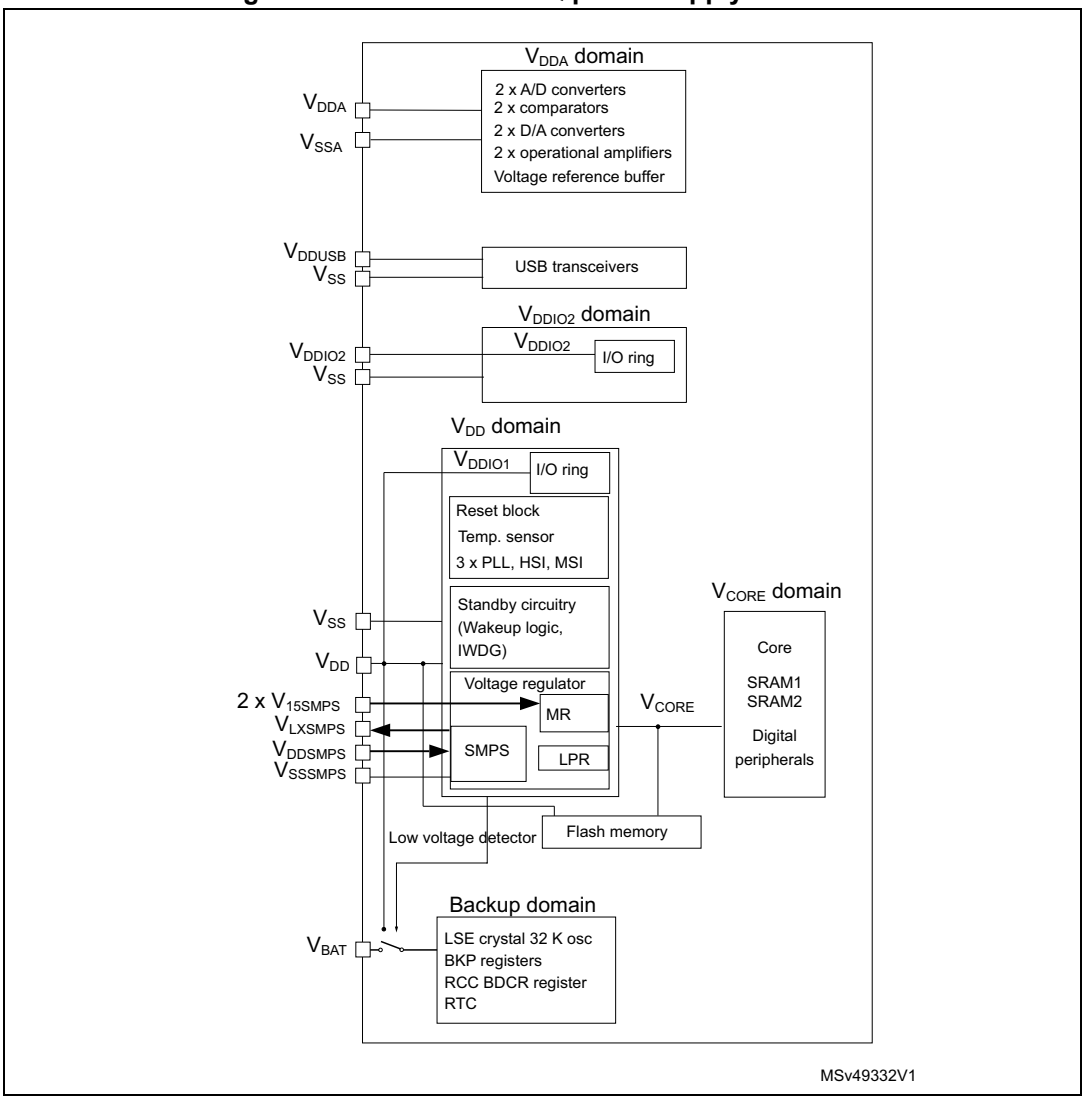


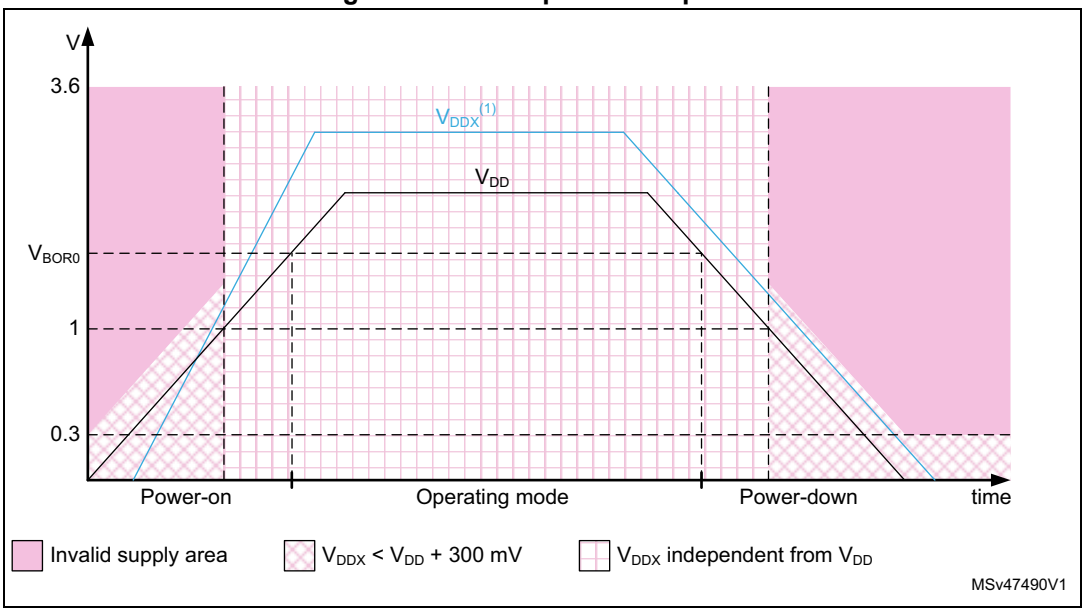
Figure 4. STM32L552xxxxQ power supply overview



During power-up and power-down phases, the following power sequence requirements must be respected:

- When V_{DD} is below 1 V, other power supplies (V_{DDA}, V_{DDIO2} and V_{DDUSB}) must remain below VDD +300 mV.
- When V_{DD} is above 1 V, all power supplies are independent.
- During the power-down phase, V_{DD} can temporarily become lower than other supplies only if the energy provided to the MCU remains below 1 mJ; this allows external decoupling capacitors to be discharged with different time constants during the power-down transient phase.

Figure 5. Power-up/down sequence



1. V_{DDX} refers to any power supply among V_{DDA}, V_{DDIO2} and V_{DDUSB}.

3.9.2 Power supply supervisor

The devices have an integrated ultra-low-power Brownout reset (BOR) active in all modes (except for Shutdown mode). The BOR ensures proper operation of the devices after power-on and during power down. The devices remain in reset mode when the monitored supply voltage V_{DD} is below a specified threshold, without the need for an external reset circuit.

The lowest BOR level is 1.71 V at power on, and other higher thresholds can be selected through option bytes.The devices feature an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it to the VPVD threshold.

An interrupt can be generated when V_{DD} drops below the VPVD threshold and/or when V_{DD} is higher than the VPVD threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

In addition, the devices embed a peripheral voltage monitor which compares the independent supply voltages V_{DDA}, V_{DDUSB}, V_{DDIO2} with a fixed threshold in order to ensure that the peripheral is in its functional supply range.

3.9.3 Voltage regulator

Two embedded linear voltage regulators supply most of the digital circuitries: the main regulator (MR) and the low-power regulator (LPR).

- The MR is used in the Run and Sleep modes and in the Stop 0 mode.
- The LPR is used in Low-power run, Low-power sleep, Stop 1 and Stop 2 modes. It is also used to supply the 64 Kbytes or only 4 Kbytes of SRAM2 in standby with SRAM2 retention.
- Both regulators are in power-down while they are in standby and Shutdown modes: the regulator output is in high impedance, and the kernel circuitry is powered down thus inducing zero consumption.

The ultra-low-power STM32L552xx devices support dynamic voltage scaling to optimize its power consumption in Run mode. The voltage from the main regulator that supplies the logic (VCORE) can be adjusted according to the system's maximum operating frequency.

The main regulator operates in the following ranges:

- Range 0 with the CPU running at up to 110 MHz.
- Range 1 with the CPU running at up to 80 MHz.
- Range 2 with a maximum CPU frequency of 26 MHz. All peripheral clocks are also limited to 26 MHz.

The VCORE can be supplied by the low-power regulator, the main regulator being switched off. The system is then in Low-power run mode.

- Low-power run mode with the CPU running at up to 2 MHz. Peripherals with independent clock can be clocked by the HSI16.

3.9.4 SMPS step down converter

The built-in SMPS step down converter is a highly power-efficient DC/DC non-linear switching regulator that improves low-power performance when the VDD voltage is high enough. This SMPS step down converter automatically enters in bypass mode when the VDD voltage falls below 2 V in Range 0 and Range 1.

Note: There is no automatic SMPS bypass in Range 2.

The SMPS step down converter can be configured in:

- High-power mode (HPM): achieving a high efficiency at high current load. It is the default selected mode after POR reset.
- Low power mode achieving very high efficiency at low load
- Bypass mode

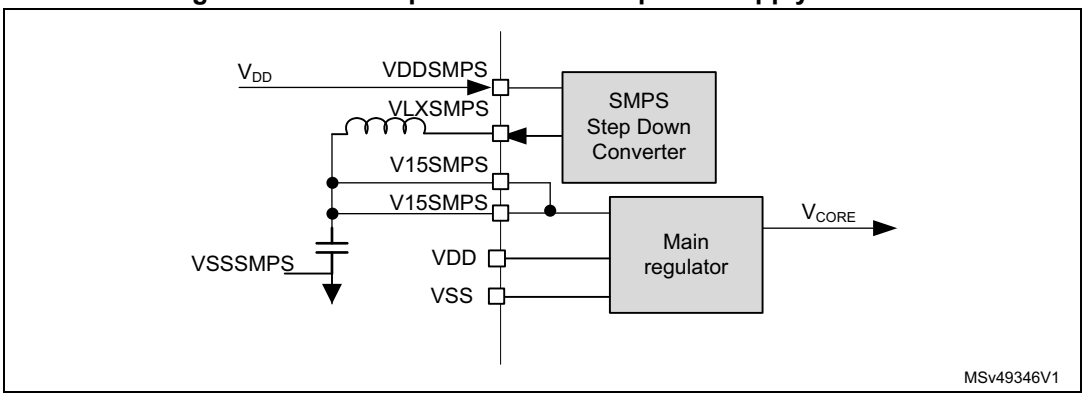
The SMPS step down converter can be switched in bypass mode at any time by the application software.

Note: The SMPS step down converter is available only on specific package.

SMPS step down converter power supply scheme

The SMPS step down converter requires an external coil with typical value of 4.7 µH to be connected between the VLXSMPS and the V15SMPS pins and a 4.7µF capacitor to be connected between the V15SMPS to VSSSMPS pins. It can be switched OFF by selecting the Bypass mode by software. Thus, only main regulator is used by the application.

Figure 6. SMPS step down converter power supply scheme



If the selected package is with the SMPS step down converter option but it is never used by the application, it is recommend to set the SMPS power supply pins as follows:

- V_{DDSMPS} and V_{LXSMPS} connected to VSS
- V_{15SMPS} connected to VDD

Table 9. SMPS external components

Component	Description	Value
C	SMPS output capacitor(1)	4.7 µF
L	SMPS inductance(2)	4.7 µH

1. For example GRM155R60J475ME87J and GRM21BR71E475KA73L.
2. For example TDK MLP2016H4R7MT.

SMPS step down converter fast startup

After POR reset, the SMPS step down converter starts in High-power mode and in Low startup mode. The low-startup feature is selected to limit the inrush current after power-on reset.

However, it is possible to configure a faster startup on the fly and it is applied for next startup either after a system reset or wakeup from low-power mode except Shutdown and VBAT modes. The fast startup is selected by setting the SMPSFSTEN bit in the PWR_CR4 register.

3.9.5 Low-power modes

The ultra-low-power STM32L552xx devices support seven low-power modes to achieve the bes
consumption, short startup time, available peripherals and available wake-up sources. *Table 11*
modes overview.

Table 10. STM32L552xx modes overview

Mode	Regulator and SMPS mode(1)	CPU	Flash	SRAM	Clocks	DMA and Periphe
Run	Ranges 0/1 SMPS HP mode	Yes	ON(3)	ON	Any	All
	Range 2 SMPS LP or HP mode					All except USB_FS
LPRun	LPR	Yes	ON(3)	ON	Any except PLL	All except USB_FS
Sleep	Ranges 0/1 SMPS HP mode	No	ON(3)	ON(4)	Any	All
	Range 2 SMPS LP or HP mode					All except USB_FS
LPSleep	LPR	No	ON(3)	ON(4)	Any except PLL	All except USB_FS
Stop 0(5)	Ranges 0/1/2	No	Off	ON	LSE LSI	BOR, PVD, PV RTC, IWDG COMPx (x=1, DAC1 OPAMPx (x=1 USARTx (x=1... LPUART1(6) I2Cx (x=1...4) LPTIMx (x=1, *** All other peripherals a

Table 10. STM32L552xx modes overview (continued)

Mode	Regulator and SMPS mode[1]	CPU	Flash	SRAM	Clocks	DMA and Periphe
Stop 1	LPR	No	Off	ON	LSE LSI	BOR, PVD, PV RTC, IWDG COMPx (x=1, DAC1 OPAMPx (x=1 USARTx (x=1... LPUART1[6] I2Cx (x=1...4) LPTIMx (x=1, *** All other peripherals a
Stop 2	LPR	No	Off	ON	LSE LSI	BOR, PVD, PV RTC, IWDG COMPx (x=1.. I2C3[7] LPUART1[6] LPTIMx (x= 1, *** All other peripherals a

Table 10. STM32L552xx modes overview (continued)

Mode	Regulator and SMPS mode[1]	CPU	Flash	SRAM	Clocks	DMA and Periphe
Standby	LPR	Powered Off	Off	SRAM2 ON	LSE LSI	BOR, RTC, IWD *** All other peripherals ar off *** I/O configuration can b pull-up or pull-d
	OFF			Powered Off		
Shutdown	OFF	Powered Off	Off	Powered Off	LSE	RTC *** All other peripherals ar off *** I/O configuration can b pull-up or pull-dow

1. LPR means Main regulator is OFF and Low-power regulator is ON.
2. All peripherals can be active or clock gated to save power consumption.
3. The Flash memory can be put in power-down and its clock can be gated off when executing from SRAM.
4. The SRAM1 and SRAM2 clocks can be gated on or off independently.
5. SMPS mode can be used in Stop 0 mode, but no significant power gain can be expected.
6. U(S)ART and LPUART reception is functional in Stop mode, and generates a wakeup interrupt on Start, address match or received
7. I2C address detection is functional in Stop mode, and generates a wakeup interrupt in case of address match.
8. USB_FS wakeup by resume from suspend and attach detection protocol event.
9. The I/Os with wakeup from Standby/Shutdown capability are: PA0, PC13, PE6, PA2, PC5.
10. I/Os can be configured with internal pull-up, pull-down or floating in Shutdown mode but the configuration is lost when exiting the Sl

By default, the microcontroller is in Run mode after a system or a power reset. It is up to the user to select one of the low-power modes described below:

- **Sleep** mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Low-power run** mode

  This mode is achieved with VCORE supplied by the low-power regulator to minimize the regulator's operating current. The code can be executed from SRAM or from Flash, and the CPU frequency is limited to 2 MHz. The peripherals with independent clock can be clocked by HSI16.

- **Low-power sleep** mode

  This mode is entered from the Low-power run mode. Only the CPU clock is stopped. When wakeup is triggered by an event or an interrupt, the system reverts to the Low-power run mode.

- **Stop 0, Stop 1 and Stop 2** modes

  Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the VCORE domain are stopped, the PLL, the MSI RC, the HSI16 RC and the HSE crystal oscillators are disabled. The LSE or LSI is still running.

  The RTC can remain active (Stop mode with RTC, Stop mode without RTC).

  Some peripherals with wake-up capability can enable the HSI16 RC during Stop mode to detect their wake-up condition.

  Three Stop modes are available: Stop 0, Stop 1 and Stop 2 modes. In Stop 2 mode, most of the VCORE domain is put in a lower leakage mode.

  Stop 1 offers the largest number of active peripherals and wakeup sources, a smaller wakeup time but a higher consumption than Stop 2. In Stop 0 mode, the main regulator remains ON, allowing a very fast wakeup time but with much higher consumption.

  The system clock when exiting from Stop 0, Stop 1 or Stop 2 modes can be either MSI up to 48 MHz or HSI16, depending on software configuration.

- **Standby** mode

  The Standby mode is used to achieve the lowest power consumption with BOR. The internal regulator is switched off so that the VCORE domain is powered off. The PLL, the MSI RC, the HSI16 RC and the HSE crystal oscillators are also switched off.

  The RTC can remain active (Standby mode with RTC, Standby mode without RTC).

  The Brownout reset (BOR) always remains active in Standby mode.

  The state of each I/O during Standby mode can be selected by software: I/O with internal pull-up, internal pull-down or floating.

  After entering Standby mode, SRAM1 and register contents are lost except for registers in the Backup domain and Standby circuitry. Optionally, the full SRAM2 or 4 Kbytes can be retained in Standby mode, supplied by the low-power regulator (standby with RAM2 retention mode).

The BORL (brown out detector low) can be configured in ultra-low-power mode to further reduce power consumption during standby mode.

The device exits Standby mode when an external reset (NRST pin), an IWDG reset, WKUP pin event (configurable rising or falling edge), or an RTC event occurs (alarm, periodic wakeup, timestamp, tamper) or a failure is detected on LSE (CSS on LSE).

The system clock after wakeup is MSI up to 8 MHz.

- **Shutdown** mode

  The Shutdown mode allows to achieve the lowest power consumption. The internal regulator is switched off so that the VCORE domain is powered off. The PLL, the HSI16, the MSI, the LSI and the HSE oscillators are also switched off.

  The RTC can remain active (Shutdown mode with RTC, Shutdown mode without RTC).

  The BOR is not available in Shutdown mode. No power voltage monitoring is possible in this mode, therefore the switch to Backup domain is not supported.

  SRAM1, SRAM2 and register contents are lost except for registers in the Backup domain.

  The device exits Shutdown mode when an external reset (NRST pin), a WKUP pin event (configurable rising or falling edge), or an RTC event occurs (alarm, periodic wakeup, timestamp, tamper).

  The system clock after wakeup is MSI at 4 MHz.

Table 11. Functionalities depending on the working mode(1)

Peripheral	Run	Sleep	Low-power run	Low-power sleep	Stop 0/1		Stop 2		Standby		Shutdown		VBAT
					-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	
CPU	Y	-	Y	-	-	-	-	-	-	-	-	-	-
Flash memory (512 Kbyte)	O(2)	O(2)	O(2)	O(2)	-	-	-	-	-	-	-	-	-
SRAM1 (192 Kbytes)	Y	Y(3)	Y	Y(3)	Y	-	Y	-	-	-	-	-	-
SRAM2 (64 Kbytes)	Y	Y(3)	Y	Y(3)	Y	-	Y	-	O(4)	-	-	-	-
FSMC	O	O	O	O	-	-	-	-	-	-	-	-	-
OCTOSPI	O	O	O	O	-	-	-	-	-	-	-	-	-
Backup registers	Y	Y	Y	Y	Y	-	Y	-	Y	-	Y	-	Y
Brownout reset (BOR)	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	-	-
Programmable voltage detector (PVD)	O	O	O	O	O	O	O	O	-	-	-	-	-
Peripheral voltage monitor (PVMx; x=1,2,3,4)	O	O	O	O	O	O	O	O	-	-	-	-	-
DMA	O	O	O	O	-	-	-	-	-	-	-	-	-
High speed internal (HSI16)	O	O	O	O	(5)	-	(5)	-	-	-	-	-	-
Oscillator HSI48	O	O	-	-	-	-	-	-	-	-	-	-	-
High speed external (HSE)	O	O	O	O	-	-	-	-	-	-	-	-	-
Low speed internal (LSI)	O	O	O	O	O	-	O	-	O	-	-	-	-
Low speed external (LSE)	O	O	O	O	O	-	O	-	O	-	O	-	O
Multi speed internal (MSI)	O	O	O	O	-	-	-	-	-	-	-	-	-
Clock security system (CSS)	O	O	O	O	-	-	-	-	-	-	-	-	-
Clock security system on LSE	O	O	O	O	O	O	O	O	O	O	-	-	-

Table 11. Functionalities depending on the working mode[1] (continued)

Peripheral	Run	Sleep	Low-power run	Low-power sleep	Stop 0/1		Stop 2		Standby		Shutdown		VBAT
					-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	
V_{DD} voltage monitoring, temperature monitoring	O	O	O	O	O	O	O	O	O	O	-	-	-
RTC / TAMP	O	O	O	O	O	O	O	O	O	O	O	O	O
Number of RTC Tamper pins	8	8	8	8	8	O	8	O	8	O	8	O	3
USB, UCPD	O[8]	O[8]	-	-	-	O	-	-	-	-	-	-	-
USARTx (x=1,2,3,4,5)	O	O	O	O	O[6]	O[6]	-	-	-	-	-	-	-
Low-power UART (LPUART)	O	O	O	O	O[6]	O[6]	O[6]	O[6]	-	-	-	-	-
I2Cx (x=1,2,4)	O	O	O	O	O[7]	O[7]	-	-	-	-	-	-	-
I2C3	O	O	O	O	O[7]	O[7]	O[7]	O[7]	-	-	-	-	-
SPIx (x=1,2,3)	O	O	O	O	-	-	-	-	-	-	-	-	-
FDCAN1	O	O	O	O	-	-	-	-	-	-	-	-	-
SDMMC1	O	O	O	O	-	-	-	-	-	-	-	-	-
SAIx (x=1,2)	O	O	O	O	-	-	-	-	-	-	-	-	-
DFSDM1	O	O	O	O	-	-	-	-	-	-	-	-	-
ADCx (x=1,2)	O	O	O	O	-	-	-	-	-	-	-	-	-
DAC1	O	O	O	O	O	-	-	-	-	-	-	-	-
VREFBUF	O	O	O	O	O	-	-	-	-	-	-	-	-
OPAMPx (x=1,2)	O	O	O	O	O	-	-	-	-	-	-	-	-
COMPx (x=1,2)	O	O	O	O	O	O	O	O	-	-	-	-	-
Temperature sensor	O	O	O	O	-	-	-	-	-	-	-	-	-
Timers (TIMx)	O	O	O	O	-	-	-	-	-	-	-	-	-
Low-power timer 1, 3 (LPTIM1 and LPTIM3)	O	O	O	O	O	O	O	O	-	-	-	-	-
Low-power timer 2 (LPTIM2)	O	O	O	O	O	O	-	-	-	-	-	-	-
Independent watchdog (IWDG)	O	O	O	O	O	O	O	O	O	O	-	-	-

Table 11. Functionalities depending on the working mode(1) (continued)

Peripheral	Run	Sleep	Low-power run	Low-power sleep	Stop 0/1		Stop 2		Standby		Shutdown		VBAT
					-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	
Window watchdog (WWDG)	O	O	O	O	-	-	-	-	-	-	-	-	-
SysTick timer	O	O	O	O	-	-	-	-	-	-	-	-	-
Touch sensing controller (TSC)	O	O	O	O	-	-	-	-	-	-	-	-	-
Random number generator (RNG)	O(8)	O(8)	-	-	-	-	-	-	-	-	-	-	-
CRC calculation unit	O	O	O	O	-	-	-	-	-	-	-	-	-
GPIOs	O	O	O	O	O	O	O	O	(9)	5 pins (10)	(11)	5 pins (10)	-

1. Legend: Y = yes (enable). O = optional (disable by default, can be enabled by software). - = not available.

Gray cells highlight the wakeup capability in each mode.

2. The Flash can be configured in Power-down mode. By default, it is not in Power-down mode.
3. The SRAM clock can be gated on or off.
4. 4 Kbytes or full SRAM2 content is preserved depending on RRS[1:0] bits configuration in PWR_CR3 register.
5. Some peripherals with wakeup from Stop capability can request HSI16 to be enabled. In this case, HSI16 is woken up by the peripheral, and only feeds the peripheral which requested it. HSI16 is automatically put off when the peripheral does not need it anymore.
6. UART and LPUART reception is functional in Stop mode, and generates a wakeup interrupt on Start, address match or received frame event.
7. I2C address detection is functional in Stop mode, and generates a wakeup interrupt in case of address match.
8. Voltage scaling ranges 0 and 1 only.
9. I/Os can be configured with internal pull-up, pull-down or floating in Standby mode.
10. The I/Os with wakeup from standby/shutdown capability are: PA0, PC13, PE6, PA2, PC5.
11. I/Os can be configured with internal pull-up, pull-down or floating in Shutdown mode but the configuration is lost when exiting the Shutdown mode.

3.9.6 Reset mode

In order to improve the consumption under reset, the I/Os state under and after reset is “analog state” (the I/O schmitt trigger is disable). In addition, the internal reset pull-up is deactivated when the reset source is internal.

3.9.7 VBAT operation

The VBAT pin allows the device VBAT domain to be powered from an external battery, an external supercapacitor, or from V_{DD} when there is no external battery and when an external

supercapacitor is present. The VBAT pin supplies the RTC with LSE and the backup registers. Three anti-tamper detection pins are available in VBAT mode.

The VBAT operation is automatically activated when V_{DD} is not present. An internal VBAT battery charging circuit is embedded and can be activated when V_{DD} is present.

Note: When the microcontroller is supplied from VBAT, neither external interrupts nor RTC alarm/events exit the microcontroller from the VBAT operation.

3.9.8 PWR TrustZone security

When the TrustZone security is activated by the TZEN option bit, the PWR is switched in TrustZone security mode.

The PWR TrustZone security allows to secure the following configuration:

- Low-power mode
- Wake-up (WKUP) pins
- Voltage detection and monitoring
- VBAT mode

Other PWR configuration bits are secure when:

- The system clock selection is secure in RCC, the voltage scaling (VOS) configuration is secure
- A GPIO is configured as secure, it's corresponding bit for Pull-up/Pull-down in standby mode is secure
- The RTC is secure, the backup domain write protection bit in PWR is secure.

3.10 Peripheral interconnect matrix

Several peripherals have direct connections between them, which allow autonomous communication between them and support the saving of CPU resources (thus power supply consumption). In addition, these hardware connections allow fast and predictable latency.

Depending on the peripherals, these interconnections can operate in Run, Sleep, Low-power run and Sleep, Stop 0, Stop 1 and Stop 2 modes. See *Table 12* for more details.

Table 12. STM32L552xx peripherals interconnect matrix

Interconnect source	Interconnect destination	Interconnect action	Run	Sleep	Low-power run	Low-power sleep	Stop 0 / Stop 1	Stop 2
TIMx	TIMx	Timers synchronization or chaining	Y	Y	Y	Y	-	-
	ADC DAC1 DFSDM1	Conversion triggers	Y	Y	Y	Y	-	-
	DMA	Memory to memory transfer trigger	Y	Y	Y	Y	-	-
	COMPx	Comparator output blanking	Y	Y	Y	Y	-	-

Table 12. STM32L552xx peripherals interconnect matrix (continued)

Interconnect source	Interconnect destination	Interconnect action	Run	Sleep	Low-power run	Low-power sleep	Stop 0 / Stop 1	Stop 2
COMPx	TIM1, 8 TIM2, 3	Timer input channel, trigger, break from analog signals comparison	Y	Y	Y	Y	-	-
	LPTIMERx	Low-power timer triggered by analog signals comparison	Y	Y	Y	Y	Y	Y (1)
ADCx	TIM1, 8	Timer triggered by analog watchdog	Y	Y	Y	Y	-	-
RTC	TIM16	Timer input channel from RTC events	Y	Y	Y	Y	-	-
	LPTIMERx	Low-power timer triggered by RTC alarms or tampers	Y	Y	Y	Y	Y	Y (1)
All clocks sources (internal and external)	TIM2 TIM15, 16, 17	Clock source used as input channel for RC measurement and trimming	Y	Y	Y	Y	-	-
USB	TIM2	Timer triggered by USB SOF	Y	Y	-	-	-	-
CSS CPU (hard fault) RAM (parity error) Flash memory (ECC error) COMPx PVD DFSDM1 (analog watchdog, short circuit detection)	TIM1,8 TIM15,16,17	Timer break	Y	Y	Y	Y	-	-
GPIO	TIMx	External trigger	Y	Y	Y	Y	-	-
	LPTIMERx	External trigger	Y	Y	Y	Y	Y	Y (1)
	ADC DAC1 DFSDM1	Conversion external trigger	Y	Y	Y	Y	-	-

1. LPTIM1 and LPTIM3 only.

3.11 Reset and clock controller (RCC)

The clock controller (see *Figure 7*) distributes the clocks coming from the different oscillators to the core and to the peripherals. It also manages the clock gating for low-power modes and ensures the clock robustness. It features:

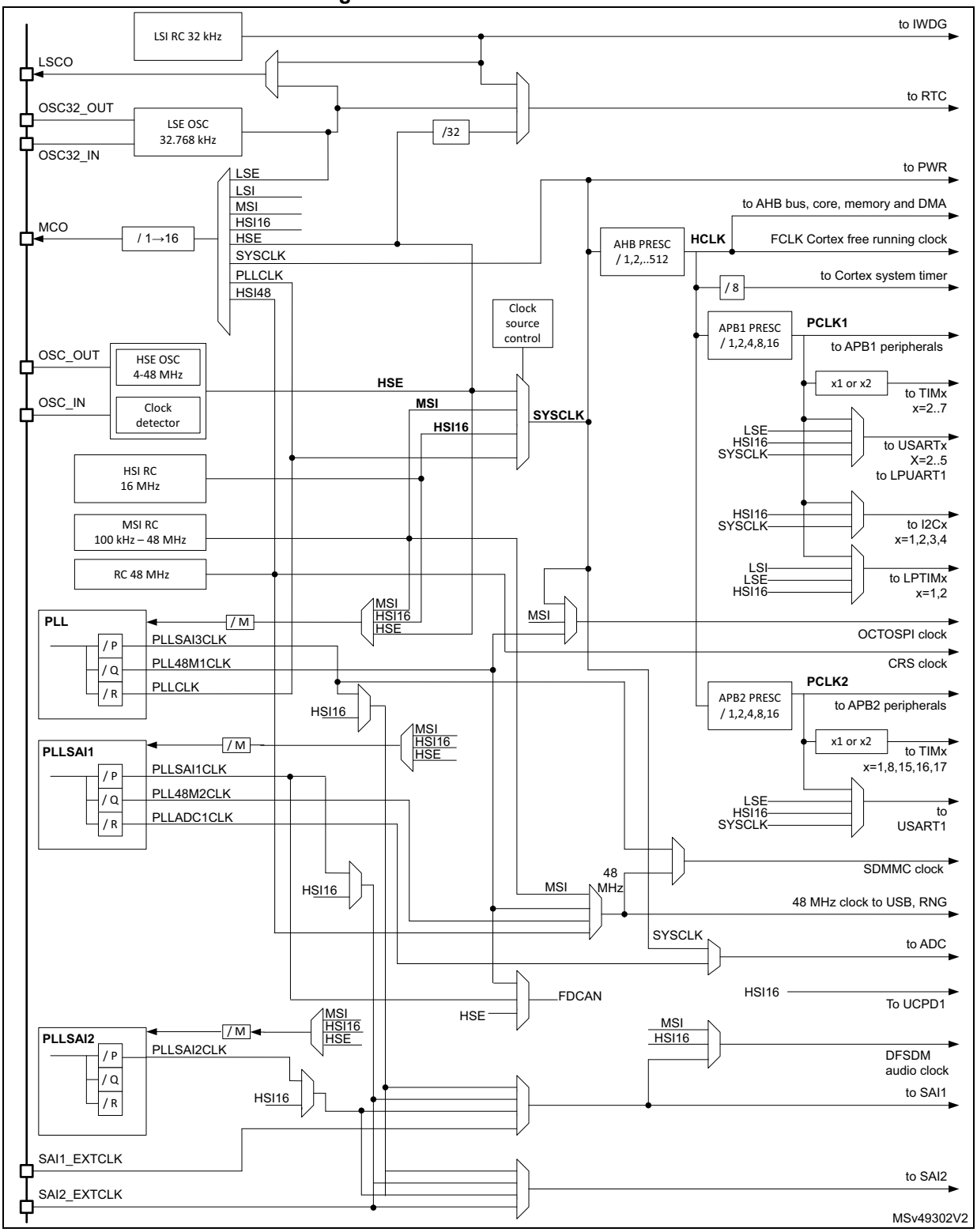
- **Clock prescaler:** to get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler.
- **Clock security system:** clock sources can be changed safely on the fly in Run mode through a configuration register.
- **Clock management:** to reduce the power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **System clock source:** four different clock sources can be used to drive the master clock SYSCLK:
  - 4 to 48 MHz high-speed external crystal or ceramic resonator (HSE), that can supply a PLL. The HSE can also be configured in bypass mode for an external clock.
  - 16 MHz high-speed internal RC oscillator (HSI16), trimmable by software, that can supply a PLL
  - Multispeed internal RC oscillator (MSI), trimmable by software, able to generate 12 frequencies from 100 kHz to 48 MHz. When a 32.768 kHz clock source is available in the system (LSE), the MSI frequency can be automatically trimmed by hardware to reach better than ±0.25% accuracy. In this mode the MSI can feed the USB device, saving the need of an external high-speed crystal (HSE). The MSI can supply a PLL.
  - System PLL which can be fed by HSE, HSI16 or MSI, with a maximum frequency at 110 MHz.
- **RC48 with clock recovery system (HSI48):** internal 48 MHz clock source (HSI48)can be used to drive the USB, the SDMMC or the RNG peripherals. This clock can be output on the MCO.
- **UCPD kernel clock**: it is derived from HSI16 clock. The HSI16 RC oscillator must be enabled prior to the UCPD kernel clock use.
- **Auxiliary clock source:** two ultra-low-power clock sources that can be used to drive the real-time clock:
  - 32.768 kHz low-speed external crystal (LSE), supporting four drive capability modes. The LSE can also be configured in bypass mode for an external clock.
  - 32 kHz low-speed internal RC (LSI), also used to drive the independent watchdog. The LSI clock accuracy is ±5% accuracy. The LSI clock can be divided by 128 to output a 250 Hz as source clock.
- **Peripheral clock sources:** several peripherals (USB, SDMMC, RNG, SAI, USARTs, I2Cs, LPTimers, ADC) have their own independent clock whatever the system clock. Three PLLs, each having three independent outputs allowing the highest flexibility, can generate independent clocks for the ADC, the USB/SDMMC/RNG and the two SAIs.
- **Startup clock:** after reset, the microcontroller restarts by default with an internal 4 MHz clock (MSI). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS):** this feature can be enabled by software. If a HSE clock failure occurs, the master clock is automatically switched to HSI16 and a software

interrupt is generated if enabled. LSE failure can also be detected and generated an interrupt.

- Clock-out capability:
  - **MCO (microcontroller clock output):** it outputs one of the internal clocks for external use by the application
  - **LSCO (low-speed clock output):** it outputs LSI or LSE in all low-power modes (except VBAT).

Several prescalers allow to configure the AHB frequency, the high speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the AHB and the APB domains is 110 MHz.

Figure 7. STM32L552xx clock tree



TrustZone security

When the TrustZone security is activated by the TZEN option bit, the RCC is switched in TrustZone security mode.

The RCC TrustZone security allows to secure some RCC system configuration and peripheral configuration clock from being read or modified by non-secure accesses:

- RCC system security:
  - HSE, HSE-CSS, HSI, MSI, LSI, LSE, LSE-CSS, HSI48 configuration and status bits
  - Main PLL, PLLSAI1, PLLSAI2, AHB prescaler configuration and status bits
  - System clock SYSCLK and HSI48 source clock selection and status bits
  - MCO clock output configuration and STOPWUCK bit
  - Reset flag RMVF configuration bit
- RCC peripheral security:
  - When a peripheral is secure, the related peripheral clock, reset, clock source selection and clock enable during low power modes control bits are secure.
- A peripheral is in secure state when:
  - For securable peripherals, when it's corresponding SEC security bit is set in the TZSC (TrustZone security controller)
  - For TrustZone-aware peripherals, a security feature of this peripheral is enabled through its dedicated bits.

3.12 Clock recovery system (CRS)

The devices embed a special block which allows automatic trimming of the internal 48 MHz oscillator to guarantee its optimal accuracy over the whole device operational range. This automatic trimming is based on the external synchronization signal, which could be either derived from USB SOF signalization, from LSE oscillator, from an external signal on CRS_SYNC pin or generated by user software. For faster lock-in during startup it is also possible to combine automatic trimming with manual trimming action.

3.13 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions.

After reset, all GPIOs are in Analog mode to reduce power consumption.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

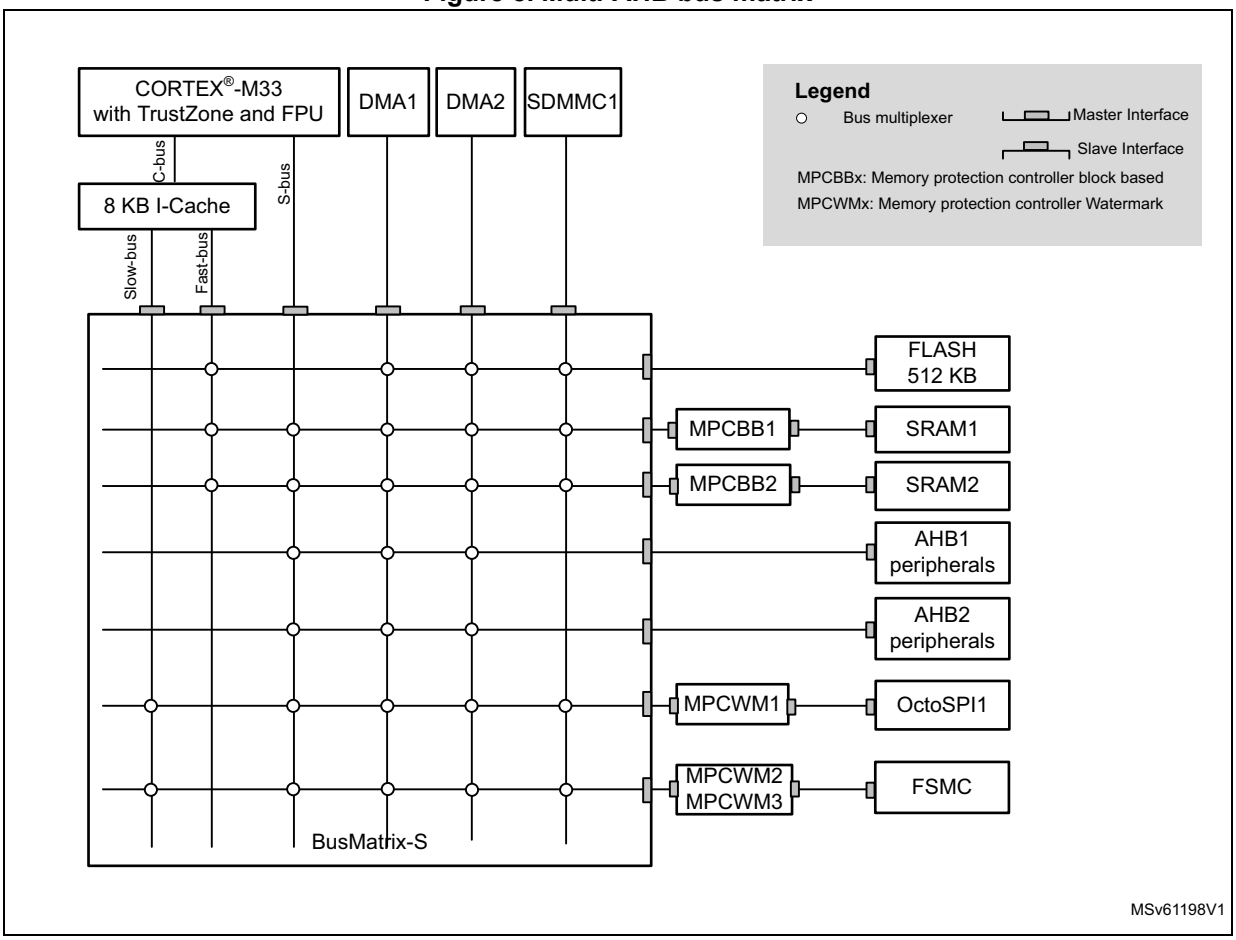
GPIO TrustZone security

Each I/O pin of GPIO port can be individually configured as secure. When the selected I/O pin is configured as secure, its corresponding configuration bits for alternate function, mode selection, I/O data are secure against a non-secure access. The associated registers bit access is restricted to a secure software only. After reset, all GPIO ports are secure.

3.14 Multi-AHB bus matrix

The 32-bit multi-AHB bus matrix interconnects all the masters (CPU, DMAs, SDMMC1) and the slaves (Flash memory, RAM, FMC, OCTOSPI, AHB and APB peripherals). It also ensures a seamless and efficient operation even when several high-speed peripherals work simultaneously.

Figure 8. Multi-AHB bus matrix



3.15 Direct memory access controller (DMA)

The device embeds 2 DMAs. Refer to *Table 13: DMA1 and DMA2 implementation* for the features implementation.

Direct memory access (DMA) is used in order to provide a high-speed data transfer between peripherals and memory as well as from memory to memory. Data can be quickly moved by DMA without any CPU actions. This keeps the CPU resources free for other operations.

The two DMA controllers have 16 channels in total, each one dedicated to manage memory access requests from one or more peripherals. Each controller has an arbiter for handling the priority between DMA requests.

The DMA supports 8 channels for each DMA1 and DMA2, independently configurable:

- Each channel is associated either with a DMA request signal coming from a peripheral, or with a software trigger in memory-to-memory transfers. This configuration is done by software.
- Priority between the requests is programmable by software (4 levels per channel: very high, high, medium, low) or by hardware in case of equality (such as request 1 has priority over request 2).
- Transfer size of source and destination are independent (byte, half-word, word), emulating packing and unpacking. Source and destination addresses must be aligned on the data size.
- Support of transfers from/to peripherals to/from memory with circular buffer management.
- Programmable number of data to be transferred: 0 to 2^{18} - 1.
- Generation of an interrupt request per channel. Each interrupt request is caused from any of the three DMA events: transfer complete, half transfer, or transfer error.
- TrustZone support:
  - Support for AHB secure and non-secure DMA transfers, independently at a first channel level, and independently at a source and destination sub-level
  - TrustZone-aware AHB slave port, protecting any secure resource (register, register field) from a non-secure software access
- Privileged / unprivileged support:
  - Support for AHB privileged and unprivileged DMA transfers, independently at a channel level
  - Privileged-aware AHB slave port.

Table 13. DMA1 and DMA2 implementation

Feature	DMA1	DMA2
Number of DMA channels	8	8
TrustZone	1 (supported)	1 (supported)

3.16 DMA request router (DMAMUX)

When a peripheral indicates a request for DMA transfer by setting its DMA request line, the DMA request is pending until it is served and the corresponding DMA request line is reset. The DMA request router allows to route the DMA control lines between the peripherals and the DMA controllers of the product.

An embedded multi-channel DMA request generator can be considered as one of such peripherals. The routing function is ensured by a multi-channel DMA request line multiplexer. Each channel selects a unique set of DMA control lines, unconditionally or synchronously with events on synchronization inputs.

DMAMUX main features

- 16-channel programmable DMA request line multiplexer output
- 4-channel DMA request generator
- 23 trigger inputs to DMA request generator
- 23 synchronization inputs
- Per DMA request generator channel:
  - DMA request trigger input selector
  - DMA request counter
  - Event overrun flag for selected DMA request trigger input
- Per DMA request line multiplexer channel output:
  - 90 input DMA request lines from peripherals
  - One DMA request line output
  - Synchronization input selector
  - DMA request counter
  - Event overrun flag for selected synchronization input
  - One event output, for DMA request chaining
- TrustZone support:
  - Support for AHB secure and non-secure DMA transfers, independently at a channel level.
  - TrustZone-aware AHB slave port, protecting any secure resource (register, register field) from a non-secure software access, with configurable interrupt event.
  - Two secure and non-secure interrupt requests, resulting from any of the respectively secure and non-secure channels. Each channel event being caused from any of the two DMAMUX input events: trigger or synchronization overrun, associated with a respectively secure and non-secure channels.
- Privileged / Unprivileged support:
  - Support for AHB privileged and unprivileged DMA transfers, independently, at a channel level.
  - Privileged-aware AHB slave port.

3.17 Interrupts and events

3.17.1 Nested vectored interrupt controller (NVIC)

The devices embed a nested vectored interrupt controller which is able to manage 8 priority levels, and to handle up to 109 maskable interrupt channels plus the 16 interrupt lines of the Cortex®-M33.

The NVIC benefits are the following:

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead
- TrustZone support. The NVIC registers are banked across secure and non-secure states

The NVIC hardware block provides flexible interrupt management features with minimal interrupt latency.

3.17.2 Extended interrupt/event controller (EXTI)

The Extended interrupts and event controller (EXTI) manages the individual CPU and system wakeup through configurable and direct event inputs. It provides wakeup requests to the power control, and generates an interrupt request to the CPU NVIC and events to the CPU event input. For the CPU an additional Event Generation block (EVG) is needed to generate the CPU event signal.

The EXTI wakeup requests allow the system to be woken up from Stop modes.

The interrupt request and event request generation can also be used in RUN modes. The EXTI also includes the EXTI mux IOport selection.

The EXTI main features are the following:

The EXTI main features are the following:

- 43 input events supported
- All event inputs allow to wake up the system.
- Events which do not have an associated wakeup flag in the peripheral, have a flag in the EXTI and generate an interrupt to the CPU from the EXTI.

The asynchronous event inputs are classified in 2 groups:

- Configurable events (signals from I/Os or peripherals able to generate a pulse)
  - Configurable events have the following features:
    Selectable active trigger edge
    Interrupt pending status register bit independent for the rising and falling edge.
    Individual interrupt and event generation mask, used for conditioning the CPU wakeup, interrupt and event generation.
    SW trigger possibility
- Direct events (interrupt and wakeup sources from peripherals having an associated flag which requiring to be cleared in the peripheral)
  - Direct events have the following features:
    Fixed rising edge active trigger
    No interrupt pending status register bit in the EXTI. (The interrupt pending status flag is provided by the peripheral generating the event.)
    Individual interrupt and event generation mask, used for conditioning the CPU wakeup and event generation.
    No SW trigger possibility
- TrustZone secure events
  - The access to control and configuration bits of secure input events can be made secure.
- EXTI IO port selection

3.18 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator with polynomial value and size.

Among other applications, the CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a mean to verify the Flash memory integrity.

The CRC calculation unit helps to compute a signature of the software during runtime, which can be ulteriorly compared with a reference signature generated at link-time and which can be stored at a given memory location.

3.19 Flexible static memory controller (FSMC)

The flexible static memory controller (FSMC) includes two memory controllers:

- The NOR/PSRAM memory controller
- The NAND/memory controller

This memory controller is also named flexible memory controller (FMC).

The main features of the FSMC controller are the following:

- Interface with static-memory mapped devices including:
  - Static random access memory (SRAM)
  - NOR Flash memory/OneNAND Flash memory
  - PSRAM (four memory banks)
  - NAND Flash memory with ECC hardware to check up to 8 Kbytes of data
  - Ferroelectric RAM (FRAM)
- 8-,16- bit data bus width
- Independent chip select control for each memory bank
- Independent configuration for each memory bank
- Write FIFO

LCD parallel interface

The FMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes, and is flexible enough to adapt to specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost effective graphic applications using LCD modules with embedded controllers or high-performance solutions using external controllers with dedicated acceleration.

TrustZone security

When the TrustZone security is enabled, the whole FSMC banks are secure after reset. Non-secure area can be configured using the TZSC MPCWMx controller.

- The FSMC NOR/PSRAM bank:
  - Up to two non-secure area can be configured thought the TZSC MPCWM2 controller with a granularity of 64 Kbytes.
- The FSMC NAND bank:
  - Can be either configured as fully secure or fully non-secure using the TZSC MPCWM3 controller.

The FSMC registers can be configured as secure through the TZSC controller.

3.20 Octo-SPI interface (OCTOSPI)

The OCTOSPI is a specialized communication interface targetting single, dual, quad or octal SPI memories. It can operate in any of the three following modes:

- Indirect mode: all the operations are performed using the OCTOSPI registers
- Status polling mode: the external memory status register is periodically read and an interrupt can be generated in case of flag setting
- Memory-mapped mode: the external memory is memory mapped and is seen by the system as if it were an internal memory supporting read and write operation

The OCTOSPI supports two frame formats:

- Classical frame format with command, address, alternate byte, dummy cycles and data phase over 1, 2, 4 or 8 data pins
- HyperBus™ frame format

The OCTOSPI offers the following features:

- Three functional modes: indirect, status-polling, and memory-mapped
- Read and write support in memory-mapped mode
- Supports for single, dual, quad and octal communication
- Dual-quad mode, where 8 bits can be sent/received simultaneously by accessing two quad memories in parallel.
- SDR and DTR support
- Data strobe support
- Fully programmable opcode for both indirect and memory mapped mode
- Fully programmable frame format for both indirect and memory mapped mode
- Each of the five following phases can be configured independently (enable, length, single/dual/quad communication)
  - Instruction phase
  - Address phase
  - Alternate bytes phase
  - Dummy cycles phase
  - Data phase
- HyperBus™ support
- Integrated FIFO for reception and transmission
- 8, 16, and 32-bit data accesses are allowed
- DMA channel for indirect mode operations
- Timeout management
- Interrupt generation on FIFO threshold, timeout, status match, operation complete, and access error

TrustZone security

When the TrustZone security is enabled, the whole OCTOSPI bank is secure after reset.

Up to two non-secure area can be configured thought the TZSC MPCWM1 controller with a granularity of 64 Kbytes.

The OCTOSPI registers can be configured as secure through the TZSC controller.

3.21 Analog-to-digital converter (ADC)

The device embeds two successive approximation analog-to-digital converters with the following features:

- 12-bit native resolution, with built-in calibration
- 5.33 Msps maximum conversion rate with full resolution
  - Down to 18.75 ns sampling time
  - Increased conversion rate for lower resolution (up to 8.88 Msps for 6-bit resolution)
- Up to 16 external channels
- 5 internal channels: internal reference voltage, temperature sensor, VBAT/3 and DAC1 outputs
- One external reference pin is available on some package, allowing the input voltage range to be independent from the power supply
- Single-ended and differential mode inputs
- Low-power design
  - Capable of low-current operation at low conversion rate (consumption decreases linearly with speed)
  - Dual clock domain architecture: ADC speed independent from CPU frequency
- Highly versatile digital interface
  - Single-shot or continuous/discontinuous sequencer-based scan mode: 2 groups of analog signals conversions can be programmed to differentiate background and high-priority real-time conversions
  - Each ADC support multiple trigger inputs for synchronization with on-chip timers and external signals
  - Results stored into a data register or in RAM with DMA controller support
  - Data pre-processing: left/right alignment and per channel offset compensation
  - Built-in oversampling unit for enhanced SNR
  - Channel-wise programmable sampling time
  - Analog watchdog for automatic voltage monitoring, generating interrupts and trigger for selected timers
  - Hardware assistant to prepare the context of the injected channels to allow fast context switching

3.21.1 Temperature sensor

The temperature sensor (TS) generates a voltage V_{TS} that varies linearly with temperature. The temperature sensor is internally connected to the ADC1_IN17 input channels which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode.

Table 14. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at a temperature of 30 °C (± 5 °C), $V_{DDA} = V_{REF+}$ = 3.0 V (± 10 mV)	0x0BFA 05A8 - 0x0BFA 05A9
TS_CAL2	TS ADC raw data acquired at a temperature of 130 °C (± 5 °C), $V_{DDA} = V_{REF+}$ = 3.0 V (± 10 mV)	0x0BFA 05CA- 0x0BFA 05CB

3.21.2 Internal voltage reference (V_{REFINT})

The internal voltage reference (VREFINT) provides a stable (bandgap) voltage output for the ADC and the comparators. The VREFINT is internally connected to the ADC1_IN0 input channel. The precise voltage of VREFINT is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

Table 15. Internal voltage reference calibration values

Calibration value name	Description	Memory address
VREFINT	Raw data acquired at a temperature of 30 °C (± 5 °C), $V_{DDA} = V_{REF+}$ = 3.0 V (± 10 mV)	0x0BFA 05AA - 0x0BFA 05AB

3.21.3 V_{BAT} battery voltage monitoring

This embedded hardware enables the application to measure the V_{BAT} battery voltage using the internal ADC channel ADC1_IN18. As the V_{BAT} voltage may be higher than the VDDA, and thus outside the ADC input range, the VBAT pin is internally connected to a bridge divider by 3. As a consequence, the converted digital value is one third of the V_{BAT} voltage.

3.22 Digital to analog converter (DAC)

Two 12-bit buffered DAC channels can be used to convert digital signals into analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in inverting configuration.

This digital interface supports the following features:

- Up to two DAC output channels
- 8-bit or 12-bit output mode
- Buffer offset calibration (factory and user trimming)
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation
- Dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- External triggers for conversion
- Sample and hold low-power mode, with internal or external capacitor

The DAC channels are triggered through the timer update outputs that are also connected to different DMA channels.

3.23 Voltage reference buffer (VREFBUF)

The devices embed a voltage reference buffer which can be used as voltage reference for ADC, DACs and also as voltage reference for external components through the VREF+ pin.

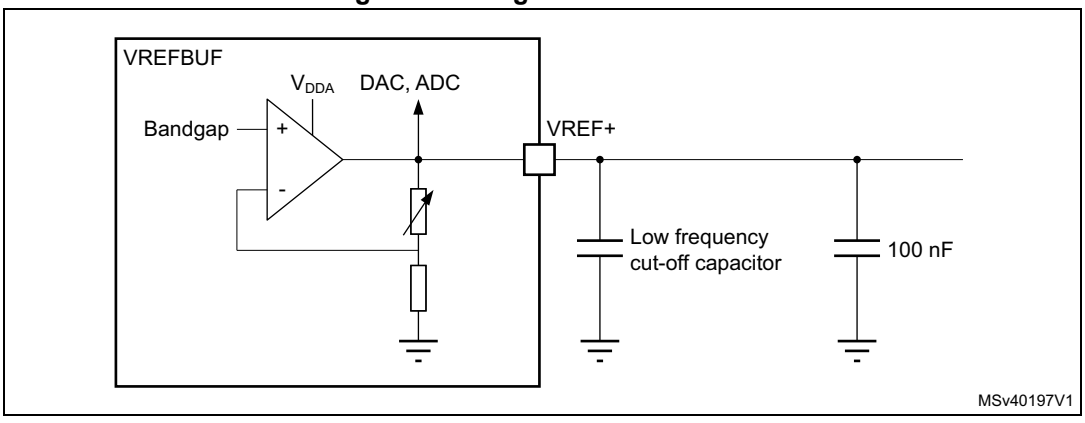
The internal voltage reference buffer supports two voltages:

- 2.048 V
- 2.5 V

An external voltage reference can be provided through the VREF+ pin when the internal voltage reference buffer is off.

The VREF+ pin is double-bonded with VDDA on some packages. In these packages the internal voltage reference buffer is not available.

Figure 9. Voltage reference buffer



3.24 Comparators (COMP)

The devices embed two rail-to-rail comparators with programmable reference voltage (internal or external), hysteresis and speed (low speed for low-power) and with selectable output polarity.

The reference voltage can be one of the following:

- External I/O
- DAC output channels
- Internal reference voltage or submultiple (1/4, 1/2, 3/4).

All comparators can wake up from Stop mode, generate interrupts and breaks for the timers and can also be combined into a window comparator.

3.25 Operational amplifier (OPAMP)

The devices embed two operational amplifiers with external or internal follower routing and PGA capability.

The operational amplifier features:

- Low input bias current
- Low offset voltage
- Low-power mode
- Rail-to-rail input

3.26 Digital filter for sigma-delta modulators (DFSDM)

The devices embed one DFSDM with four digital filters modules and eight external input serial channels (transceivers) or alternately eight internal parallel inputs support.

The DFSDM peripheral is dedicated to interface the external ΣΔ modulators to the microcontroller and then to perform digital filtering of the received data streams (which represent analog value on ΣΔ modulators inputs).

The DFSDM can also interface the PDM (pulse density modulation) microphones and perform PDM to PCM conversion and filtering in hardware. The DFSDM features optional parallel data stream inputs from microcontrollers memory (through DMA/CPU transfers into DFSDM).

The DFSDM transceivers support several serial interface formats (to support various ΣΔ modulators) and the DFSDM digital filter modules perform digital processing according to the user's selected filter parameters with up to 24-bit final ADC resolution.

The DFSDM peripheral supports:

- Up to 4 multiplexed input digital serial channels:
  - Configurable SPI interface to connect various ΣΔ modulators
  - Configurable Manchester coded 1 wire interface support
  - Clock output for ΣΔ modulator(s)
- Alternative inputs from up to 4 internal digital parallel channels:
  - Inputs with up to 16 bit resolution
  - Internal sources: ADCs data or memory (CPU/DMA write) data streams
- Adjustable digital signal processing:
  - Sincx filter: filter order/type (1..5), oversampling ratio (up to 1..1024)
  - Integrator: oversampling ratio (1..256)
- Up to 24-bit output data resolution:
  - Right bit-shifter on final data (0..31 bits)
- Signed output data format
- Automatic data offset correction (offset stored in register by user)
- Continuous or single conversion
- Start-of-conversion synchronization with:
  - Software trigger
  - Internal timers
  - External events
  - Start-of-conversion synchronously with first DFSDM filter (DFSDM_FLT0)
- Analog watchdog feature:
  - Low value and high value data threshold registers
  - Own configurable Sincx digital filter (order = 1..3, oversampling ratio = 1..32)
  - Input from output data register or from one or more input digital serial channels
  - Continuous monitoring independently from standard conversion
- Short-circuit detector to detect saturated analog input values (bottom and top ranges):
  - Up to 8-bit counter to detect 1..256 consecutive 0’s or 1’s on input data stream
  - Mnitoring continuously each channel (4 serial channel transceiver outputs)
- Break generation on analog watchdog event or short-circuit detector event
- Extremes detector:
  - Store minimum and maximum values of output data values
  - Refreshed by software
- DMA may be used to read the conversion data
- Interrupts: end of conversion, overrun, analog watchdog, short-circuit, channel clock absence
- “Regular” or “injected” conversions:
  - “Regular” conversions can be requested at any time or even in continuous mode without having any impact on the timing of “injected” conversions.

3.27 Touch sensing controller (TSC)

The touch sensing controller provides a simple solution to add capacitive sensing functionality to any application. A capacitive sensing technology is able to detect finger presence near an electrode that is protected from direct touch by a dielectric (glass, plastic or other). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle.

The touch sensing controller is fully supported by the STMTouch touch sensing firmware library which is free to use and allows touch sensing functionality to be implemented reliably in the end application.

The main features of the touch sensing controller are the following:

- Proven and robust surface charge transfer acquisition principle
- Supports up to 22 capacitive sensing channels
- Up to 3 capacitive sensing channels can be acquired in parallel offering a very good response time
- Spread spectrum feature to improve system robustness in noisy environments
- Full hardware management of the charge transfer acquisition sequence
- Programmable charge transfer frequency
- Programmable sampling capacitor I/O pin
- Programmable channel I/O pin
- Programmable max count value to avoid long acquisition when a channel is faulty
- Dedicated end of acquisition and max count error flags with interrupt capability
- One sampling capacitor for up to 3 capacitive sensing channels to reduce the system components
- Compatible with proximity, touchkey, linear and rotary touch sensor implementation
- Designed to operate with STMTouch touch sensing firmware library

Note: The number of capacitive sensing channels is dependent on the size of the packages and subject to I/O availability.

3.28 True random number generator (RNG)

The RNG is a true random number generator that provides full entropy outputs to the application as 32-bit samples. It is composed of a live entropy source (analog) and an internal conditioning component.

The RNG is a NIST SP 800-90B compliant entropy source that can be used to construct a non-deterministic random bit generator (NDRBG).

The true random number generator:

- delivers 32-bit true random numbers, produced by an analog entropy source conditioned by a NIST SP800-90B approved conditioning stage,
- can be used as entropy source to construct a non-deterministic random bit generator (NDRBG),
- produces four 32-bit random samples every 412 AHB clock cycles if fAHB < 77 MHz (256 RNG clock cycles otherwise),
- embeds start-up and NIST SP800-90B approved continuous health tests (repetition count and adaptive proportion tests), associated with specific error management,
- can be disabled to reduce power consumption, or enabled with an automatic low-power mode (default configuration),
- has an AMBA AHB slave peripheral, accessible through 32-bit word single accesses only (else an AHB bus error is generated, and the write accesses are ignored).

3.29 HASH hardware accelerator (HASH)

The hash processor is a fully compliant implementation of the secure hash algorithm (SHA-1, SHA-224, SHA-256), the MD5 (message-digest algorithm 5) hash algorithm and the HMAC (keyed-hash message authentication code) algorithm suitable for a variety of applications.

It computes a message digest (160 bits for the SHA-1 algorithm, 256 bits for the SHA-256 algorithm and 224 bits for the SHA-224 algorithm,128 bits for the MD5 algorithm) for messages of up to (264 - 1) bits, while the HMAC algorithms provide a way of authenticating messages by means of hash functions. The HMAC algorithms consist in calling the SHA-1, SHA-224, SHA-256 or MD5 hash function twice.

3.30 Timers and watchdogs

The devices include two advanced control timers, up to nine general-purpose timers, two basic timers, two low-power timers, two watchdog timers and a SysTick timer.

Table 16 compares the features of the advanced control, general-purpose and basic timers.

Table 16. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complementary outputs
Advanced control	TIM1, TIM8	16-bit	Up, down, Up/down	Any integer between 1 and 65536	Yes	4	3
General-purpose	TIM2, TIM5	32-bit	Up, down, Up/down	Any integer between 1 and 65536	Yes	4	No
General-purpose	TIM3, TIM4	16-bit	Up, down, Up/down	Any integer between 1 and 65536	Yes	4	No
General-purpose	TIM15	16-bit	Up	Any integer between 1 and 65536	Yes	2	1
General-purpose	TIM16, TIM17	16-bit	Up	Any integer between 1 and 65536	Yes	1	1
Basic	TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

3.30.1 Advanced-control timer (TIM1, TIM8)

The advanced-control timers can each be seen as a three-phase PWM multiplexed on six channels. They have complementary PWM outputs with programmable inserted dead-times. They can also be seen as complete general-purpose timers.

The four independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes) with full modulation capability (0-100%)
- One-pulse mode output

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled in order to turn off any power switches driven by these outputs.

Many features are shared with the general-purpose TIMx timers (described in *Section 3.30.2*) using the same architecture, so the advanced-control timers can work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

3.30.2 General-purpose timers (TIM2, TIM3, TIM4, TIM5, TIM15, TIM16, TIM17)

There are up to seven synchronizable general-purpose timers embedded in the STM32L552xx devices (see *Table 16* for differences).
Each general-purpose timer can be used to generate PWM outputs, or act as a simple time base.

- TIM2, TIM3, TIM4 and TIM5

  They are full-featured general-purpose timers:

  – TIM2 and TIM5 have a 32-bit auto-reload up/downcounter and 32-bit prescaler

  – TIM3 and TIM4 have 16-bit auto-reload up/downcounter and 16-bit prescaler.

  These timers feature four independent channels for input capture/output compare, PWM or one-pulse mode output. They can work together, or with the other general-purpose timers via the Timer Link feature for synchronization or event chaining.

  The counters can be frozen in debug mode.

  All have independent DMA request generation and support quadrature encoders.

- TIM15, 16 and 17

  They are general-purpose timers with mid-range features:

  They have 16-bit auto-reload upcounters and 16-bit prescalers.

  – TIM15 has two channels and one complementary channel

  – TIM16 and TIM17 have one channel and one complementary channel

  All channels can be used for input capture/output compare, PWM or one-pulse mode output.

  The timers can work together via the Timer Link feature for synchronization or event chaining. The timers have independent DMA request generation.

  The counters can be frozen in debug mode.

3.30.3 Basic timers (TIM6 and TIM7)

The basic timers are mainly used for DAC trigger generation. They can also be used as generic 16-bit timebases.

3.30.4 Low-power timers (LPTIM1, LPTIM2 and LPTIM3)

The devices embed two low-power timers. These timers have an independent clock and are running in Stop mode if they are clocked by LSE, LSI or an external clock. They are able to wakeup the system from Stop mode.

LPTIM1 and LPTIM3 are active in Stop 0, Stop 1 and Stop 2 modes.

LPTIM2 is active in Stop 0 and Stop 1 mode.

This low-power timer supports the following features:

- 16-bit up counter with 16-bit autoreload register
- 16-bit compare register
- Configurable output: pulse, PWM
- Continuous/ one shot mode
- Selectable software/hardware input trigger
- Selectable clock source
  - Internal clock sources: LSE, LSI, HSI16 or APB clock
  - External clock source over LPTIM input (working even with no internal clock source running, used by pulse counter application).
- Programmable digital glitch filter
- Encoder mode (LPTIM1 only).

3.30.5 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and an 8-bit prescaler. It is clocked from an independent 32 kHz internal RC (LSI) and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

3.30.6 Window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.30.7 SysTick timer

The Cortex®-M33 with TrustZone embeds two SysTick timers.

When TrustZone is activated, two SysTick timer are available:

- SysTick, Secure instance.
- SysTick, Non-secure instance.

When TrustZone is disabled, only one SysTick timer is available.

This timer (secure or non-secure) is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

3.31 Real-time clock (RTC)

The RTC supports the following features:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month.
- Two programmable alarms.
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Digital calibration circuit with 0.95 ppm resolution, to compensate for quartz crystal inaccuracy.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event, or by a switch to V_{BAT} mode.
- 17-bit auto-reload wakeup timer (WUT) for periodic events with programmable resolution and period.
- TrustZone support:
  - RTC fully securable
  - Alarm A, alarm B, wakeup Timer and timestamp individual secure or non-secure configuration

The RTC is supplied through a switch that takes power either from the V_{DD} supply when present or from the V_{BAT} pin.

The RTC clock sources can be:

- A 32.768 kHz external crystal (LSE)
- An external resonator or oscillator (LSE)
- The internal low power RC oscillator (LSI, with typical frequency of 32 kHz)
- The high-speed external clock (HSE), divided by a prescaler in the RCC.

The RTC is functional in VBAT mode and in all low-power modes when it is clocked by the LSE. When clocked by the LSI, the RTC is not functional in VBAT mode, but is functional in all low-power modes except Shutdown mode.

All RTC events (Alarm, WakeUp Timer, Timestamp) can generate an interrupt and wakeup the device from the low-power modes.

3.32 Tamper and backup registers (TAMP)

32 32-bit backup registers are retained in all low-power modes and also in VBAT mode. They can be used to store sensitive data as their content is protected by an tamper detection circuit. 8 tamper pins and 7 internal tampers are available for anti-tamper detection.

The external tamper pins can be configured for edge detection, or level detection with or without filtering, or active tamper which increases the security level by auto checking that the tamper pins are not externally opened or shorted.

TAMP main features:

- 32 backup registers:
  - The backup registers (TAMP_BKPxR) are implemented in the RTC domain that remains powered-on by VBAT when the VDD power is switched off
- 8 external tamper detection events
  - Each external event can be configured to be active or passive
  - External passive tampers with configurable filter and internal pull-up
- 5 internal tamper events
- Any tamper detection can generate a RTC timestamp event
- Any tamper detection can erase the backup registers
- TrustZone support:
  - Tamper secure or non-secure configuration.
  - Backup registers configuration in 3 configurable-size areas:
    1 read/write secure area
    1 write secure/read non-secure area
    1 read/write non-secure area
- Monotonic counter.

3.33 Inter-integrated circuit interface (I2C)

The device embeds four I2C. Refer to *Table 17: I2C implementation* for the features implementation.

The I^2C bus interface handles communications between the microcontroller and the serial I^2C bus. It controls all I^2C bus-specific sequencing, protocol, arbitration and timing.

The I2C peripheral supports:

- I^2C-bus specification and user manual rev. 5 compatibility:
  - Slave and master modes, multimaster capability
  - Standard-mode (Sm), with a bitrate up to 100 kbit/s
  - Fast-mode (Fm), with a bitrate up to 400 kbit/s
  - Fast-mode plus (Fm+), with a bitrate up to 1 Mbit/s and 20 mA output drive I/Os
  - 7-bit and 10-bit addressing mode, multiple 7-bit slave addresses
  - Programmable setup and hold times
  - Optional clock stretching
- System management bus (SMBus) specification rev 2.0 compatibility:
  - Hardware PEC (packet error checking) generation and verification with ACK control
  - Address resolution protocol (ARP) support
  - SMBus alert
- Power system management protocol (PMBus™) specification rev 1.1 compatibility
- Independent clock: a choice of independent clock sources allowing the I2C communication speed to be independent from the PCLK reprogramming. Refer to *Figure 7: STM32L552xx clock tree*
- Wakeup from Stop mode on address match
- Programmable analog and digital noise filters
- 1-byte buffer with DMA capability

Table 17. I2C implementation

I2C features(1)	I2C1	I2C2	I2C3	I2C4
Standard-mode (up to 100 kbit/s)	X	X	X	X
Fast-mode (up to 400 kbit/s)	X	X	X	X
Fast-mode Plus with 20 mA output drive I/Os (up to 1 Mbit/s)	X	X	X	X
Programmable analog and digital noise filters	X	X	X	X
SMBus/PMBus hardware support	X	X	X	X
Independent clock	X	X	X	X
Wakeup from Stop 0, Stop 1 mode on address match	X	X	X	X
Wakeup from Stop 2 mode on address match	-	-	X	-

1. X: supported

3.34 Universal synchronous/asynchronous receiver transmitter (USART)

The devices have three embedded universal synchronous receiver transmitters (USART1, USART2 and USART3) and two universal asynchronous receiver transmitters (UART4, UART5).

These interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN master/slave capability. They provide hardware management of the CTS and RTS signals, and RS485 driver enable. They are able to communicate at speeds of up to 10 Mbit/s.

The USART1, USART2 and USART3 also provide a Smartcard mode (ISO 7816 compliant) and an SPI-like communication capability.

All USART have a clock domain independent from the CPU clock, allowing the USARTx (x=1,2,3,4,5) to wake up the MCU from Stop mode using baudrates up to 200 Kbaud. The wake up events from Stop mode are programmable and can be:

- Start bit detection
- Any received data frame
- A specific programmed data frame

All USART interfaces can be served by the DMA controller.

Table 18. USART/UART/LPUART features

USART modes/features(1)	USART1	USART2	USART3	UART4	UART5	LPUART1
Hardware flow control for modem	X	X	X	X	X	X
Continuous communication using DMA	X	X	X	X	X	X
Multiprocessor communication	X	X	X	X	X	X
Synchronous mode	X	X	X	-	-	-
Smartcard mode	X	X	X	-	-	-
Single-wire half-duplex communication	X	X	X	X	X	X
IrDA SIR ENDEC block	X	X	X	X	X	-
LIN mode	X	X	X	X	X	-
Dual clock domain	X	X	X	X	X	X
Wakeup from Stop 0 / Stop 1 modes	X	X	X	X	X	X
Wakeup from Stop 2 mode	-	-	-	-	-	X
Receiver timeout interrupt	X	X	X	X	X	-
Modbus communication	X	X	X	X	X	-
Auto baud rate detection	X (4 modes)					-
Driver enable	X	X	X	X	X	X
LPUART/USART data length	7, 8 and 9 bits					

1. X = supported.

3.35 Low-power universal asynchronous receiver transmitter (LPUART)

The devices embed one low-power UART. The LPUART supports asynchronous serial communication with minimum power consumption. It supports half-duplex single-wire communication and modem operations (CTS/RTS). It allows multiprocessor communication.

The LPUART has a clock domain independent from the CPU clock, and can wakeup the system from Stop mode using baudrates up to 220 Kbaud. The wake up events from Stop mode are programmable and can be:

- Start bit detection
- Any received data frame
- A specific programmed data frame

Only a 32.768 kHz clock (LSE) is needed to allow LPUART communication up to 9600 baud. Therefore, even in Stop mode, the LPUART can wait for an incoming frame while having an extremely low energy consumption. Higher speed clock can be used to reach higher baudrates.

The LPUART interface can be served by the DMA controller.

3.36 Serial peripheral interface (SPI)

Three SPI interfaces allow communication up to slave modes, in half-duplex, full-duplex and simplex modes. The 3-bit prescaler gives eight master mode frequencies and the frame size is configurable from 4 bits to 16 bits. The SPI interfaces support NSS pulse mode, TI mode and hardware CRC calculation.

All SPI interfaces can be served by the DMA controller.

3.37 Serial audio interfaces (SAI)

The devices embed two SAI. Refer to *Table 19: SAI implementation* for the features implementation. The SAI bus interface handles communications between the microcontroller and the serial audio protocol.

The SAI peripheral supports:

- Two independent audio sub-blocks which can be transmitters or receivers with their respective FIFO.
- 8-word integrated FIFOs for each audio sub-block.
- Synchronous or asynchronous mode between the audio sub-blocks.
- Master or slave configuration independent for both audio sub-blocks.
- Clock generator for each audio block to target independent audio frequency sampling when both audio sub-blocks are configured in master mode.
- Data size configurable: 8-, 10-, 16-, 20-, 24-, 32-bit.
- Peripheral with large configurability and flexibility allowing to target as example the following audio protocol: I2S, LSB or MSB-justified, PCM/DSP, TDM, AC’97 and SPDIF out.

- Up to 16 slots available with configurable size and with the possibility to select which ones are active in the audio frame.
- Number of bits by frame may be configurable.
- Frame synchronization active level configurable (offset, bit length, level).
- First active bit position in the slot is configurable.
- LSB first or MSB first for data transfer.
- Mute mode.
- Stereo/Mono audio frame capability.
- Communication clock strobing edge configurable (SCK).
- Error flags with associated interrupts if enabled respectively.
  - Overrun and underrun detection.
  - Anticipated frame synchronization signal detection in slave mode.
  - Late frame synchronization signal detection in slave mode.
  - Codec not ready for the AC'97 mode in reception.
- Interruption sources when enabled:
  - Errors.
  - FIFO requests.
- DMA interface with two dedicated channels to handle access to the dedicated integrated FIFO of each SAI audio sub-block.

Table 19. SAI implementation

SAI features(1)	SAI1	SAI2
I2S, LSB or MSB-justified, PCM/DSP, TDM, AC'97	X	X
Mute mode	X	X
Stereo/Mono audio frame capability.	X	X
16 slots	X	X
Data size configurable: 8-, 10-, 16-, 20-, 24-, 32-bit	X	X
FIFO size	X (8 Word)	X (8 Word)
SPDIF	X	X
PDM	X	-

1. X: supported

3.38 Secure digital input/output and MultiMediaCards Interface (SDMMC)

The SD/SDIO, MultiMediaCard (MMC) host interface (SDMMC) provides an interface between the AHB bus and SD memory cards, SDIO cards and MMC devices.

The SDMMC features include the following:

- Full compliance with MultiMediaCard System Specification Version 4.51. Card support for three different databus modes: 1-bit (default), 4-bit and 8-bit
- Full compatibility with previous versions of MultiMediaCards (backward compatibility)
- Full compliance with SD Memory Card Specifications Version 4.1. (SDR104 SDMMC_CK speed limited to maximum allowed IO speed, SPI mode and UHS-II mode not supported)
- Full compliance with SDIO Card Specification Version 4.0: card support for two different databus modes: 1-bit (default) and 4-bit. (SDR104 SDMMC_CK speed limited to maximum allowed IO speed, SPI mode and UHS-II mode not supported)
- Data transfer up to 104 Mbyte/s for the 8-bit mode (depending maximum allowed IO speed)
- Data and command output enable signals to control external bidirectional drivers.

3.39 Controller area network (FDCAN)

The controller area network (CAN) subsystem consists of one CAN modules and message RAM memory.

The CAN module (FDCAN) is compliant with ISO 11898-1 (CAN protocol specification version 2.0 part A, B) and CAN FD protocol specification version 1.0.

A 1 Kbyte message RAM memory implements filters, receive FIFOs, receive buffers, transmit event FIFOs, transmit buffers.

3.40 Universal serial bus (USB FS)

The devices embed a full-speed USB device peripheral compliant with the USB specification version 2.0. The internal USB PHY supports USB FS signaling, embedded DP pull-up and battery charging detection according to Battery Charging Specification Revision 1.2.

The USB interface implements a full-speed (12 Mbit/s) function interface with added support for USB 2.0 link power management. It has software-configurable endpoint setting with packet memory up-to 1 Kbyte and suspend/resume support.

This interface requires a precise 48 MHz clock which can be generated from the internal main PLL (the clock source must use a HSE crystal oscillator) or by the internal 48 MHz oscillator (HSI48) in automatic trimming mode. The synchronization for this oscillator can be taken from the USB data stream itself (SOF signalization) which allows crystal less operation.

3.41 USB Type-C™ / USB Power Delivery controller (UCPD)

The device embeds one controller (UCPD) compliant with USB Type-C Rev. 1.2 and USB Power Delivery Rev. 3.0 specifications.

The controller uses specific I/Os supporting the USB Type-C and USB Power Delivery requirements, featuring:

- USB Type-C pull-up (Rp, all values) and pull-down (Rd) resistors
- “Dead battery” support
- USB Power Delivery message transmission and reception
- FRS (fast role swap) support

The digital controller handles notably:

- USB Type-C level detection with debounce, generating interrupts
- FRS detection, generating an interrupt
- Byte-level interface for USB Power Delivery payload, generating interrupts (DMA compatible)
- USB Power Delivery timing dividers (including a clock pre-scaler)
- CRC generation/checking
- 4b5b encode/decode
- Ordered sets (with a programmable ordered set mask at receive)
- Frequency recovery in receiver during preamble

The interface offers low-power operation compatible with Stop mode, maintaining the capacity to detect incoming USB Power Delivery messages and FRS signaling.

3.42 Development support

3.42.1 Serial wire JTAG debug port (SWJ-DP)

The Arm® SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

Debug is performed using two pins only instead of five required by the JTAG (JTAG pins could be re-used as GPIO with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

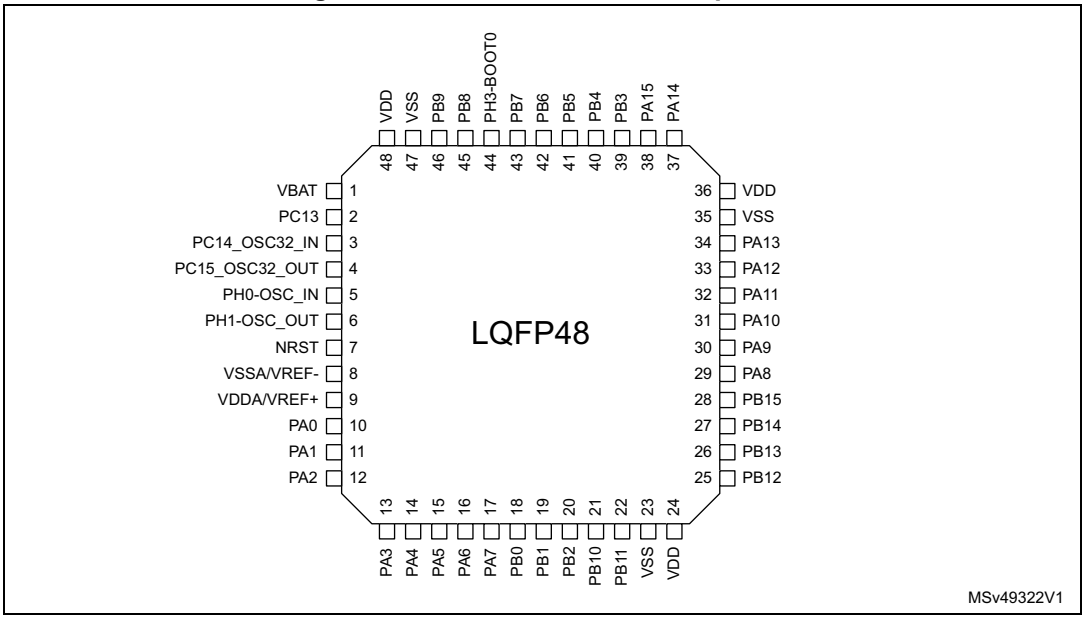
3.42.2 Embedded Trace Macrocell™

The Arm® Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the devices through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. Real-time instruction and data flow activity be recorded and then formatted for display on the host computer that runs the debugger software. TPA hardware is commercially available from common development tool vendors.

The Embedded Trace Macrocell operates with third party debugger software tools.

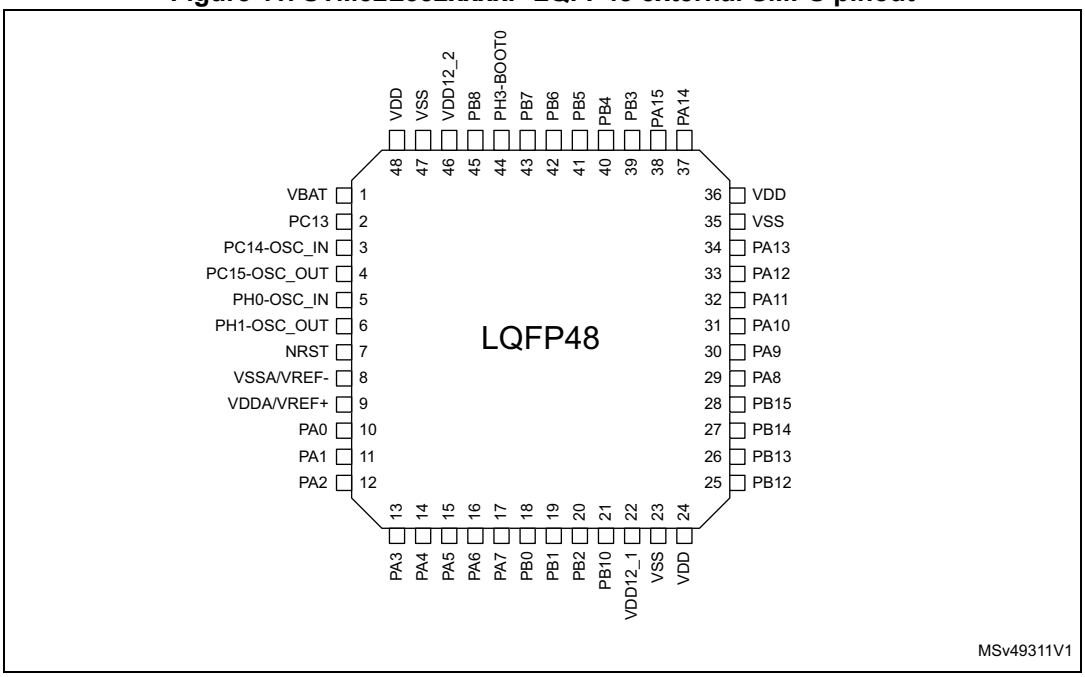
4 Pinouts and pin description

Figure 10. STM32L552xx LQFP48 pinout



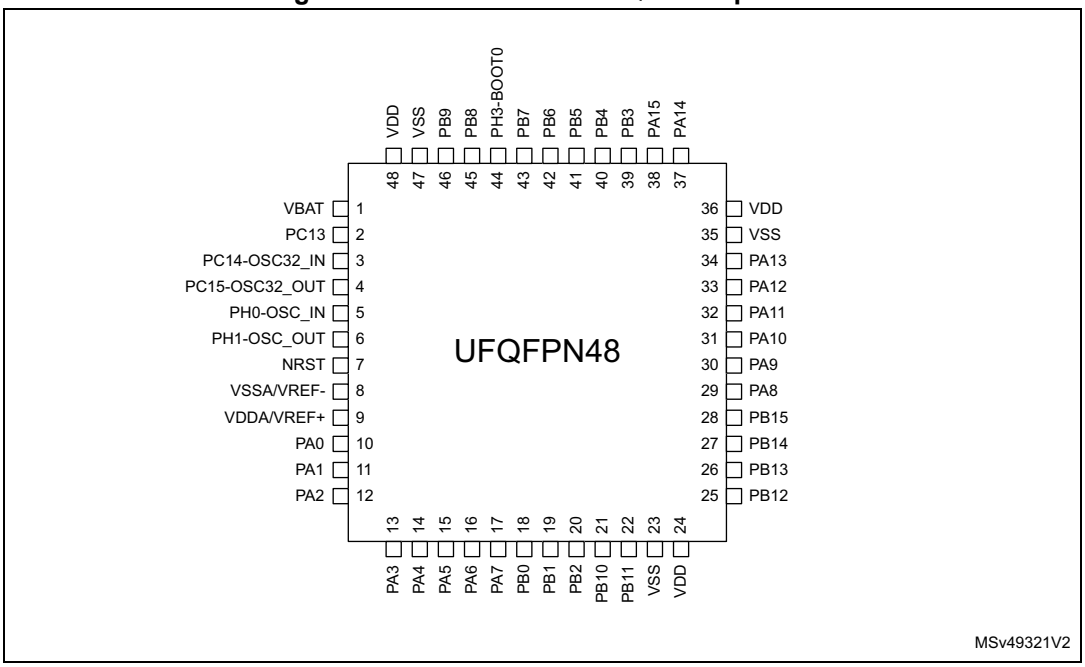
1. The above figure shows the package top view.

Figure 11. STM32L552xxxxP LQFP48 external SMPS pinout



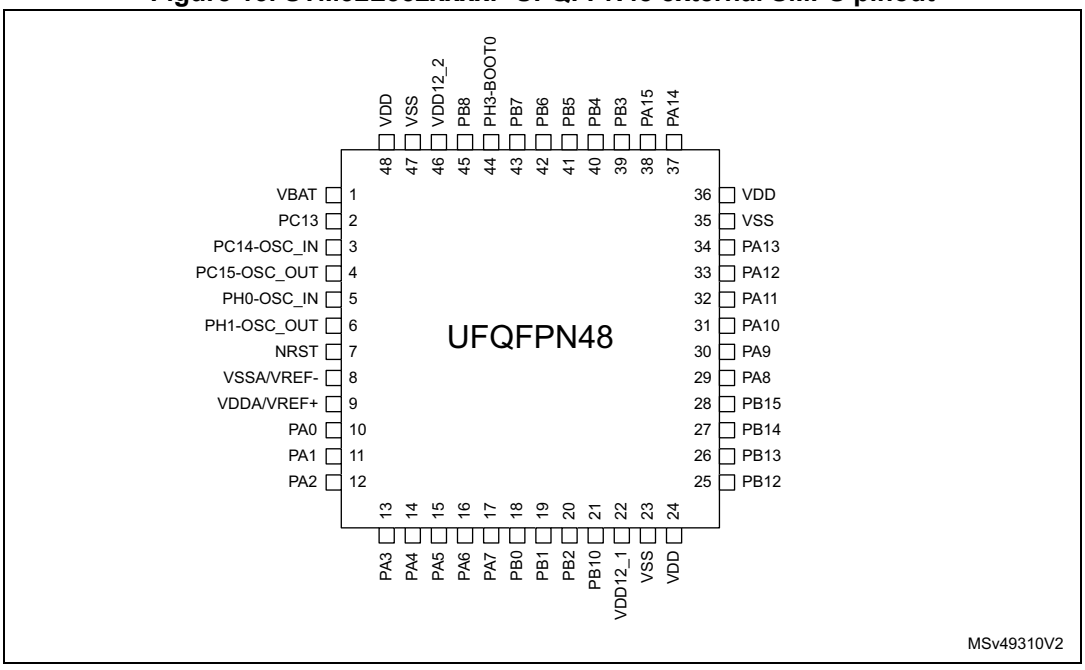
1. The above figure shows the package top view.

Figure 12. STM32L552xx UFQFPN48 pinout



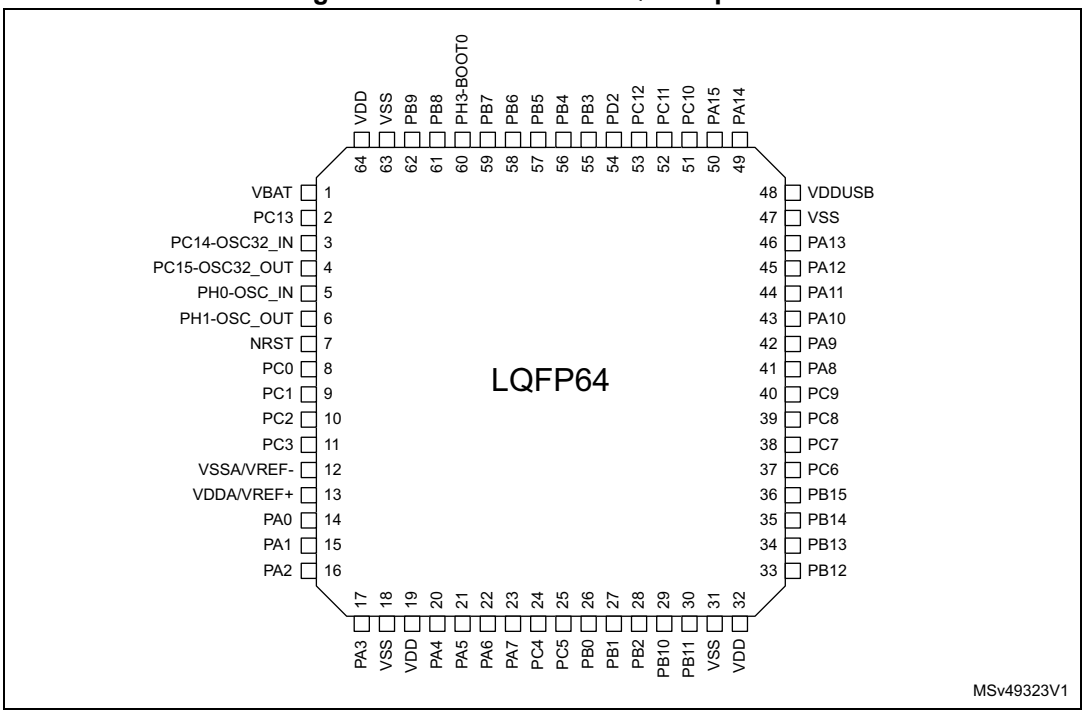
1. The above figure shows the package top view.

Figure 13. STM32L552xxxxP UFQFPN48 external SMPS pinout



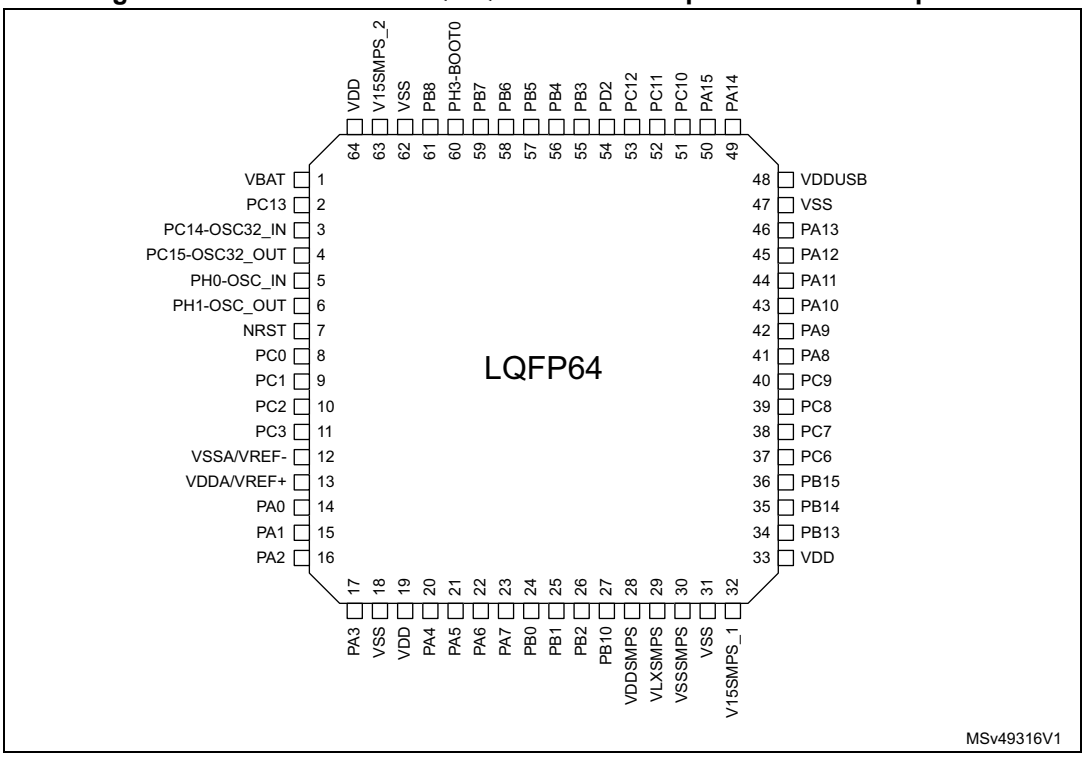
1. The above figure shows the package top view.

Figure 14. STM32L552xx LQFP64 pinout



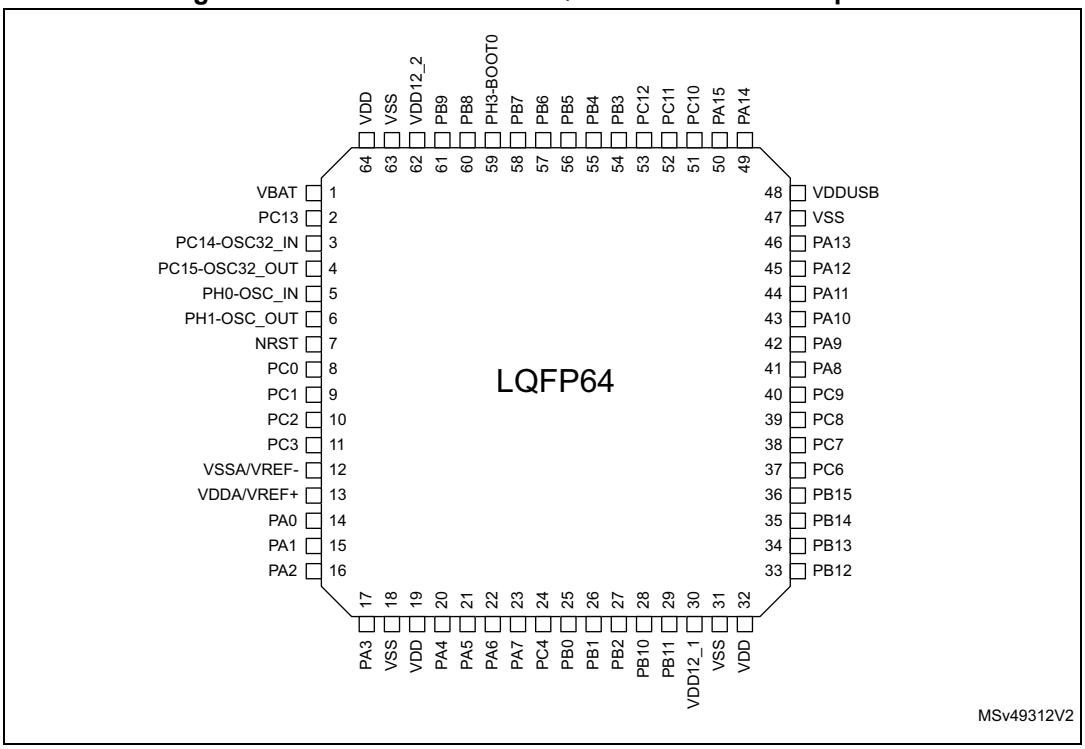
1. The above figure shows the package top view.

Figure 15. STM32L552xxxxQ LQFP64 SMPS step down converter pinout



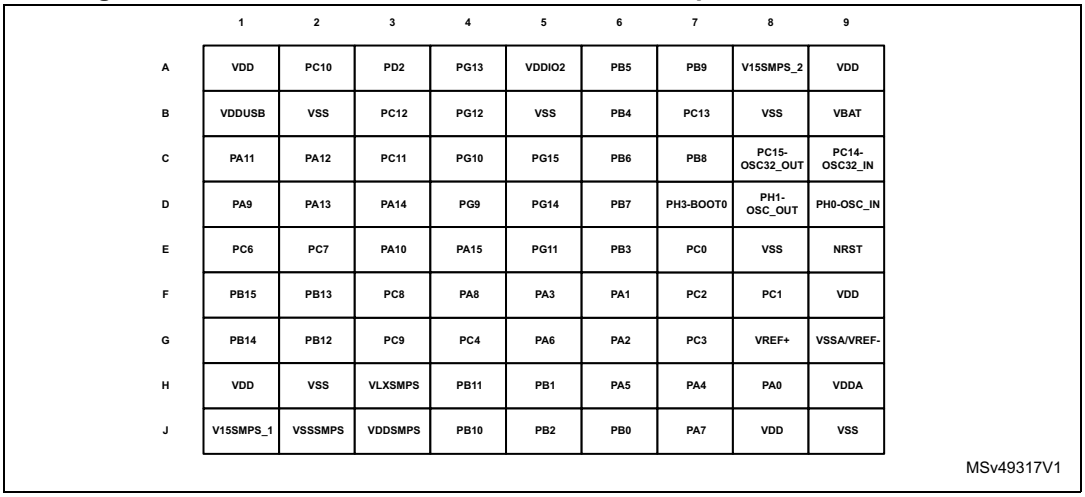
1. The above figure shows the package top view.

Figure 16. STM32L552xxxxP LQFP64 external SMPS pinout



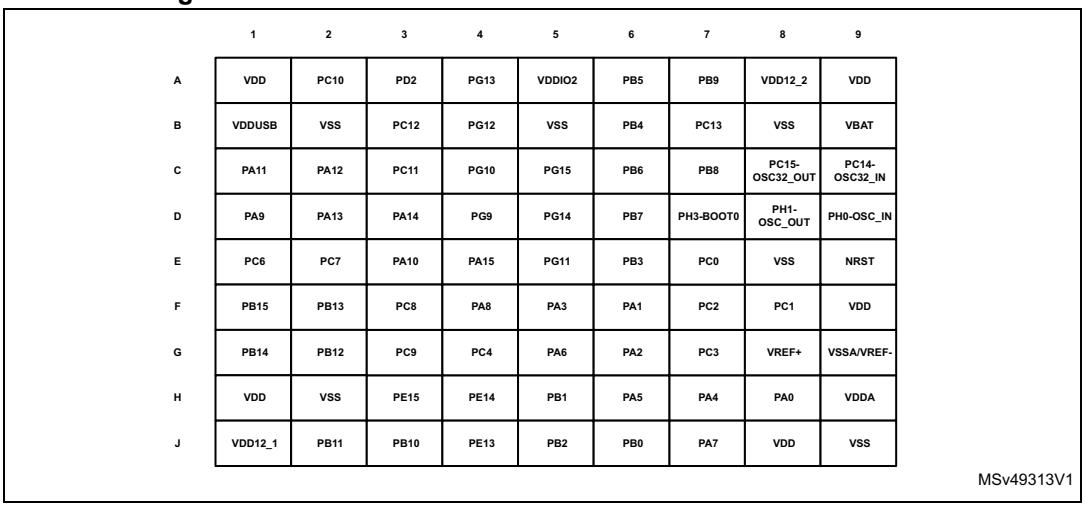
1. The above figure shows the package top view.

Figure 17. STM32L552xxxxQ WLCSP81 SMPS step down converter ballout



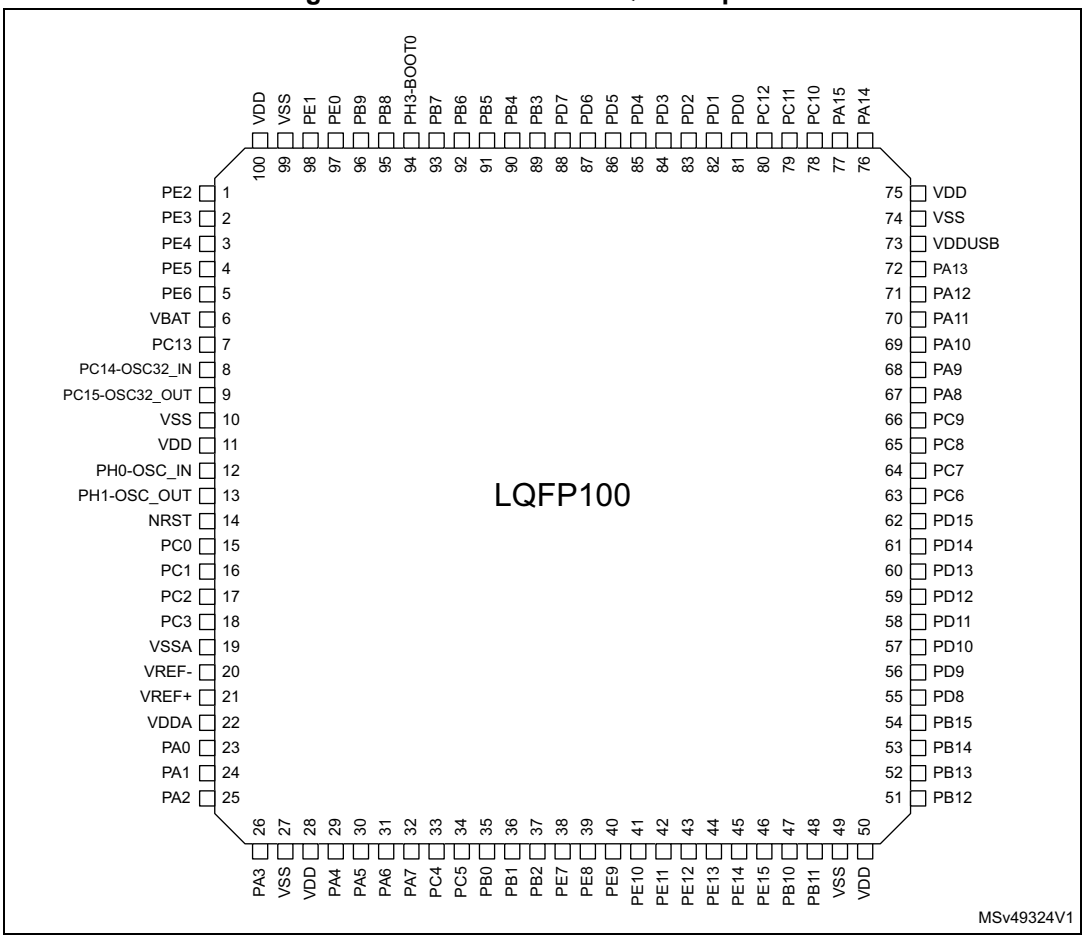
1. The above figure shows the package top view.

Figure 18. STM32L552xxxxP WLCSP81 external SMPS ballout



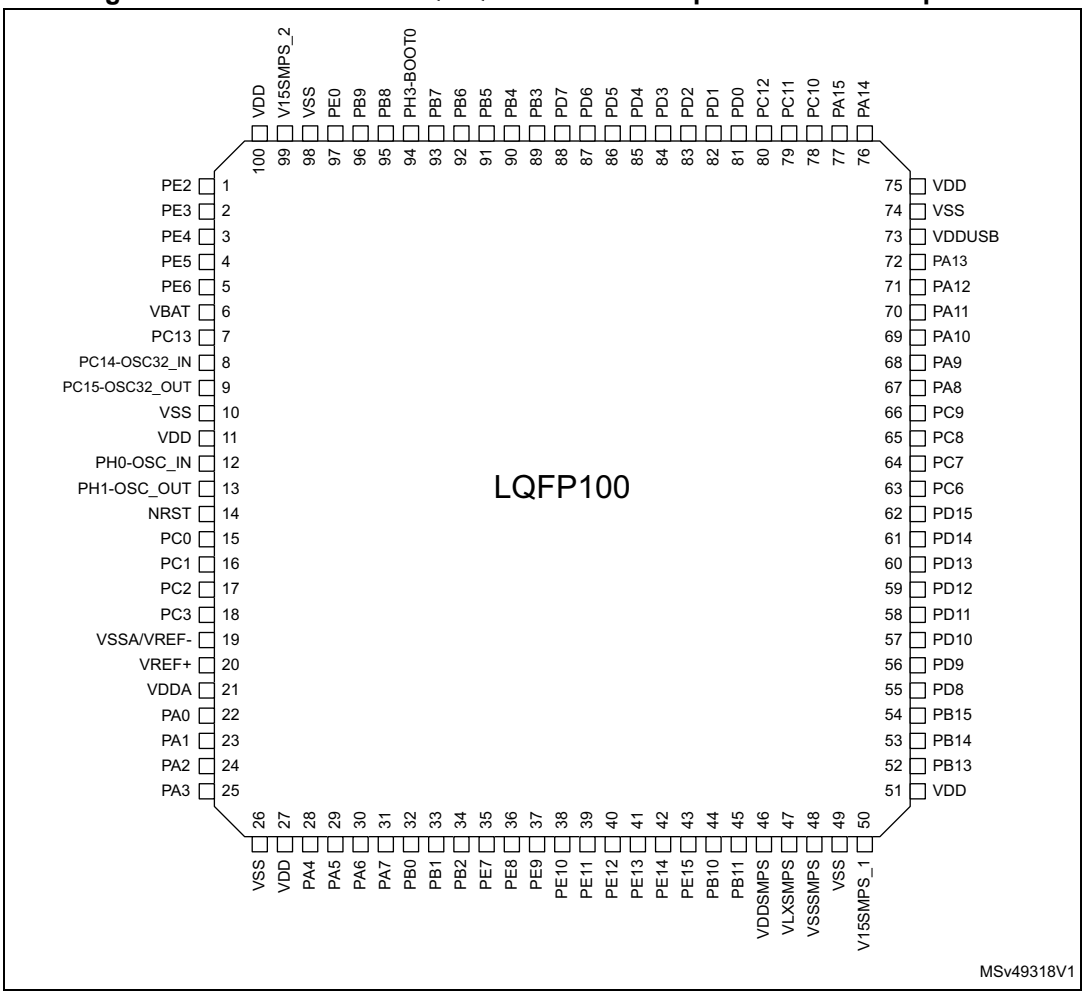
1. The above figure shows the package top view.

Figure 19. STM32L552xx LQFP100 pinout



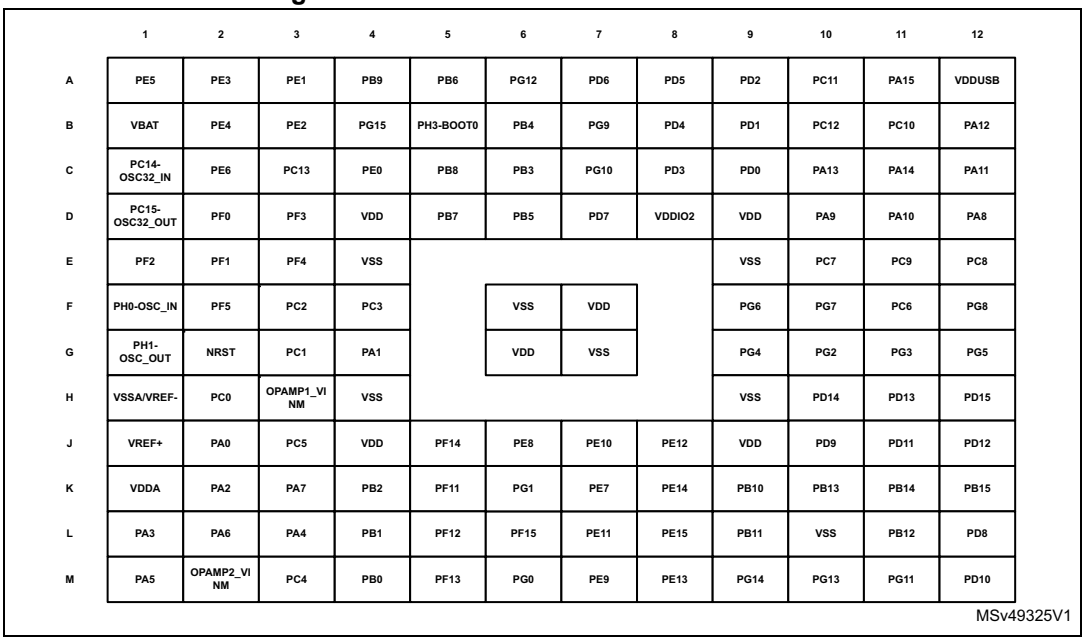
1. The above figure shows the package top view.

Figure 20. STM32L552xxxxQ LQFP100 SMPS step down converter pinout



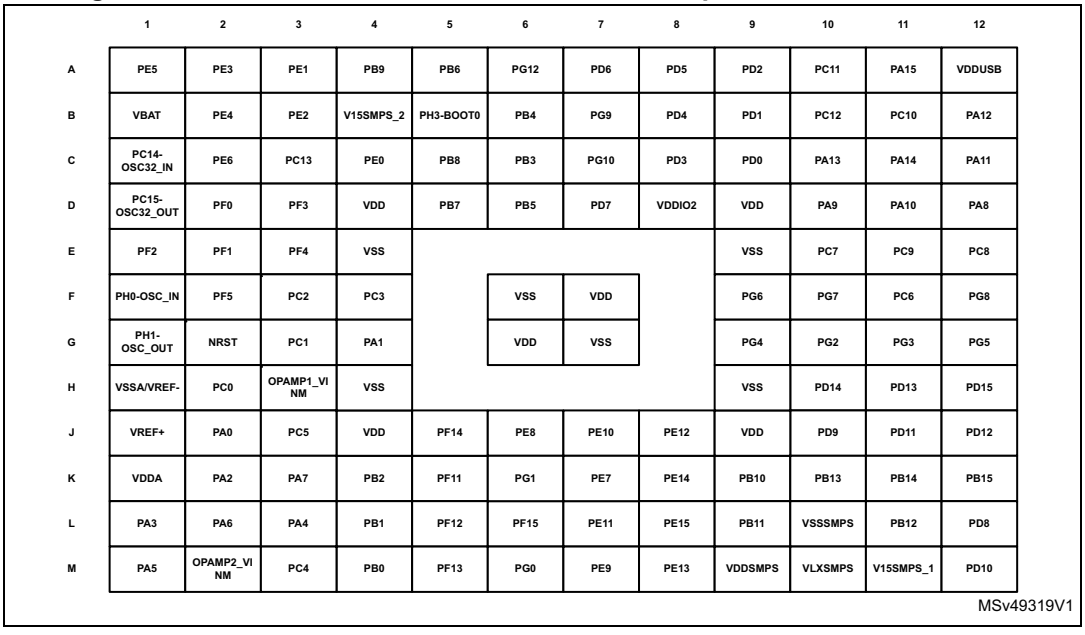
1. The above figure shows the package top view.

Figure 21. STM32L552xx UFBGA132 ballout



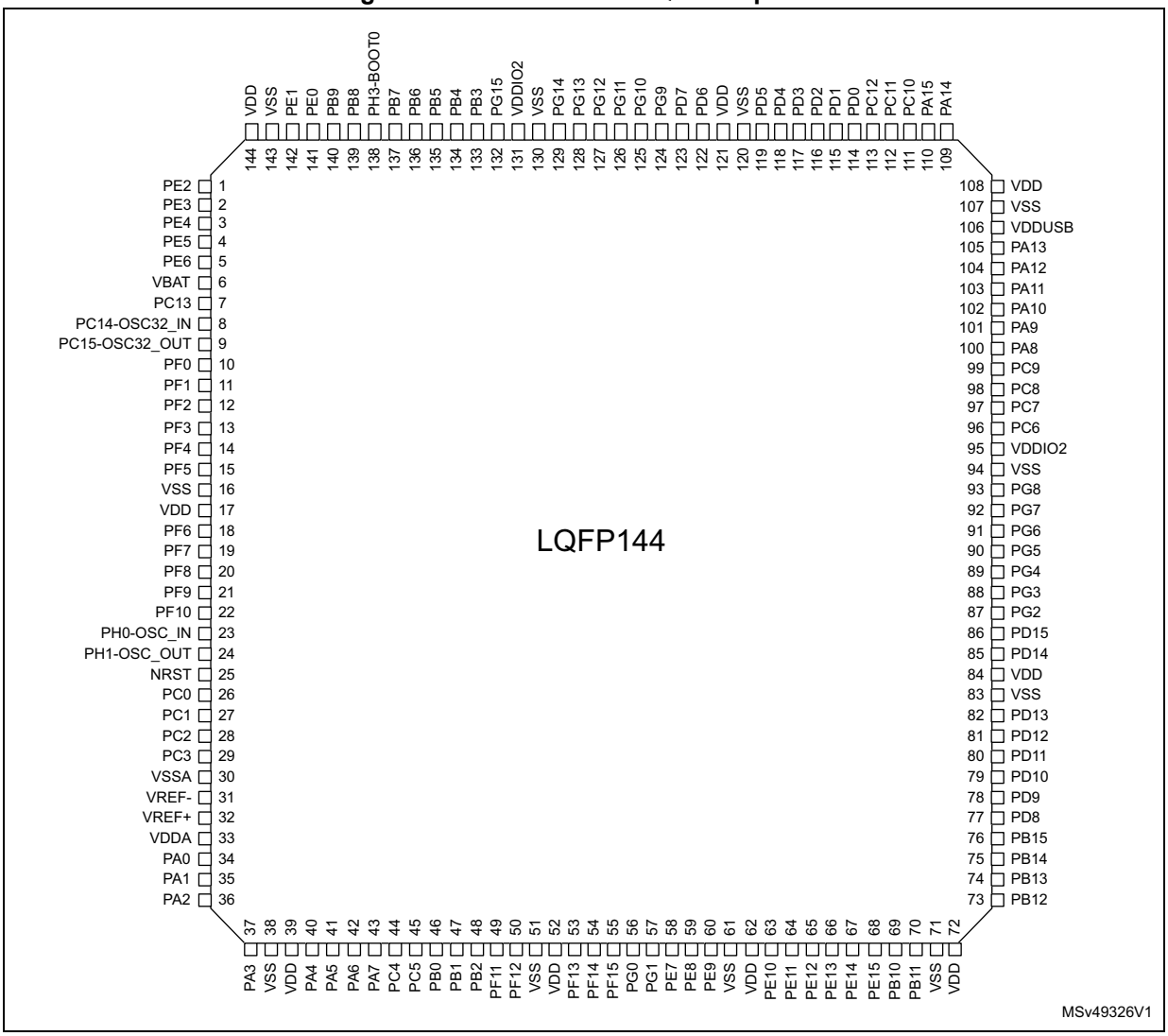
1. The above figure shows the package top view.

Figure 22. STM32L552xxxxQ UFBGA132 SMPS step down converter ballout



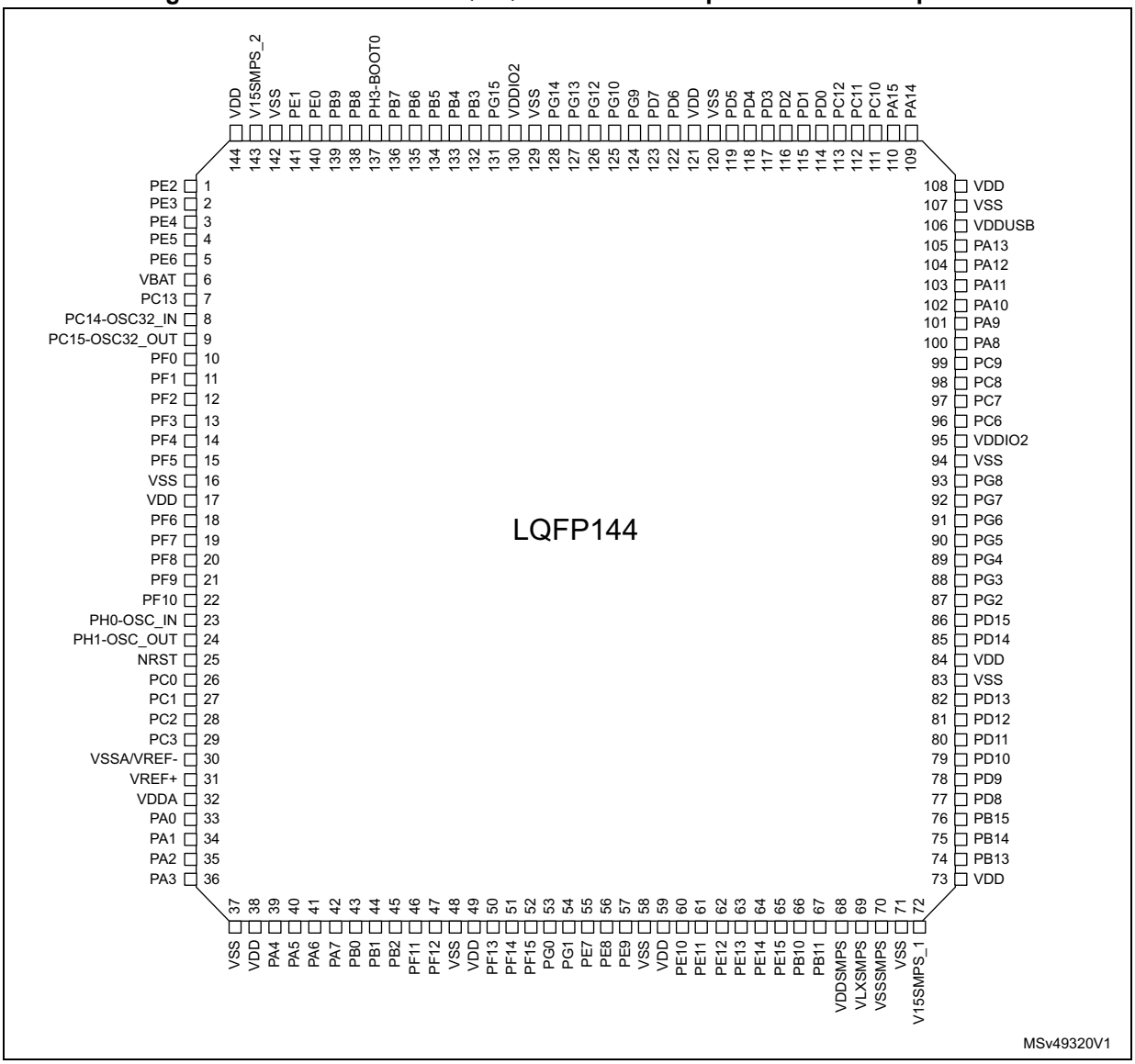
1. The above figure shows the package top view.

Figure 23. STM32L552xx LQFP144 pinout



1. The above figure shows the package top view.

Figure 24. STM32L552xxxxQ LQFP144 SMPS step down converter pinout



1. The above figure shows the package top view.

Table 20. Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after rese	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input / output pin
I/O structure		FT	5 V tolerant I/O
		TT	3.6 V tolerant I/O
		B	Dedicated BOOT0 pin
		RST	Bidirectional reset pin with embedded weak pull-up resistor
		Option for TT or FT I/Os	
		_f (1)	I/O, Fm+ capable
		_u (2)	I/O, with USB function supplied by V_{DDUSB}
		_a (3)(4)	I/O, with Analog switch function supplied by V_{DDA}
		_s (5)	I/O supplied only by V_{DDIO2}
		_c	I/O, USB Type-C PD capable
		_d	I/O, USB Type-C PD dead battery function
Notes		Unless otherwise specified by a note, all I/Os are set as analog inputs during and after reset.	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

1. The related I/O structures in *Table 21* are: FT_f, FT_fa.
2. The related I/O structures in *Table 21* are: FT_u.
3. The related I/O structures in *Table 21* are: FT_a, FT_fa, TT_a.
4. The analog switch for the TSC function is supplied by V_{DD}.
5. The related I/O structures in *Table 21* are: FT_s, FT_fs.

Table 21. STM32L552xx pin definitions

Pin Number														Pin name (function after reset)	Pin type	I/O structure	Notes	Alter
STM32L552xxxxP				STM32L552xxxxQ					STM32L552xx									
UFQFPN48_Ext-SMPS	LQFP48_Ext-SMPS	LQFP64_Ext-SMPS	WLCSP81_Ext-SMPS	LQFP64_SMPS	WLCSP81_SMPS	LQFP100_SMPS	UFBGA132_SMPS	LQFP144_SMPS	UFQFPN48	LQFP48	LQFP64	LQFP100	UFBGA132	LQFP144				
-	-	-	-	-	-	1	B3	1	-	-	-	1	B3	1	PE2	I/O	FT	-	TRACE S TS F SA E
-	-	-	-	-	-	2	A2	2	-	-	-	2	A2	2	PE3	I/O	FT	-	TRACE OCT TS F S E
-	-	-	-	-	-	3	B2	3	-	-	-	3	B2	3	PE4	I/O	FT	-	TRACE DFS TS FMC_A E
-	-	-	-	-	-	4	A1	4	-	-	-	4	A1	4	PE5	I/O	FT	-	TRACE S DFS TS F SA E

Table 21. STM32L552xx pin definitions (continued)

Pin Number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alter
STM32L552xxxxP				STM32L552xxxxQ					STM32L552xx										
UFQFPN48_Ext-SMPS	LQFP48_Ext-SMPS	LQFP64_Ext-SMPS	WLCSP81_Ext-SMPS	LQFP64_SMPS	WLCSP81_SMPS	LQFP100_SMPS	UFBGA132_SMPS	LQFP144_SMPS	UFQFPN48	LQFP48	LQFP64	LQFP100	UFBGA132	LQFP144					
-	-	-	-	-	-	5	C2	5	-	-	-	5	C2	5	PE6	I/O	FT	-	TRACE SAI1_ S E
1	1	1	B9	1	B9	6	B1	6	1	1	1	6	B1	6	VBAT	S	-	-	
2	2	2	B7	2	B7	7	C3	7	2	2	2	7	C3	7	PC13	I/O	FT	(1) (2)	E
3	3	3	C9	3	C9	8	C1	8	3	3	3	8	C1	8	PC14-OSC32_IN (PC14)	I/O	FT	(1) (2)	E
4	4	4	C8	4	C8	9	D1	9	4	4	4	9	D1	9	PC15-OSC32_OUT (PC15)	I/O	FT	(1) (2)	E
-	-	-	-	-	-	-	D2	10	-	-	-	-	D2	10	PF0	I/O	FT_f	-	I2C2_ E
-	-	-	-	-	-	-	E2	11	-	-	-	-	E2	11	PF1	I/O	FT_f	-	I2C2_ E

Table 21. STM32L552xx pin definitions (continued)

Pin Number														Pin name (function after reset)	Pin type	I/O structure	Notes	Alter
STM32L552xxxxP				STM32L552xxxxQ					STM32L552xx									
UFQFPN48_Ext-SMPS	LQFP48_Ext-SMPS	LQFP64_Ext-SMPS	WLCSP81_Ext-SMPS	LQFP64_SMPS	WLCSP81_SMPS	LQFP100_SMPS	UFBGA132_SMPS	LQFP144_SMPS	UFQFPN48	LQFP48	LQFP64	LQFP100	UFBGA132	LQFP144				
-	-	-	-	-	-	-	E1	12	-	-	-	-	E1	12	PF2	I/O	FT	-	I2C2_S E
-	-	-	-	-	-	-	D3	13	-	-	-	-	D3	13	PF3	I/O	FT	-	LPTIM E
-	-	-	-	-	-	-	E3	14	-	-	-	-	E3	14	PF4	I/O	FT	-	LP FMC_
-	-	-	-	-	-	-	F2	15	-	-	-	-	F2	15	PF5	I/O	FT	-	LP FMC_
-	-	-	-	-	-	10	F6	16	-	-	-	10	F6	16	VSS	S	-	-	
-	-	-	-	-	-	11	F7	17	-	-	-	11	F7	17	VDD	S	-	-	
-	-	-	-	-	-	-	-	18	-	-	-	-	-	18	PF6	I/O	FT	-	TIM5_E OC S E
-	-	-	-	-	-	-	-	19	-	-	-	-	-	19	PF7	I/O	FT	-	T OC SA E
-	-	-	-	-	-	-	-	20	-	-	-	-	-	20	PF8	I/O	FT	-	T OC SA E

Table 21. STM32L552xx pin definitions (continued)

Pin Number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alter
STM32L552xxxxP				STM32L552xxxxQ					STM32L552xx										
UFQFPN48_Ext-SMPS	LQFP48_Ext-SMPS	LQFP64_Ext-SMPS	WLCSP81_Ext-SMPS	LQFP64_SMPS	WLCSP81_SMPS	LQFP100_SMPS	UFBGA132_SMPS	LQFP144_SMPS	UFQFPN48	LQFP48	LQFP64	LQFP100	UFBGA132	LQFP144					
-	-	-	-	-	-	-	-	21	-	-	-	-	-	21	PF9	I/O	FT	-	T OC S T E
-	-	-	-	-	-	-	-	22	-	-	-	-	-	22	PF10	I/O	FT	-	OC DFS SAI1_D E
5	5	5	D9	5	D9	12	F1	23	5	5	5	12	F1	23	PH0-OSC_IN (PH0)	I/O	FT	-	E
6	6	6	D8	6	D8	13	G1	24	6	6	6	13	G1	24	PH1-OSC_OUT (PH1)	I/O	FT	-	E
7	7	7	E9	7	E9	14	G2	25	7	7	7	14	G2	25	NRST	I-O	RST	-	

Table 21. STM32L552xx pin definitions (continued)

Pin Number														Pin name (function after reset)	Pin type	I/O structure	Notes	Alter
STM32L552xxxxP				STM32L552xxxxQ					STM32L552xx									
UFQFPN48_Ext-SMPS	LQFP48_Ext-SMPS	LQFP64_Ext-SMPS	WLCSP81_Ext-SMPS	LQFP64_SMPS	WLCSP81_SMPS	LQFP100_SMPS	UFBGA132_SMPS	LQFP144_SMPS	UFQFPN48	LQFP48	LQFP64	LQFP100	UFBGA132	LQFP144				
-	-	8	E7	8	E7	15	H2	26	-	-	8	15	H2	26	PC0	I/O	FT_fa	-	LP OC I LP SD S LP E
-	-	9	F8	9	F8	16	G3	27	-	-	9	16	G3	27	PC1	I/O	FT_fa	-	T LP S I LP OC S E
-	-	10	F7	10	F7	17	F3	28	-	-	10	17	F3	28	PC2	I/O	FT_a	-	LP S DFS OC E

Table 21. STM32L552xx pin definitions (continued)

Pin Number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alter
STM32L552xxxxP				STM32L552xxxxQ					STM32L552xx										
UFQFPN48_Ext-SMPS	LQFP48_Ext-SMPS	LQFP64_Ext-SMPS	WLCSP81_Ext-SMPS	LQFP64_SMPS	WLCSP81_SMPS	LQFP100_SMPS	UFBGA132_SMPS	LQFP144_SMPS	UFQFPN48	LQFP48	LQFP64	LQFP100	UFBGA132	LQFP144					
-	-	11	G7	11	G7	18	F4	29	-	-	11	18	F4	29	PC3	I/O	FT_a	-	LP LP SAI1_D OCT S LP E
-	-	-	-	-	-	-	-	-	-	-	-	19	-	30	VSSA	S	-	-	
-	-	-	-	-	-	-	-	-	-	-	-	20	-	31	VREF-	S	-	-	
8	8	12	G9	12	G9	19	H1	30	8	8	12	-	H1	-	VSSA/ VREF-	S	-	-	
-	-	-	G8	-	G8	20	J1	31	-	-	-	21	J1	32	VREF+	S	-	-	
-	-	-	H9	-	H9	21	K1	32	-	-	-	22	K1	33	VDDA	S	-	-	
9	9	13	-	13	-	-	-	-	9	9	13	-	-	-	VDDA/ VREF+	S	-	-	

Table 21. STM32L552xx pin definitions (continued)

Pin Number														Pin name (function after reset)	Pin type	I/O structure	Notes	Alter
STM32L552xxxxP				STM32L552xxxxQ					STM32L552xx									
UFQFPN48_Ext-SMPS	LQFP48_Ext-SMPS	LQFP64_Ext-SMPS	WLCSP81_Ext-SMPS	LQFP64_SMPS	WLCSP81_SMPS	LQFP100_SMPS	UFBGA132_SMPS	LQFP144_SMPS	UFQFPN48	LQFP48	LQFP64	LQFP100	UFBGA132	LQFP144					
10	10	14	H8	14	H8	22	J2	33	10	10	14	23	J2	34	PA0	I/O	FT_a	-	TIM2_C T USART 2_NS SA T E
-	-	-	-	-	-	-	H3	-	-	-	-	-	H3	-	OPAMP1_VINM	I	TT	-	
11	11	15	F6	15	F6	23	G4	34	11	11	15	24	G4	35	PA1	I/O	FT_a	-	TIM2_C I2 S USART 2_DE OCT TI E

Table 21. STM32L552xx pin definitions (continued)

Pin Number														Pin name (function after reset)	Pin type	I/O structure	Notes	Alter
STM32L552xxxxP				STM32L552xxxxQ					STM32L552xx									
UFQFPN48_Ext-SMPS	LQFP48_Ext-SMPS	LQFP64_Ext-SMPS	WLCSP81_Ext-SMPS	LQFP64_SMPS	WLCSP81_SMPS	LQFP100_SMPS	UFBGA132_SMPS	LQFP144_SMPS	UFQFPN48	LQFP48	LQFP64	LQFP100	UFBGA132	LQFP144				
12	12	16	G6	16	G6	24	K2	35	12	12	16	25	K2	36	PA2	I/O	FT_a	-	TIM2_C US LP OCT UCP SA TI E
13	13	17	F5	17	F5	25	L1	36	13	13	17	26	L1	37	PA3	I/O	TT_a	-	TIM2_C S US LP OCT SA TI E
-	-	18	H2	18	H2	26	G7	37	-	-	18	27	G7	38	VSS	S	-	-	
-	-	19	-	19	-	27	G6	38	-	-	19	28	G6	39	VDD	S	-	-	
14	14	20	H7	20	H7	28	L3	39	14	14	20	29	L3	40	PA4	I/O	TT_a	-	OCT SPI1_N US S LP E

Table 21. STM32L552xx pin definitions (continued)

Pin Number														Pin name (function after reset)	Pin type	I/O structure	Notes	Alter
STM32L552xxxxP				STM32L552xxxxQ					STM32L552xx									
UFQFPN48_Ext-SMPS	LQFP48_Ext-SMPS	LQFP64_Ext-SMPS	WLCSP81_Ext-SMPS	LQFP64_SMPS	WLCSP81_SMPS	LQFP100_SMPS	UFBGA132_SMPS	LQFP144_SMPS	UFQFPN48	LQFP48	LQFP64	LQFP100	UFBGA132	LQFP144					
15	15	21	H6	21	H6	29	M1	40	15	15	21	30	M1	41	PA5	I/O	TT_a	-	TIM2_C TI S LP E
16	16	22	G5	22	G5	30	L2	41	16	16	22	31	L2	42	PA6	I/O	FT_a	-	T T T S USART LPU OC T E
-	-	-	-	-	-	-	M2	-	-	-	-	-	M2	-	OPAMP2_VINM	I	TT	-	

Table 21. STM32L552xx pin definitions (continued)

Pin Number														Pin name (function after reset)	Pin type	I/O structure	Notes	Alter
STM32L552xxxxP				STM32L552xxxxQ					STM32L552xx									
UFQFPN48_Ext-SMPS	LQFP48_Ext-SMPS	LQFP64_Ext-SMPS	WLCSP81_Ext-SMPS	LQFP64_SMPS	WLCSP81_SMPS	LQFP100_SMPS	UFBGA132_SMPS	LQFP144_SMPS	UFQFPN48	LQFP48	LQFP64	LQFP100	UFBGA132	LQFP144					
17	17	23	J7	23	J7	31	K3	42	17	17	23	32	K3	43	PA7	I/O	FT_fa	-	TI T TI I S OC T E
-	-	24	G4	-	G4	-	M3	-	-	-	24	33	M3	44	PC4	I/O	FT_a	-	US OC E
-	-	-	-	-	-	-	J3	-	-	-	25	34	J3	45	PC5	I/O	FT_a	-	US E
18	18	25	J6	24	J6	32	M4	43	18	18	26	35	M4	46	PB0	I/O	TT_a	-	TI T TI S US OC CC SA E

Table 21. STM32L552xx pin definitions (continued)

Pin Number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alter
STM32L552xxxxP				STM32L552xxxxQ					STM32L552xx										
UFQFPN48_Ext-SMPS	LQFP48_Ext-SMPS	LQFP64_Ext-SMPS	WLCSP81_Ext-SMPS	LQFP64_SMPS	WLCSP81_SMPS	LQFP100_SMPS	UFBGA132_SMPS	LQFP144_SMPS	UFQFPN48	LQFP48	LQFP64	LQFP100	UFBGA132	LQFP144					
19	19	26	H5	25	H5	33	L4	44	19	19	27	36	L4	47	PB1	I/O	FT_a	-	TI T TI DFS USART LPUAR OC LP E
20	20	27	J5	26	J5	34	K4	45	20	20	28	37	K4	48	PB2	I/O	FT_a	-	LP I2 DFS OCT UCP E
-	-	-	-	-	-	-	K5	46	-	-	-	-	K5	49	PF11	I/O	FT	-	OCT E
-	-	-	-	-	-	-	L5	47	-	-	-	-	L5	50	PF12	I/O	FT	-	FMC_
-	-	-	J9	-	J9	-	-	48	-	-	-	-	-	51	VSS	S	-	-	
-	-	-	J8	-	J8	-	-	49	-	-	-	-	-	52	VDD	S	-	-	
-	-	-	-	-	-	-	M5	50	-	-	-	-	M5	53	PF13	I/O	FT	-	I2C4_S E

Table 21. STM32L552xx pin definitions (continued)

Pin Number														Pin name (function after reset)	Pin type	I/O structure	Notes	Alter
STM32L552xxxxP				STM32L552xxxxQ					STM32L552xx									
UFQFPN48_Ext-SMPS	LQFP48_Ext-SMPS	LQFP64_Ext-SMPS	WLCSP81_Ext-SMPS	LQFP64_SMPS	WLCSP81_SMPS	LQFP100_SMPS	UFBGA132_SMPS	LQFP144_SMPS	UFQFPN48	LQFP48	LQFP64	LQFP100	UFBGA132	LQFP144				
-	-	-	-	-	-	-	J5	51	-	-	-	-	J5	54	PF14	I/O	FT_f	-	I TS FMC_
-	-	-	-	-	-	-	L6	52	-	-	-	-	L6	55	PF15	I/O	FT_f	-	I TS FMC_
-	-	-	-	-	-	-	M6	53	-	-	-	-	M6	56	PG0	I/O	FT	-	TS FMC_
-	-	-	-	-	-	-	K6	54	-	-	-	-	K6	57	PG1	I/O	FT	-	TS FMC_
-	-	-	-	-	-	35	K7	55	-	-	-	38	K7	58	PE7	I/O	FT	-	T DFS FMC_ E
-	-	-	-	-	-	36	J6	56	-	-	-	39	J6	59	PE8	I/O	FT	-	TI DFS SA E
-	-	-	-	-	-	37	M7	57	-	-	-	40	M7	60	PE9	I/O	FT	-	T DFS OCT FMC_ E

Table 21. STM32L552xx pin definitions (continued)

Pin Number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alter
STM32L552xxxxP				STM32L552xxxxQ					STM32L552xx										
UFQFPN48_Ext-SMPS	LQFP48_Ext-SMPS	LQFP64_Ext-SMPS	WLCSP81_Ext-SMPS	LQFP64_SMPS	WLCSP81_SMPS	LQFP100_SMPS	UFBGA132_SMPS	LQFP144_SMPS	UFQFPN48	LQFP48	LQFP64	LQFP100	UFBGA132	LQFP144					
-	-	-	-	-	-	-	-	58	-	-	-	-	L10	61	VSS	S	-	-	
-	-	-	H1	-	H1	-	J4	59	-	-	-	-	J4	62	VDD	S	-	-	
-	-	-	-	-	-	38	J7	60	-	-	-	41	J7	63	PE10	I/O	FT	-	TI TS OCT SA E
-	-	-	-	-	-	39	L7	61	-	-	-	42	L7	64	PE11	I/O	FT	-	T TS OCT FMC_I
-	-	-	-	-	-	40	J8	62	-	-	-	43	J8	65	PE12	I/O	FT	-	TI S TS OCT FMC_I
-	-	-	J4	-	-	41	M8	63	-	-	-	44	M8	66	PE13	I/O	FT	-	TIM1_C TS OCT FMC_D

Table 21. STM32L552xx pin definitions (continued)

Pin Number														Pin name (function after reset)	Pin type	I/O structure	Notes	Alter
STM32L552xxxxP				STM32L552xxxxQ					STM32L552xx									
UFQFPN48_Ext-SMPS	LQFP48_Ext-SMPS	LQFP64_Ext-SMPS	WLCSP81_Ext-SMPS	LQFP64_SMPS	WLCSP81_SMPS	LQFP100_SMPS	UFBGA132_SMPS	LQFP144_SMPS	UFQFPN48	LQFP48	LQFP64	LQFP100	UFBGA132	LQFP144				
-	-	-	H4	-	-	42	K8	64	-	-	-	45	K8	67	PE14	I/O	FT	-	T TI S OC FMC_D
-	-	-	H3	-	-	43	L8	65	-	-	-	46	L8	68	PE15	I/O	FT	-	T S OC FMC_D
21	21	28	J3	27	J4	44	K9	66	21	21	29	47	K9	69	PB10	I/O	FT_f	-	T LP I2C4_S S US LP T OC CC SA E

Table 21. STM32L552xx pin definitions (continued)

Pin Number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alter
STM32L552xxxxP				STM32L552xxxxQ					STM32L552xx										
UFQFPN48_Ext-SMPS	LQFP48_Ext-SMPS	LQFP64_Ext-SMPS	WLCSP81_Ext-SMPS	LQFP64_SMPS	WLCSP81_SMPS	LQFP100_SMPS	UFBGA132_SMPS	LQFP144_SMPS	UFQFPN48	LQFP48	LQFP64	LQFP100	UFBGA132	LQFP144					
-	-	29	J2	-	H4	45	L9	67	22	22	30	48	L9	70	PB11	I/O	FT_f	-	TIM2_C I US LP OCT CC E
-	-	-	-	28	J3	46	M9	68	-	-	-	-	-	-	VDDSMPS	S	-	-	
-	-	-	-	29	H3	47	M10	69	-	-	-	-	-	-	VLXSMPS	S	-	-	
-	-	-	-	30	J2	48	L10	70	-	-	-	-	-	-	VSSSMPS	S	-	-	
22	22	30	J1	-	-	-	-	-	-	-	-	-	-	-	VDD12_1	S	-	-	
23	23	31	B2	31	B2	49	E9	71	23	23	31	49	E9	71	VSS	S	-	-	
-	-	-	-	32	J1	50	M11	72	-	-	-	-	-	-	V15SMPS_1	S	-	-	
24	24	32	A1	33	A1	51	D4	73	24	24	32	50	D4	72	VDD	S	-	-	

Table 21. STM32L552xx pin definitions (continued)

Pin Number														Pin name (function after reset)	Pin type	I/O structure	Notes	Alter
STM32L552xxxxP				STM32L552xxxxQ					STM32L552xx									
UFQFPN48_Ext-SMPS	LQFP48_Ext-SMPS	LQFP64_Ext-SMPS	WLCSP81_Ext-SMPS	LQFP64_SMPS	WLCSP81_SMPS	LQFP100_SMPS	UFBGA132_SMPS	LQFP144_SMPS	UFQFPN48	LQFP48	LQFP64	LQFP100	UFBGA132	LQFP144					
25	25	33	G2	-	G2	-	L11	-	25	25	33	51	L11	73	PB12	I/O	FT	-	T I2 S DFS US LPUAR TS OCT S TI E
26	26	34	F2	34	F2	52	K10	74	26	26	34	52	K10	74	PB13	I/O	FT _f	-	TI LF I2C2_S DFS USART LPU TS UCP SA TI E

Table 21. STM32L552xx pin definitions (continued)

Pin Number														Pin name (function after reset)	Pin type	I/O structure	Notes	Alter
STM32L552xxxxP				STM32L552xxxxQ					STM32L552xx									
UFQFPN48_Ext-SMPS	LQFP48_Ext-SMPS	LQFP64_Ext-SMPS	WLCSP81_Ext-SMPS	LQFP64_SMPS	WLCSP81_SMPS	LQFP100_SMPS	UFBGA132_SMPS	LQFP144_SMPS	UFQFPN48	LQFP48	LQFP64	LQFP100	UFBGA132	LQFP144					
27	27	35	G1	35	G1	53	K11	75	27	27	35	53	K11	75	PB14	I/O	FT_fd	-	TI LP TI I S DFS USART 3_DE SA T E
28	28	36	F1	36	F1	54	K12	76	28	28	36	54	K12	76	PB15	I/O	FT_c	-	R TI TI S DFS S T E
-	-	-	-	-	-	55	L12	77	-	-	-	55	L12	77	PD8	I/O	FT	-	US FMC_D
-	-	-	-	-	-	56	J10	78	-	-	-	56	J10	78	PD9	I/O	FT	-	US R SA E

Table 21. STM32L552xx pin definitions (continued)

Pin Number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alter
STM32L552xxxxP				STM32L552xxxxQ					STM32L552xx										
UFQFPN48_Ext-SMPS	LQFP48_Ext-SMPS	LQFP64_Ext-SMPS	WLCSP81_Ext-SMPS	LQFP64_SMPS	WLCSP81_SMPS	LQFP100_SMPS	UFBGA132_SMPS	LQFP144_SMPS	UFQFPN48	LQFP48	LQFP64	LQFP100	UFBGA132	LQFP144					
-	-	-	-	-	-	57	M12	79	-	-	-	57	M12	79	PD10	I/O	FT	-	US TS F SA E
-	-	-	-	-	-	58	J11	80	-	-	-	58	J11	80	PD11	I/O	FT	-	I2 USART 3_NSS F S LP E
-	-	-	-	-	-	59	J12	81	-	-	-	59	J12	81	PD12	I/O	FT_f	-	TIM4_ USART 3_DE FMC_A LP E
-	-	-	-	-	-	60	H11	82	-	-	-	60	H11	82	PD13	I/O	FT_f	-	TIM4_ TS F LP E
-	-	-	-	-	-	-	-	83	-	-	-	-	-	83	VSS	S	-	-	

Table 21. STM32L552xx pin definitions (continued)

Pin Number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alter
STM32L552xxxxP				STM32L552xxxxQ					STM32L552xx										
UFQFPN48_Ext-SMPS	LQFP48_Ext-SMPS	LQFP64_Ext-SMPS	WLCSP81_Ext-SMPS	LQFP64_SMPS	WLCSP81_SMPS	LQFP100_SMPS	UFBGA132_SMPS	LQFP144_SMPS	UFQFPN48	LQFP48	LQFP64	LQFP100	UFBGA132	LQFP144					
-	-	-	-	-	-	-	-	84	-	-	-	-	-	84	VDD	S	-	-	
-	-	-	-	-	-	61	H10	85	-	-	-	61	H10	85	PD14	I/O	FT	-	TIM4_ E
-	-	-	-	-	-	62	H12	86	-	-	-	62	H12	86	PD15	I/O	FT	-	TIM4_ E
-	-	-	-	-	-	-	G10	87	-	-	-	-	G10	87	PG2	I/O	FT _s	-	SPI1_ SA E
-	-	-	-	-	-	-	G11	88	-	-	-	-	G11	88	PG3	I/O	FT _s	-	SPI1_M S E
-	-	-	-	-	-	-	G9	89	-	-	-	-	G9	89	PG4	I/O	FT _s	-	SPI1_M SA E
-	-	-	-	-	-	-	G12	90	-	-	-	-	G12	90	PG5	I/O	FT _s	-	S LPU F S E

Table 21. STM32L552xx pin definitions (continued)

Pin Number														Pin name (function after reset)	Pin type	I/O structure	Notes	Alter
STM32L552xxxxP				STM32L552xxxxQ					STM32L552xx									
UFQFPN48_Ext-SMPS	LQFP48_Ext-SMPS	LQFP64_Ext-SMPS	WLCSP81_Ext-SMPS	LQFP64_SMPS	WLCSP81_SMPS	LQFP100_SMPS	UFBGA132_SMPS	LQFP144_SMPS	UFQFPN48	LQFP48	LQFP64	LQFP100	UFBGA132	LQFP144					
-	-	-	-	-	-	-	F9	91	-	-	-	-	F9	91	PG6	I/O	FT_s	-	OCT I2 LPUAR UCP E
-	-	-	-	-	-	-	F10	92	-	-	-	-	F10	92	PG7	I/O	FT_fs	-	SAI1_C DFS LP UCP SA E
-	-	-	-	-	-	-	F12	93	-	-	-	-	F12	93	PG8	I/O	FT_fs	-	I LP E
-	-	-	-	-	-	-	-	94	-	-	-	-	-	94	VSS	S	-	-	
-	-	-	-	-	-	-	-	95	-	-	-	-	-	95	VDDIO 2	S	-	-	

Table 21. STM32L552xx pin definitions (continued)

Pin Number														Pin name (function after reset)	Pin type	I/O structure	Notes	Alter
STM32L552xxxxP				STM32L552xxxxQ					STM32L552xx									
UFQFPN48_Ext-SMPS	LQFP48_Ext-SMPS	LQFP64_Ext-SMPS	WLCSP81_Ext-SMPS	LQFP64_SMPS	WLCSP81_SMPS	LQFP100_SMPS	UFBGA132_SMPS	LQFP144_SMPS	UFQFPN48	LQFP48	LQFP64	LQFP100	UFBGA132	LQFP144				
-	-	37	E1	37	E1	63	F11	96	-	-	37	63	F11	96	PC6	I/O	FT	-	TIM3_C DFS SDM TS SD SA E
-	-	38	E2	38	E2	64	E10	97	-	-	38	64	E10	97	PC7	I/O	FT	-	TIM3_C DFS SDMM TS SD SA E
-	-	39	F3	39	F3	65	E12	98	-	-	39	65	E12	98	PC8	I/O	FT	-	TIM3_C TS SD E

Table 21. STM32L552xx pin definitions (continued)

Pin Number														Pin name (function after reset)	Pin type	I/O structure	Notes	Alter
STM32L552xxxxP				STM32L552xxxxQ					STM32L552xx									
UFQFPN48_Ext-SMPS	LQFP48_Ext-SMPS	LQFP64_Ext-SMPS	WLCSP81_Ext-SMPS	LQFP64_SMPS	WLCSP81_SMPS	LQFP100_SMPS	UFBGA132_SMPS	LQFP144_SMPS	UFQFPN48	LQFP48	LQFP64	LQFP100	UFBGA132	LQFP144				
-	-	40	G3	40	G3	66	E11	99	-	-	40	66	E11	99	PC9	I/O	FT_f	-	T TI TIM3_C TS U SD SA E
29	29	41	F4	41	F4	67	D12	100	29	29	41	67	D12	100	PA8	I/O	FT_f	-	MCO S US SA LP E
30	30	42	D1	42	D1	68	D10	101	30	30	42	68	D10	101	PA9	I/O	FT_fu	-	TIM1_C US S TI E
31	31	43	E3	43	E3	69	D11	102	31	31	43	69	D11	102	PA10	I/O	FT_fu	-	TIM1_ US C S TI E

Table 21. STM32L552xx pin definitions (continued)

Pin Number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alter
STM32L552xxxxP				STM32L552xxxxQ					STM32L552xx										
UFQFPN48_Ext-SMPS	LQFP48_Ext-SMPS	LQFP64_Ext-SMPS	WLCSP81_Ext-SMPS	LQFP64_SMPS	WLCSP81_SMPS	LQFP100_SMPS	UFBGA132_SMPS	LQFP144_SMPS	UFQFPN48	LQFP48	LQFP64	LQFP100	UFBGA132	LQFP144					
32	32	44	C1	44	C1	70	C12	103	32	32	44	70	C12	103	PA11	I/O	FT_u	-	T TI S USART 1_NSS USB_D
33	33	45	C2	45	C2	71	B12	104	33	33	45	71	B12	104	PA12	I/O	FT_u	-	T S USART 1_DE USB_I
34	34	46	D2	46	D2	72	C10	105	34	34	46	72	C10	105	PA13 (JTMS/ SWDIO)	I/O	FT	(3)	JT IR_OU S E
-	-	47	-	47	-	-	-	-	-	-	47	-	-	-	VSS	S	-	-	
-	-	48	B1	48	B1	73	A12	106	-	-	48	73	A12	106	VDDUSB	S	-	-	
35	35	-	B5	-	B5	74	H4	107	35	35	-	74	H4	107	VSS	S	-	-	
36	36	-	A9	-	A9	75	D9	108	36	36	-	75	D9	108	VDD	S	-	-	

Table 21. STM32L552xx pin definitions (continued)

Pin Number														Pin name (function after reset)	Pin type	I/O structure	Notes	Alter
STM32L552xxxxP				STM32L552xxxxQ					STM32L552xx									
UFQFPN48_Ext-SMPS	LQFP48_Ext-SMPS	LQFP64_Ext-SMPS	WLCSP81_Ext-SMPS	LQFP64_SMPS	WLCSP81_SMPS	LQFP100_SMPS	UFBGA132_SMPS	LQFP144_SMPS	UFQFPN48	LQFP48	LQFP64	LQFP100	UFBGA132	LQFP144					
37	37	49	D3	49	D3	76	C11	109	37	37	49	76	C11	109	PA14 (JTCK/ SWCL K)	I/O	FT	(3)	JT LP I2 I2 S E
38	38	50	E4	50	E4	77	A11	110	38	38	50	77	A11	110	PA15 (JTDI)	I/O	FT _c	(3)	JTD T US SPI1_N USART UART DE, E
-	-	51	A2	51	A2	78	B11	111	-	-	51	78	B11	111	PC10	I/O	FT	-	T LP S US U TS SD SA E

Table 21. STM32L552xx pin definitions (continued)

Pin Number														Pin name (function after reset)	Pin type	I/O structure	Notes	Alter
STM32L552xxxxP				STM32L552xxxxQ					STM32L552xx									
UFQFPN48_Ext-SMPS	LQFP48_Ext-SMPS	LQFP64_Ext-SMPS	WLCSP81_Ext-SMPS	LQFP64_SMPS	WLCSP81_SMPS	LQFP100_SMPS	UFBGA132_SMPS	LQFP144_SMPS	UFQFPN48	LQFP48	LQFP64	LQFP100	UFBGA132	LQFP144				
-	-	52	C3	52	C3	79	A10	112	-	-	52	79	A10	112	PC11	I/O	FT	-	LP OCT S US U TS UCP SD SA E
-	-	53	B3	53	B3	80	B10	113	-	-	53	80	B10	113	PC12	I/O	FT	-	T S US U TS SD S E
-	-	-	-	-	-	81	C9	114	-	-	-	81	C9	114	PD0	I/O	FT	-	S FD FMC_I
-	-	-	-	-	-	82	B9	115	-	-	-	82	B9	115	PD1	I/O	FT	-	S FD FMC_I

Table 21. STM32L552xx pin definitions (continued)

Pin Number														Pin name (function after reset)	Pin type	I/O structure	Notes	Alter
STM32L552xxxxP				STM32L552xxxxQ					STM32L552xx									
UFQFPN48_Ext-SMPS	LQFP48_Ext-SMPS	LQFP64_Ext-SMPS	WLCSP81_Ext-SMPS	LQFP64_SMPS	WLCSP81_SMPS	LQFP100_SMPS	UFBGA132_SMPS	LQFP144_SMPS	UFQFPN48	LQFP48	LQFP64	LQFP100	UFBGA132	LQFP144				
-	-	-	A3	54	A3	83	A9	116	-	-	54	83	A9	116	PD2	I/O	FT	-	TRACE USART 3_DE T SDM E
-	-	-	-	-	-	84	C8	117	-	-	-	84	C8	117	PD3	I/O	FT	-	S S DFS USART 2_NS E
-	-	-	-	-	-	85	B8	118	-	-	-	85	B8	118	PD4	I/O	FT	-	S DFS USART 2_DE, F E
-	-	-	-	-	-	86	A8	119	-	-	-	86	A8	119	PD5	I/O	FT	-	US OC F E
-	-	-	-	-	-	-	-	120	-	-	-	-	-	120	VSS	S	-	-	
-	-	-	-	-	-	-	-	121	-	-	-	-	-	121	VDD	S	-	-	

Table 21. STM32L552xx pin definitions (continued)

Pin Number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alter
STM32L552xxxxP				STM32L552xxxxQ					STM32L552xx										
UFQFPN48_Ext-SMPS	LQFP48_Ext-SMPS	LQFP64_Ext-SMPS	WLCSP81_Ext-SMPS	LQFP64_SMPS	WLCSP81_SMPS	LQFP100_SMPS	UFBGA132_SMPS	LQFP144_SMPS	UFQFPN48	LQFP48	LQFP64	LQFP100	UFBGA132	LQFP144					
-	-	-	-	-	-	87	A7	122	-	-	-	87	A7	122	PD6	I/O	FT	-	SAI1_D DFSI US OCT FM S E
-	-	-	-	-	-	88	D7	123	-	-	-	88	D7	123	PD7	I/O	FT	-	DFS US OCT FMC_I E
-	-	-	D4	-	D4	-	B7	124	-	-	-	-	B7	124	PG9	I/O	FT_s	-	S US FMC_I SA TI E
-	-	-	C4	-	C4	-	C7	125	-	-	-	-	C7	125	PG10	I/O	FT_s	-	LP S US F S TI E

Table 21. STM32L552xx pin definitions (continued)

Pin Number														Pin name (function after reset)	Pin type	I/O structure	Notes	Alter
STM32L552xxxxP				STM32L552xxxxQ					STM32L552xx									
UFQFPN48_Ext-SMPS	LQFP48_Ext-SMPS	LQFP64_Ext-SMPS	WLCSP81_Ext-SMPS	LQFP64_SMPS	WLCSP81_SMPS	LQFP100_SMPS	UFBGA132_SMPS	LQFP144_SMPS	UFQFPN48	LQFP48	LQFP64	LQFP100	UFBGA132	LQFP144					
-	-	-	E5	-	E5	-	-	-	-	-	-	-	M11	126	PG11	I/O	FT_s	-	LP OC S USART SA T E
-	-	-	B4	-	B4	-	A6	126	-	-	-	-	A6	127	PG12	I/O	FT_s	-	LP S USART 1_D S E
-	-	-	A4	-	A4	-	-	127	-	-	-	-	M10	128	PG13	I/O	FT_fs	-	I US FMC_A
-	-	-	D5	-	D5	-	-	128	-	-	-	-	M9	129	PG14	I/O	FT_fs	-	I2C1_S E
-	-	-	B8	-	B8	-	H9	129	-	-	-	-	H9	130	VSS	S	-	-	
-	-	-	A5	-	A5	-	D8	130	-	-	-	-	D8	131	VDDIO2	S	-	-	

Table 21. STM32L552xx pin definitions (continued)

Pin Number														Pin name (function after reset)	Pin type	I/O structure	Notes	Alter
STM32L552xxxxP				STM32L552xxxxQ					STM32L552xx									
UFQFPN48_Ext-SMPS	LQFP48_Ext-SMPS	LQFP64_Ext-SMPS	WLCSP81_Ext-SMPS	LQFP64_SMPS	WLCSP81_SMPS	LQFP100_SMPS	UFBGA132_SMPS	LQFP144_SMPS	UFQFPN48	LQFP48	LQFP64	LQFP100	UFBGA132	LQFP144					
-	-	-	C5	-	C5	-	-	131	-	-	-	-	B4	132	PG15	I/O	FT_s	-	LP I2 E
39	39	54	E6	55	E6	89	C6	132	39	39	55	89	C6	133	PB3 (JTDO/ TRACESWO)	I/O	FT_a	-	JTDO TIM2_C S USART 1_DE SA E
40	40	55	B6	56	B6	90	B6	133	40	40	56	90	B6	134	PB4 (NJTRST)	I/O	FT_fa	(3)	NJTR I S S USART UART DE, SA TI E

Table 21. STM32L552xx pin definitions (continued)

Pin Number														Pin name (function after reset)	Pin type	I/O structure	Notes	Alter
STM32L552xxxxP				STM32L552xxxxQ					STM32L552xx									
UFQFPN48_Ext-SMPS	LQFP48_Ext-SMPS	LQFP64_Ext-SMPS	WLCSP81_Ext-SMPS	LQFP64_SMPS	WLCSP81_SMPS	LQFP100_SMPS	UFBGA132_SMPS	LQFP144_SMPS	UFQFPN48	LQFP48	LQFP64	LQFP100	UFBGA132	LQFP144					
41	41	56	A6	57	A6	91	D6	134	41	41	57	91	D6	135	PB5	I/O	FT_d	-	LP T OCT I2 S S US UART NSS, CC S TI E
42	42	57	C6	58	C6	92	A5	135	42	42	58	92	A5	136	PB6	I/O	FT_fa	-	LP T TI I2C1_S US TS S TII E

Table 21. STM32L552xx pin definitions (continued)

Pin Number														Pin name (function after reset)	Pin type	I/O structure	Notes	Alter
STM32L552xxxxP				STM32L552xxxxQ					STM32L552xx									
UFQFPN48_Ext-SMPS	LQFP48_Ext-SMPS	LQFP64_Ext-SMPS	WLCSP81_Ext-SMPS	LQFP64_SMPS	WLCSP81_SMPS	LQFP100_SMPS	UFBGA132_SMPS	LQFP144_SMPS	UFQFPN48	LQFP48	LQFP64	LQFP100	UFBGA132	LQFP144					
43	43	58	D6	59	D6	93	D5	136	43	43	59	93	D5	137	PB7	I/O	FT_fa	-	LP T T I2C1_S US UA TS TI E
44	44	59	D7	60	D7	94	B5	137	44	44	60	94	B5	138	PH3-BOOT0	I/O	FT	-	E
45	45	60	C7	61	C7	95	C5	138	45	45	61	95	C5	139	PB8	I/O	FT_f	-	TIM4_C I DFS SDM FD SD SA T E

Table 21. STM32L552xx pin definitions (continued)

Pin Number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alter
STM32L552xxxxP				STM32L552xxxxQ					STM32L552xx										
UFQFPN48_Ext-SMPS	LQFP48_Ext-SMPS	LQFP64_Ext-SMPS	WLCSP81_Ext-SMPS	LQFP64_SMPS	WLCSP81_SMPS	LQFP100_SMPS	UFBGA132_SMPS	LQFP144_SMPS	UFQFPN48	LQFP48	LQFP64	LQFP100	UFBGA132	LQFP144					
-	-	61	A7	-	A7	96	A4	139	46	46	62	96	A4	140	PB9	I/O	FT_f	-	IR_OU SAI1_ S SDM FD SD S TI E
-	-	-	-	-	-	97	C4	140	-	-	-	97	C4	141	PE0	I/O	FT	-	T F TI E
-	-	-	-	-	-	-	A3	141	-	-	-	98	A3	142	PE1	I/O	FT	-	F TI E
46	46	62	A8	-	-	-	-	-	-	-	-	-	-	-	VDD12_2	S	-	-	
47	47	63	E8	62	E8	98	E4	142	47	47	63	99	E4	143	VSS	S	-	-	
-	-	-	-	63	A8	99	B4	143	-	-	-	-	-	-	V15SMPS_2	S	-	-	
48	48	64	F9	64	F9	100	J9	144	48	48	64	100	J9	144	VDD	S	-	-	

1. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the u
   mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF
   - These GPIOs must not be used as current sources (for example to drive a LED).
2. After a Backup domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the RTC
   system reset. For details on how to manage these GPIOs, refer to the Backup domain and RTC register descriptions in the RM0438
3. After reset, these pins are configured as JTAG/SW debug alternate functions, and the internal pull-up on PA15, PA13, PB4 pins and
   activated.

Table 22. Alternate function AF0 to AF7(1)

Port		AF0	AF1	AF2	AF3	AF4	AF5
		SYS_AF	TIM1/2/5/8/LPTIM1	TIM1/2/3/4/5/LPTIM3	SPI2/SAI1/I2C4/USART2/TIM1/8/OCTOSPI1	I2C1/2/3/4	SPI1/2/3/I2C4/DFSDM1/OCTOSPI1
Port A	PA0	-	TIM2_CH1	TIM5_CH1	TIM8_ETR	-	-
	PA1	-	TIM2_CH2	TIM5_CH2	-	I2C1_SMBA	SPI1_SCK
	PA2	-	TIM2_CH3	TIM5_CH3	-	-	-
	PA3	-	TIM2_CH4	TIM5_CH4	SAI1_CK1	-	-
	PA4	-	-	-	OCTOSPI1_NCS	-	SPI1_NSS
	PA5	-	TIM2_CH1	TIM2_ETR	TIM8_CH1N	-	SPI1_SCK
	PA6	-	TIM1_BKIN	TIM3_CH1	TIM8_BKIN	-	SPI1_MISO
	PA7	-	TIM1_CH1N	TIM3_CH2	TIM8_CH1N	I2C3_SCL	SPI1_MOSI
	PA8	MCO	TIM1_CH1	-	SAI1_CK2	-	-
	PA9	-	TIM1_CH2	-	SPI2_SCK	-	-
	PA10	-	TIM1_CH3	-	SAI1_D1	-	-
	PA11	-	TIM1_CH4	TIM1_BKIN2	-	-	SPI1_MISO
	PA12	-	TIM1_ETR	-	-	-	SPI1_MOSI
	PA13	JTMS/SWDIO	IR_OUT	-	-	-	-
	PA14	JTCK/SWCLK	LPTIM1_OUT	-	-	I2C1_SMBA	I2C4_SMBA
	PA15	JTDI	TIM2_CH1	TIM2_ETR	USART2_RX	-	SPI1_NSS

Table 22. Alternate function AF0 to AF7(1) (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5
		SYS_AF	TIM1/2/5/8/LPTIM1	TIM1/2/3/4/5/LPTIM3	SPI2/SAI1/I2C4/USART2/TIM1/8/OCTOSPI1	I2C1/2/3/4	SPI1/2/3/I2C4/DFSDM1/OCTOSPI1
Port B	PB0	-	TIM1_CH2N	TIM3_CH3	TIM8_CH2N	-	SPI1_NSS
	PB1	-	TIM1_CH3N	TIM3_CH4	TIM8_CH3N	-	-
	PB2	-	LPTIM1_OUT	-	-	I2C3_SMBA	-
	PB3	JTDO/TRACESWO	TIM2_CH2	-	-	-	SPI1_SCK
	PB4	NJTRST	-	TIM3_CH1	-	I2C3_SDA	SPI1_MISO
	PB5	-	LPTIM1_IN1	TIM3_CH2	OCTOSPI1_NCLK	I2C1_SMBA	SPI1_MOSI
	PB6	-	LPTIM1_ETR	TIM4_CH1	TIM8_BKIN2	I2C1_SCL	I2C4_SCL
	PB7	-	LPTIM1_IN2	TIM4_CH2	TIM8_BKIN	I2C1_SDA	I2C4_SDA
	PB8	-	-	TIM4_CH3	SAI1_CK1	I2C1_SCL	DFSDM1_CKOUT
	PB9	-	IR_OUT	TIM4_CH4	SAI1_D2	I2C1_SDA	SPI2_NSS
	PB10	-	TIM2_CH3	LPTIM3_OUT	I2C4_SCL	I2C2_SCL	SPI2_SCK
	PB11	-	TIM2_CH4	-	I2C4_SDA	I2C2_SDA	-
	PB12	-	TIM1_BKIN	-	TIM1_BKIN	I2C2_SMBA	SPI2_NSS
	PB13	-	TIM1_CH1N	LPTIM3_IN1	-	I2C2_SCL	SPI2_SCK
	PB14	-	TIM1_CH2N	LPTIM3_ETR	TIM8_CH2N	I2C2_SDA	SPI2_MISO
	PB15	RTC_REFIN	TIM1_CH3N	-	TIM8_CH3N	-	SPI2_MOSI

Table 22. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5
		SYS_AF	TIM1/2/5/8/LPTIM1	TIM1/2/3/4/5/LPTIM3	SPI2/SAI1/I2C4/USART2/TIM1/8/OCTOSPI1	I2C1/2/3/4	SPI1/2/3/I2C4/DFSDM1/OCTOSPI1
Port C	PC0	-	LPTIM1_IN1	-	OCTOSPI1_IO7	I2C3_SCL	-
	PC1	TRACED0	LPTIM1_OUT	-	SPI2_MOSI	I2C3_SDA	-
	PC2	-	LPTIM1_IN2	-	-	-	SPI2_MISO
	PC3	-	LPTIM1_ETR	LPTIM3_OUT	SAI1_D1	-	SPI2_MOSI
	PC4	-	-	-	-	-	-
	PC5	-	-	-	SAI1_D3	-	-
	PC6	-	-	TIM3_CH1	TIM8_CH1	-	-
	PC7	-	-	TIM3_CH2	TIM8_CH2	-	-
	PC8	-	-	TIM3_CH3	TIM8_CH3	-	-
	PC9	TRACED0	TIM8_BKIN2	TIM3_CH4	TIM8_CH4	-	-
	PC10	TRACED1	-	LPTIM3_ETR	-	-	-
	PC11	-	-	LPTIM3_IN1	-	-	OCTOSPI1_N
	PC12	TRACED3	-	-	-	-	-
	PC13	-	-	-	-	-	-
	PC14	-	-	-	-	-	-
	PC15	-	-	-	-	-	-

Table 22. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5
		SYS_AF	TIM1/2/5/8/LPTIM1	TIM1/2/3/4/5/LPTIM3	SPI2/SAI1/I2C4/USART2/TIM1/8/OCTOSPI1	I2C1/2/3/4	SPI1/2/3/I2C4/DFSDM1/OCTOSPI1
Port D	PD0	-	-	-	-	-	SPI2_NSS
	PD1	-	-	-	-	-	SPI2_SCK
	PD2	TRACED2	-	TIM3_ETR	-	-	-
	PD3	-	-	-	SPI2_SCK	-	SPI2_MISO
	PD4	-	-	-	-	-	SPI2_MOSI
	PD5	-	-	-	-	-	-
	PD6	-	-	-	SAI1_D1	-	SPI3_MOSI
	PD7	-	-	-	-	-	-
	PD8	-	-	-	-	-	-
	PD9	-	-	-	-	-	-
	PD10	-	-	-	-	-	-
	PD11	-	-	-	-	I2C4_SMBA	-
	PD12	-	-	TIM4_CH1	-	I2C4_SCL	-
	PD13	-	-	TIM4_CH2	-	I2C4_SDA	-
	PD14	-	-	TIM4_CH3	-	-	-
	PD15	-	-	TIM4_CH4	-	-	-

Table 22. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5
		SYS_AF	TIM1/2/5/8/LPTIM1	TIM1/2/3/4/5/LPTIM3	SPI2/SAI1/I2C4/USART2/TIM1/8/OCTOSPI1	I2C1/2/3/4	SPI1/2/3/I2C4/DFSDM1/OCTOSPI1
Port E	PE0	-	-	TIM4_ETR	-	-	-
	PE1	-	-	-	-	-	-
	PE2	TRACECK	-	TIM3_ETR	SAI1_CK1	-	-
	PE3	TRACED0	-	TIM3_CH1	OCTOSPI1_DQS	-	-
	PE4	TRACED1	-	TIM3_CH2	SAI1_D2	-	-
	PE5	TRACED2	-	TIM3_CH3	SAI1_CK2	-	-
	PE6	TRACED3	-	TIM3_CH4	SAI1_D1	-	-
	PE7	-	TIM1_ETR	-	-	-	-
	PE8	-	TIM1_CH1N	-	-	-	-
	PE9	-	TIM1_CH1	-	-	-	-
	PE10	-	TIM1_CH2N	-	-	-	-
	PE11	-	TIM1_CH2	-	-	-	-
	PE12	-	TIM1_CH3N	-	-	-	SPI1_NSS
	PE13	-	TIM1_CH3	-	-	-	SPI1_SCK
	PE14	-	TIM1_CH4	TIM1_BKIN2	TIM1_BKIN2	-	SPI1_MISO
	PE15	-	TIM1_BKIN	-	TIM1_BKIN	-	SPI1_MOSI

Table 22. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5
		SYS_AF	TIM1/2/5/8/LPTIM1	TIM1/2/3/4/5/LPTIM3	SPI2/SAI1/I2C4/USART2/TIM1/8/OCTOSPI1	I2C1/2/3/4	SPI1/2/3/I2C4/DFSDM1/OCTOSPI1
Port F	PF0	-	-	-	-	I2C2_SDA	-
	PF1	-	-	-	-	I2C2_SCL	-
	PF2	-	-	-	-	I2C2_SMBA	-
	PF3	-	-	LPTIM3_IN1	-	-	-
	PF4	-	-	LPTIM3_ETR	-	-	-
	PF5	-	-	LPTIM3_OUT	-	-	-
	PF6	-	TIM5_ETR	TIM5_CH1	-	-	-
	PF7	-	-	TIM5_CH2	-	-	-
	PF8	-	-	TIM5_CH3	-	-	-
	PF9	-	-	TIM5_CH4	-	-	-
	PF10	-	-	-	OCTOSPI1_CLK	-	-
	PF11	-	-	-	OCTOSPI1_NCLK	-	-
	PF12	-	-	-	-	-	-
	PF13	-	-	-	-	I2C4_SMBA	-
	PF14	-	-	-	-	I2C4_SCL	-
	PF15	-	-	-	-	I2C4_SDA	-

Table 22. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5
		SYS_AF	TIM1/2/5/8/LPTIM1	TIM1/2/3/4/5/LPTIM3	SPI2/SAI1/I2C4/USART2/TIM1/8/OCTOSPI1	I2C1/2/3/4	SPI1/2/3/I2C4/DFSDM1/OCTOSPI1
Port G	PG0	-	-	-	-	-	-
	PG1	-	-	-	-	-	-
	PG2	-	-	-	-	-	SPI1_SCK
	PG3	-	-	-	-	-	SPI1_MISO
	PG4	-	-	-	-	-	SPI1_MOSI
	PG5	-	-	-	-	-	SPI1_NSS
	PG6	-	-	-	OCTOSPI1_DQS	I2C3_SMBA	-
	PG7	-	-	-	SAI1_CK1	I2C3_SCL	-
	PG8	-	-	-	-	I2C3_SDA	-
	PG9	-	-	-	-	-	-
	PG10	-	LPTIM1_IN1	-	-	-	-
	PG11	-	LPTIM1_IN2	-	OCTOSPI1_IO5	-	-
	PG12	-	LPTIM1_ETR	-	-	-	-
	PG13	-	-	-	-	I2C1_SDA	-
	PG14	-	-	-	-	I2C1_SCL	-
	PG15	-	LPTIM1_OUT	-	-	I2C1_SMBA	-

Table 22. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5
		SYS_AF	TIM1/2/5/8/LPTIM1	TIM1/2/3/4/5/LPTIM3	SPI2/SAI1/I2C4/USART2/TIM1/8/OCTOSPI1	I2C1/2/3/4	SPI1/2/3/I2C4/DFSDM1/OCTOSPI1
Port H - -	PH0	-	-	-	-	-	-
	PH1	-	-	-	-	-	-
	PH3	-	-	-	-	-	-

1. Refer to *Table 23* for AF8 to AF15.

Table 23. Alternate function AF8 to AF15(1)

Port		AF8	AF9	AF10	AF11	AF12	AF13
		UART4/5/LPUART1/SDMMC1	FDCAN1/TSC	USB/OCTOSPI1	UCPD1	SDMMC1/COMP1/2/TIM1/8/FMC	SAI1/2/TIM
Port A	PA0	UART4_TX	-	-	-	-	SAI1_EXTC
	PA1	UART4_RX	-	OCTOSPI1_DQS	-	-	-
	PA2	LPUART1_TX	-	OCTOSPI1_NCS	UCPD1_FRSTX1	-	SAI2_EXTC
	PA3	LPUART1_RX	-	OCTOSPI1_CLK	-	-	SAI1_MCLK
	PA4	-	-	-	-	-	SAI1_FS_
	PA5	-	-	-	-	-	-
	PA6	LPUART1_CTS_NSS	-	OCTOSPI1_IO3	-	TIM1_BKIN	TIM8_BKI
	PA7	-	-	OCTOSPI1_IO2	-	-	-
	PA8	-	-	-	-	-	SAI1_SCK_
	PA9	-	-	-	-	-	SAI1_FS_
	PA10	-	-	CRS_SYNC	-	-	SAI1_SD_
	PA11	-	FDCAN1_RX	USB_DM	-	TIM1_BKIN2	-
	PA12	-	FDCAN1_TX	USB_DP	-	-	-
	PA13	-	-	USB_NOE	-	-	SAI1_SD_
	PA14	-	-	-	-	-	SAI1_FS_
	PA15	UART4_RTS_DE	-	-	-	-	SAI2_FS_

Table 23. Alternate function AF8 to AF15(1) (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13
		UART4/5/LPUART1/SDMMC1	FDCAN1/TSC	USB/OCTOSPI1	UCPD1	SDMMC1/COMP1/2/TIM1/8/FMC	SAI1/2/TIM
Port B	PB0	-	-	OCTOSPI1_IO1	-	COMP1_OUT	SAI1_EXTC
	PB1	LPUART1_RTS_DE	-	OCTOSPI1_IO0	-	-	-
	PB2	-	-	OCTOSPI1_DQS	UCPD1_FRSTX1	-	-
	PB3	-	-	CRS_SYNC	-	-	SAI1_SCK
	PB4	UART5_RTS_DE	TSC_G2_IO1	-	-	-	SAI1_MCLK
	PB5	UART5_CTS_NSS	TSC_G2_IO2	-	-	COMP2_OUT	SAI1_SD_
	PB6	-	TSC_G2_IO3	-	-	TIM8_BKIN2	SAI1_FS_
	PB7	UART4_CTS_NSS	TSC_G2_IO4	-	-	FMC_NL	TIM8_BKI
	PB8	SDMMC1_CKIN	FDCAN1_RX	-	-	SDMMC1_D4	SAI1_MCLK
	PB9	SDMMC1_CDIR	FDCAN1_TX	-	-	SDMMC1_D5	SAI1_FS_
	PB10	LPUART1_RX	TSC_SYNC	OCTOSPI1_CLK	-	COMP1_OUT	SAI1_SCK
	PB11	LPUART1_TX	-	OCTOSPI1_NCS	-	COMP2_OUT	-
	PB12	LPUART1_RTS_DE	TSC_G1_IO1	OCTOSPI1_NCLK	-	-	SAI2_FS_
	PB13	LPUART1_CTS_NSS	TSC_G1_IO2	-	UCPD1_FRSTX2	-	SAI2_SCK
	PB14	-	TSC_G1_IO3	-	-	-	SAI2_MCLK
	PB15	-	-	-	-	-	SAI2_SD_

Table 23. Alternate function AF8 to AF15(1) (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13
		UART4/5/LPUART1/SDMMC1	FDCAN1/TSC	USB/OCTOSPI1	UCPD1	SDMMC1/COMP1/2/TIM1/8/FMC	SAI1/2/TIM
Port C	PC0	LPUART1_RX	-	-	-	SDMMC1_D5	SAI2_FS_
	PC1	LPUART1_TX	-	OCTOSPI1_IO4	-	-	SAI1_SD_
	PC2	-	TSC_G3_IO1	OCTOSPI1_IO5	-	-	-
	PC3	-	TSC_G1_IO4	OCTOSPI1_IO6	-	-	SAI1_SD_
	PC4	-	-	OCTOSPI1_IO7	-	-	-
	PC5	-	-	-	-	-	-
	PC6	SDMMC1_D0DIR	TSC_G4_IO1	-	-	SDMMC1_D6	SAI2_MCLK
	PC7	SDMMC1_D123DIR	TSC_G4_IO2	-	-	SDMMC1_D7	SAI2_MCLK
	PC8	-	TSC_G4_IO3	-	-	SDMMC1_D0	-
	PC9	-	TSC_G4_IO4	USB_NOE	-	SDMMC1_D1	SAI2_EXTC
	PC10	UART4_TX	TSC_G3_IO2	-	-	SDMMC1_D2	SAI2_SCK_
	PC11	UART4_RX	TSC_G3_IO3	-	UCPD1_FRSTX2	SDMMC1_D3	SAI2_MCLK
	PC12	UART5_TX	TSC_G3_IO4	-	-	SDMMC1_CK	SAI2_SD_
	PC13	-	-	-	-	-	-
	PC14	-	-	-	-	-	-
	PC15	-	-	-	-	-	-

Table 23. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13
		UART4/5/LPUART1/SDMMC1	FDCAN1/TSC	USB/OCTOSPI1	UCPD1	SDMMC1/COMP1/2/TIM1/8/FMC	SAI1/2/TIM
Port D	PD0	-	FDCAN1_RX	-	-	FMC_D2	-
	PD1	-	FDCAN1_TX	-	-	FMC_D3	-
	PD2	UART5_RX	TSC_SYNC	-	-	SDMMC1_CMD	-
	PD3	-	-	-	-	FMC_CLK	-
	PD4	-	-	OCTOSPI1_IO4	-	FMC_NOE	-
	PD5	-	-	OCTOSPI1_IO5	-	FMC_NWE	-
	PD6	-	-	OCTOSPI1_IO6	-	FMC_NWAIT	SAI1_SD_
	PD7	-	-	OCTOSPI1_IO7	-	FMC_NCE/FMC_NE1	-
	PD8	-	-	-	-	FMC_D13	-
	PD9	-	-	-	-	FMC_D14	SAI2_MCLK
	PD10	-	TSC_G6_IO1	-	-	FMC_D15	SAI2_SCK
	PD11	-	TSC_G6_IO2	-	-	FMC_A16	SAI2_SD_
	PD12	-	TSC_G6_IO3	-	-	FMC_A17	SAI2_FS_
	PD13	-	TSC_G6_IO4	-	-	FMC_A18	-
	PD14	-	-	-	-	FMC_D0	-
	PD15	-	-	-	-	FMC_D1	-

Table 23. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13
		UART4/5/LPUART1/SDMMC1	FDCAN1/TSC	USB/OCTOSPI1	UCPD1	SDMMC1/COMP1/2/TIM1/8/FMC	SAI1/2/TIM
Port E	PE0	-	-	-	-	FMC_NBL0	-
	PE1	-	-	-	-	FMC_NBL1	-
	PE2	-	TSC_G7_IO1	-	-	FMC_A23	SAI1_MCLK
	PE3	-	TSC_G7_IO2	-	-	FMC_A19	SAI1_SD_
	PE4	-	TSC_G7_IO3	-	-	FMC_A20	SAI1_FS_
	PE5	-	TSC_G7_IO4	-	-	FMC_A21	SAI1_SCK
	PE6	-	-	-	-	FMC_A22	SAI1_SD_
	PE7	-	-	-	-	FMC_D4	SAI1_SD_
	PE8	-	-	-	-	FMC_D5	SAI1_SCK
	PE9	-	-	OCTOSPI1_NCLK	-	FMC_D6	SAI1_FS_
	PE10	-	TSC_G5_IO1	OCTOSPI1_CLK	-	FMC_D7	SAI1_MCLK
	PE11	-	TSC_G5_IO2	OCTOSPI1_NCS	-	FMC_D8	-
	PE12	-	TSC_G5_IO3	OCTOSPI1_IO0	-	FMC_D9	-
	PE13	-	TSC_G5_IO4	OCTOSPI1_IO1	-	FMC_D10	-
	PE14	-	-	OCTOSPI1_IO2	-	FMC_D11	-
	PE15	-	-	OCTOSPI1_IO3	-	FMC_D12	-

Table 23. Alternate function AF8 to AF15(1) (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13
		UART4/5/LPUART1/SDMMC1	FDCAN1/TSC	USB/OCTOSPI1	UCPD1	SDMMC1/COMP1/2/TIM1/8/FMC	SAI1/2/TIM
Port F	PF0	-	-	-	-	FMC_A0	-
	PF1	-	-	-	-	FMC_A1	-
	PF2	-	-	-	-	FMC_A2	-
	PF3	-	-	-	-	FMC_A3	-
	PF4	-	-	-	-	FMC_A4	-
	PF5	-	-	-	-	FMC_A5	-
	PF6	-	-	OCTOSPI1_IO3	-	-	SAI1_SD_
	PF7	-	-	OCTOSPI1_IO2	-	-	SAI1_MCLK
	PF8	-	-	OCTOSPI1_IO0	-	-	SAI1_SCK_
	PF9	-	-	OCTOSPI1_IO1	-	-	SAI1_FS_
	PF10	-	-	-	-	-	SAI1_D3
	PF11	-	-	-	-	-	-
	PF12	-	-	-	-	FMC_A6	-
	PF13	-	-	-	-	FMC_A7	-
	PF14	-	TSC_G8_IO1	-	-	FMC_A8	-
	PF15	-	TSC_G8_IO2	-	-	FMC_A9	-

Table 23. Alternate function AF8 to AF15(1) (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13
		UART4/5/LPUART1/SDMMC1	FDCAN1/TSC	USB/OCTOSPI1	UCPD1	SDMMC1/COMP1/2/TIM1/8/FMC	SAI1/2/TIM
Port G	PG0	-	TSC_G8_IO3	-	-	FMC_A10	-
	PG1	-	TSC_G8_IO4	-	-	FMC_A11	-
	PG2	-	-	-	-	FMC_A12	SAI2_SCK
	PG3	-	-	-	-	FMC_A13	SAI2_FS_
	PG4	-	-	-	-	FMC_A14	SAI2_MCLK
	PG5	LPUART1_CTS_NSS	-	-	-	FMC_A15	SAI2_SD_
	PG6	LPUART1_RTS_DE	-	-	UCPD1_FRSTX1	-	-
	PG7	LPUART1_TX	-	-	UCPD1_FRSTX2	FMC_INT	SAI1_MCLK
	PG8	LPUART1_RX	-	-	-	-	-
	PG9	-	-	-	-	FMC_NCE/FMC_NE2	SAI2_SCK
	PG10	-	-	-	-	FMC_NE3	SAI2_FS_
	PG11	-	-	-	-	-	SAI2_MCLK
	PG12	-	-	-	-	FMC_NE4	SAI2_SD_
	PG13	-	-	-	-	FMC_A24	-
	PG14	-	-	-	-	FMC_A25	-
	PG15	-	-	-	-	-	-

Table 23. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13
		UART4/5/LPUART1/SDMMC1	FDCAN1/TSC	USB/OCTOSPI1	UCPD1	SDMMC1/COMP1/2/TIM1/8/FMC	SAI1/2/TIM
Port H	PH0	-	-	-	-	-	-
	PH1	-	-	-	-	-	-
	PH3	-	-	-	-	-	-

1. Refer to *Table 22* for AF0 to AF7.

5 Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

5.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3σ).

5.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = V_{DDA} = 3 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ±2σ).

5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 25*.

5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 26*.

Figure 25. Pin loading conditions

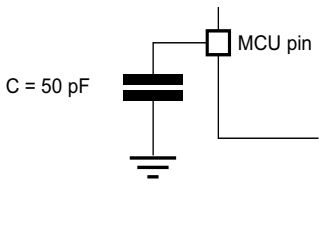
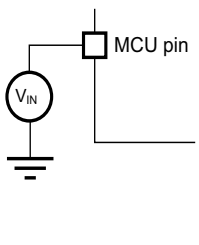


Figure 26. Pin input voltage



5.1.6 Power supply scheme

Figure 27. STM32L552xx and STM32L562xx power supply overview

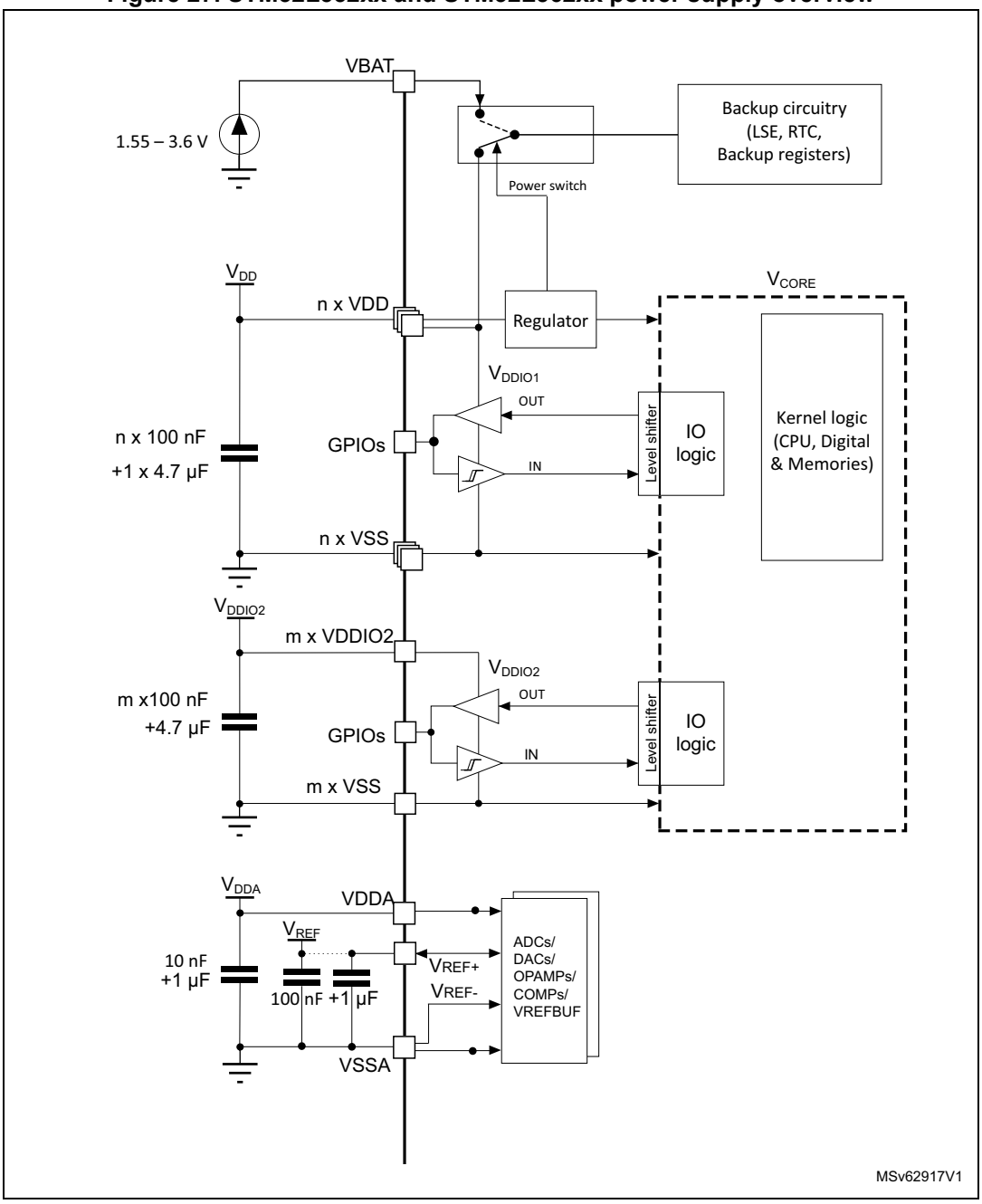
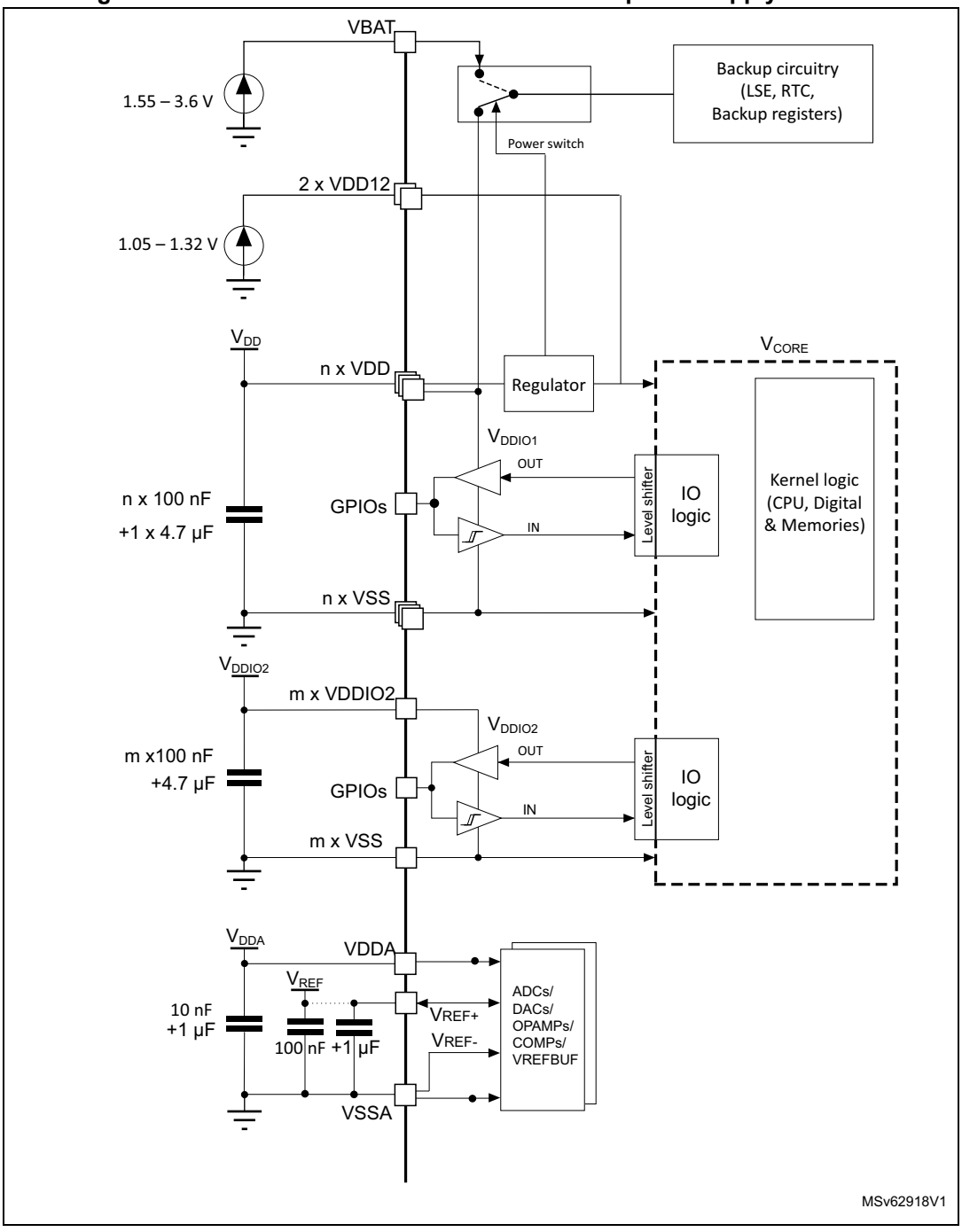
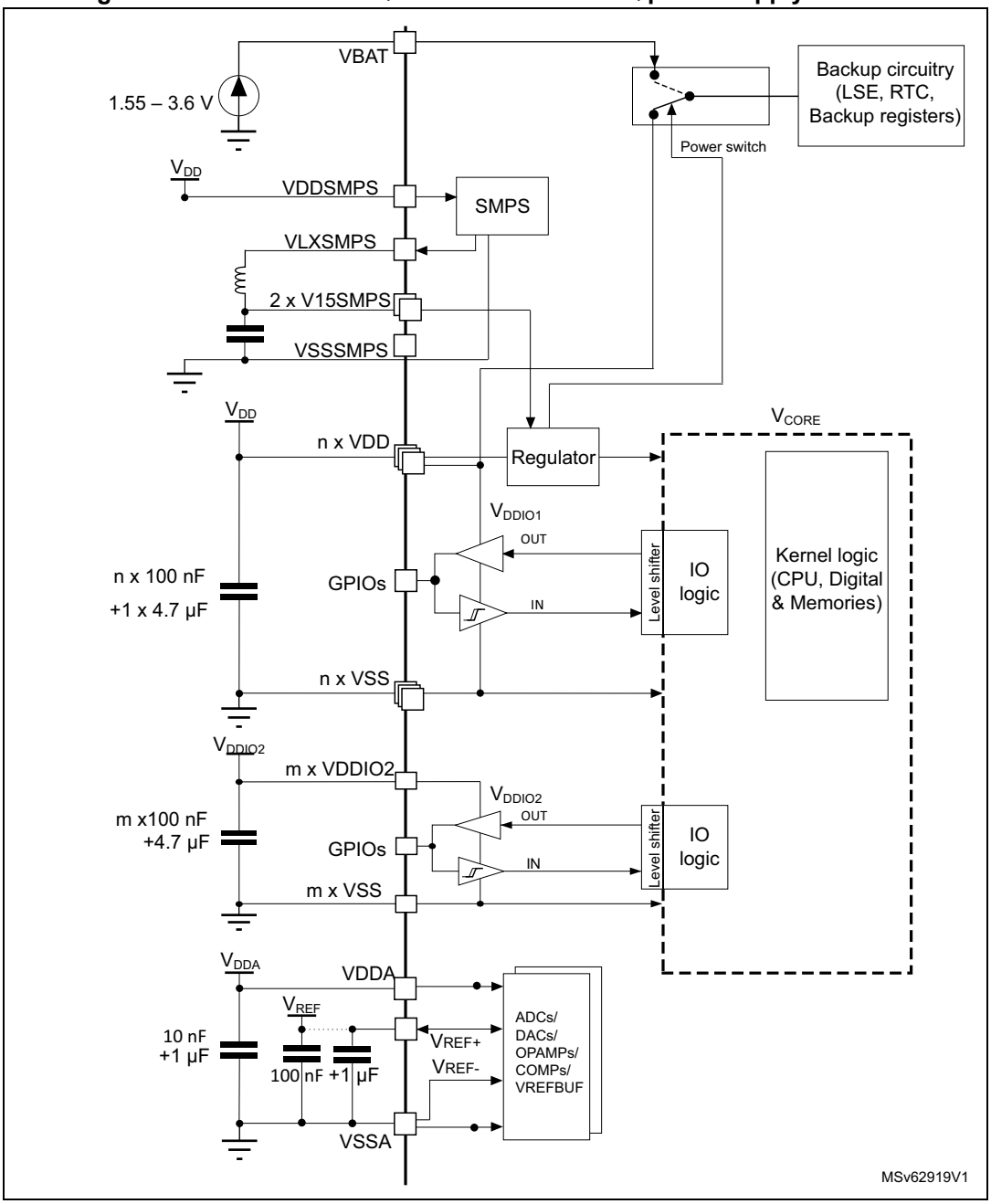


Figure 28. STM32L552xxxP and STM32L562xxxP power supply overview



Note: If the selected package has the external SMPS option but no external SMPS is used by the application (the embedded LDO is used instead), the VDD12 pins are kept unconnected.

Figure 29. STM32L552xxxQ and STM32L562xxxQ power supply overview



1. Refer to *Figure 3* for SMPS step down converter power supply scheme.

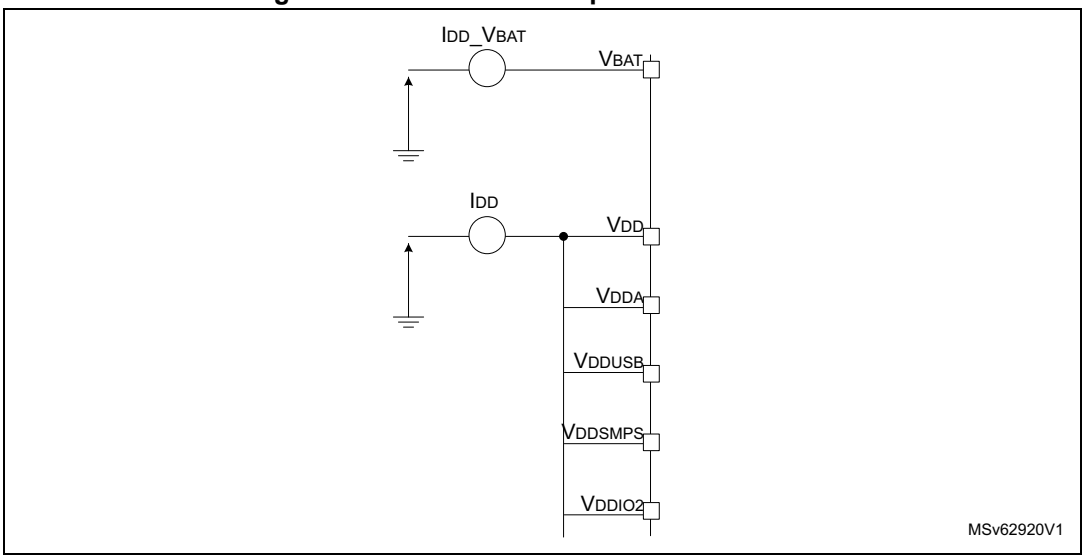
Note: If the selected package has the SMPS step down converter option but the application does not ever use the SMPS, it is recommended to set the SMPS power supply pins as follows: VDDSMPS and VLXSMPS connected to VSS
V15SMPSconnected to VDD.

Caution: Each power supply pair (V_{DD}/V_{SS}, V_{DDA}/V_{SSA} etc.) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

5.1.7 Current consumption measurement

The I_{DD_ALL} parameters given in *Table 33* to *Table 96* represent the total MCU consumption including the current supplying V_{DD}, V_{DDIO2}, V_{DDA}, V_{DDUSB}, V_{BAT} and V_{DDSMPS} if the device embeds the SMPS.

Figure 30. Current consumption measurement



5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 24: Voltage characteristics*, *Table 25: Current characteristics* and *Table 26: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Device mission profile (application conditions) is compliant with JEDEC JESD47 qualification standard, extended mission profiles are available on demand.

Table 24. Voltage characteristics(1)

Symbol	Ratings		Min	Max	Unit
V_{DDX} - V_{SS}	External main supply voltage (including V_{DD}, V_{DDA}, V_{DDIO2}, V_{DDUSB}, V_{BAT}, V_{DDSMPS}, V_{REF+})		-0.3	4.0	V
V_{DD12} - V_{SS}	External SMPS supply voltage	All ranges 0/1/2	-0.3	1.4	
			-0.3		
V_{IN}(2)	Input voltage on FT_xxx pins except FT_c pins		V_{SS}-0.3	min (V_{DD}, V_{DDA}, V_{DDIO2}, V_{DDUSB}, V_{DDSMPS}) + 4.0(3)(4)	
	Input voltage on FT_c pins		V_{SS}-0.3	5.5	
	Input voltage on any other pins		V_{SS}-0.3	4.0	

Table 24. Voltage characteristics(1) (continued)

Symbol	Ratings	Min	Max	Unit
$V_{REF+} - V_{DDA}$	Allowed voltage difference for $V_{REF+} > V_{DDA}$	-	0.4	V
$\lvert\Delta V_{DDx}\rvert$	Variations between different V_{DDX} power pins of the same domain	-	50	mV
$\lvert V_{SSx}-V_{SS}\rvert$	Variations between all the different ground pins(5)	-	50	

1. All main power (V_{DD}, V_{DDA}, V_{DDIO2}, V_{DDUSB}, V_{BAT}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to *Table 25: Current characteristics* for the maximum allowed injected current values.
3. This formula has to be applied only on the power supplies related to the IO structure described in the pin definition table.
4. To sustain a voltage higher than 4 V the internal pull-up/pull-down resistors must be disabled.
5. Include VREF- pin.

Table 25. Current characteristics

Symbol	Ratings	Max	Unit
$\sum IV_{DD}$	Total current into sum of all V_{DD} power lines (source)(1) (2)	160	mA
$\sum IV_{SS}$	Total current out of sum of all V_{SS} ground lines (sink)(1) (2)	160	
$IV_{DD(PIN)}$	Maximum current into each V_{DD} power pin (source)(1)	100	
$IV_{SS(PIN)}$	Maximum current out of each V_{SS} ground pin (sink)(1)	100	
$I_{IO(PIN)}$	Output current sunk by any I/O and control pin except FT_f	20	
	Output current sunk by any FT_f pin	20	
	Output current sourced by any I/O and control pin	20	
$\sum I_{IO(PIN)}$	Total output current sunk by sum of all I/Os and control pins(3)	100	
	Total output current sourced by sum of all I/Os and control pins(3)	100	
$I_{INJ(PIN)}$(4)	Injected current on FT_xxx, TT_xx, RST and B pins, except PA4, PA5	-5/+0(5)	
	Injected current on PA4, PA5	-5/0	
$\sum\lvert I_{INJ(PIN)}\rvert$	Total injected current (sum of all I/Os and control pins)(6)	+/-25	

1. All main power (V_{DD}, V_{DDA}, V_{DDIO2}, V_{DDUSB}, V_{BAT}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supplies, in the permitted range.
2. Valid also for V_{DD12} on SMPS package.
3. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count QFP packages.
4. Positive injection (when $V_{IN} > V_{DDIOx}$) is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
5. A negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer also to *Table 24: Voltage characteristics* for the minimum allowed input voltage values.
6. When several inputs are submitted to a current injection, the maximum $\sum\lvert I_{INJ(PIN)}\rvert$ is the absolute sum of the negative injected currents (instantaneous values).

Table 26. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Maximum junction temperature	150	°C

5.3 Operating conditions

5.3.1 General operating conditions

Table 27. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	110	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	110	
f_{PCLK2}	Internal APB2 clock frequency	-	0	110	
V_{DD}	Standard operating voltage	-	1.71 (1)	3.6	V
V_{DDSMPS}	Supply voltage for the internal SMPS step-down converter	$V_{DDSMPS} = V_{DD}$	1.71 (1)	3.6	V
V_{DD12}	Standard operating voltage	Up to 110 MHz	1.14	1.32	V
		Up to 80 MHz	1.08	1.32	
		Up to 26 MHz	1.05 (2)	1.32	
V_{DDIO2}	PG[15:2] I/Os supply voltage	At least one I/O in PG[15:2] used	1.08	3.6	V
		PG[15:2] not used	0	3.6	
V_{DDA}	Analog supply voltage	ADC or COMP used	1.62	3.6	V
		DAC or OPAMP used	1.8		
		VREFBUF used	2.4		
		ADC, DAC, OPAMP, COMP, VREFBUF not used	0		

Table 27. General operating conditions (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{BAT}	Backup operating voltage	-	1.55	3.6	V
V_{DDUSB}	USB supply voltage	USB used	3.0	3.6	V
		USB not used	0	3.6	
V_{IN}	I/O input voltage	TT_xx I/O	-0.3	V_{DDIOx}+0.3	V
		FT_c I/O	-0.3	5	
		All I/O except FT_c and TT_xx	-0.3	MIN(MIN(V_{DD}, V_{DDA}, V_{DDIO2}, V_{DDUSB}) +3.6 V, 5.5 V)(3)(4)	
P_D	Power dissipation at T_A = 85 °C for suffix 6(5)	LQFP48	See *Section 6.8: Thermal characteristics* for application appropriate thermal resistance and package. Power dissipation is then calculated according ambient temperature (T_A) and maximum junction temperature (T_J) and selected thermal resistance.		mW
		UFQFPN48			
		LQFP64			
		WLCSP81			
		LQFP100			
		UFBGA132			
		LQFP144			
P_D	Power dissipation at T_A = 125 °C for suffix 3(5)	LQFP48	See *Section 6.8: Thermal characteristics* for application appropriate thermal resistance and package. Power dissipation is then calculated according ambient temperature (T_A) and maximum junction temperature (T_J) and selected thermal resistance.		mW
		UFQFPN48			
		LQFP64			
		WLCSP81			
		LQFP100			
		UFBGA132			
		LQFP144			

Table 27. General operating conditions (continued)

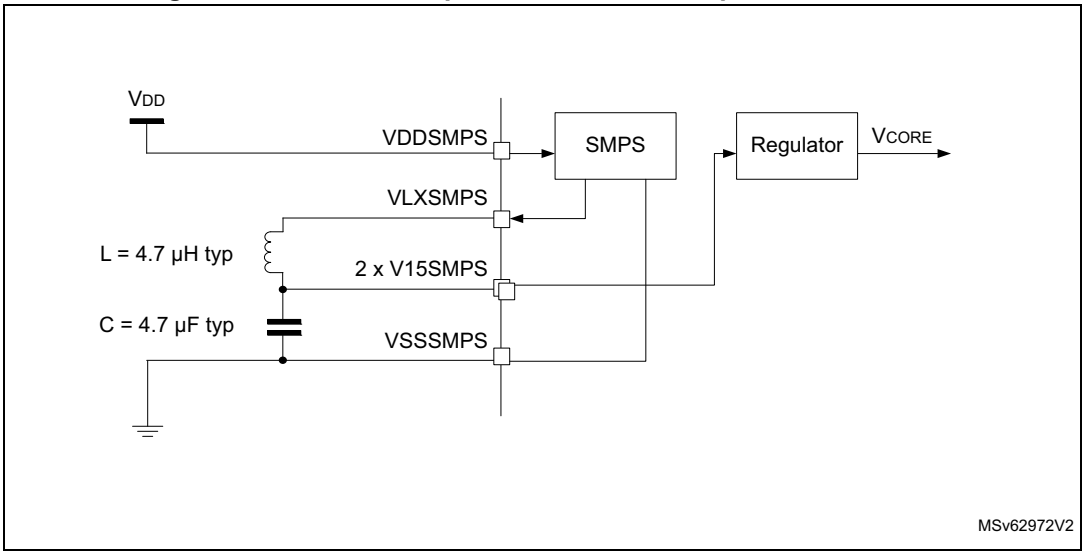
Symbol	Parameter	Conditions	Min	Max	Unit
T_A	Ambient temperature for the suffix 6 version	Maximum power dissipation	–40	85	°C
		Low-power dissipation(6)	–40	105	
	Ambient temperature for the suffix 3 version	Maximum power dissipation	–40	125	
		Low-power dissipation(6)	–40	130	
T_J	Junction temperature range	Suffix 6 version	–40	105	°C
		Suffix 3 version	–40	130	

1. When RESET is released functionality is guaranteed down to V_{BOR0} Min.
2. For Flash erase and program operation, V_{DD12} min must be 1.08 V.
3. This formula has to be applied only on the power supplies related to the IO structure described by the pin definition table. Maximum I/O input voltage is the smallest value between MIN(V_{DD}, V_{DDA}, V_{DDIO2}, V_{DDUSB})+3.6 V and 5.5V.
4. For operation with voltage higher than Min (V_{DD}, V_{DDA}, V_{DDIO2}, V_{DDUSB}) +0.3 V, the internal Pull-up and Pull-Down resistors must be disabled.
5. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax} (see *Section 7.7: Thermal characteristics*).
6. In low-power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax} (see *Section 7.7: Thermal characteristics*).

5.3.2 SMPS step-down converter

The device embeds an SMPS step down converter which requires the external components shown in below figure.

Figure 31. External components for SMPS step down converter



The following table summarizes the SMPS behavior depending on the main regulator range, VDD and consumption.

Table 28. SMPS modes summary

Ranges	Max AHB clock	V_{CORE}	SMPS mode	
			$V_{DD} \leq 2.05$ V	$V_{DD} > 2.05$ V
Range 0	110 MHz	1.28 V	Automatic Bypass mode $V_{15SMPS} = V_{DD}$	HP mode Max current consumption = 120 mA V_{15SMPS} = 1.6 V
Range 1	80 MHz	1.2 V	Automatic Bypass mode $V_{15SMPS} = V_{DD}$	HP mode Max current consumption = 80 mA V_{15SMPS} = 1.5 V
Range 2	26 MHz	1.0 V	Software Bypass mode(1) $V_{15SMPS} = V_{DD}$	LP mode or HP mode Max current consumption = 30 mA V_{15SMPS} = 1.3 V

1. There is no automatic SMPS bypass in Range 2. The user application should use PVD0 to monitor V_{DD} supply and request the SMPS Bypass mode.

Table 29. SMPS characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VDDSMPS	SMPS power supply		1.71(2)		3.6	V
V15SMPS	SMPS output voltage	Range 0	1.55	1.6	1.65	V
		Range 1	1.45	1.5	1.55	
		Range 2	1.25	1.3	1.35	
SR	SMPS output slew rate	Fast startup disabled SMPSFSTEN = 0	-	600	-	µs/V
		Fast startup enabled SMPSFSTEN = 1	-	120	-	

1. Guaranteed by design.
2. When VDDSMPS is less than 2.05V, the SMPS bypass mode is forced by hardware in Range 0 and Range 1. In Range 2, there is no automatic switch into SMPS bypass mode. It should be requested by software. Refer to *Table 28: SMPS modes summary*.

5.3.3 Operating conditions at power-up / power-down

The parameters given in *Table 30* are derived from tests performed under the ambient temperature condition summarized in *Table 27*.

Table 30. Operating conditions at power-up / power-down(1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	0	∞	µs/V
	V_{DD} fall time rate		10	∞	
t_{VDDA}	V_{DDA} rise time rate	-	0	∞	
	V_{DDA} fall time rate		10	∞	
t_{VDDUSB}	V_{DDUSB} rise time rate	-	0	∞	
	V_{DDUSB} fall time rate		10	∞	
t_{VDDIO2}	V_{DDIO2} rise time rate	-	0	∞	
	V_{DDIO2} fall time rate		10	∞	

1. At power-up, the V_{DD12} voltage should not be forced externally.

5.3.4 Embedded reset and power control block characteristics

The parameters given in *Table 31* are derived from tests performed under the ambient temperature conditions summarized in *Table 27: General operating conditions*.

Table 31. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions(1)	Min	Typ	Max	Unit
$t_{RSTTEMPO}$(2)	Reset temporization after BOR0 is detected	V_{DD} rising	-	250	400	µs
V_{BOR0}(2)	Brown-out reset threshold 0	Rising edge	1.62	1.66	1.7	V
		Falling edge	1.6	1.64	1.69	
V_{BOR1}	Brown-out reset threshold 1	Rising edge	2.06	2.1	2.14	V
		Falling edge	1.96	2	2.04	
V_{BOR2}	Brown-out reset threshold 2	Rising edge	2.26	2.31	2.35	V
		Falling edge	2.16	2.20	2.24	
V_{BOR3}	Brown-out reset threshold 3	Rising edge	2.56	2.61	2.66	V
		Falling edge	2.47	2.52	2.57	
V_{BOR4}	Brown-out reset threshold 4	Rising edge	2.85	2.90	2.95	V
		Falling edge	2.76	2.81	2.86	
V_{PVD0}	Programmable voltage detector threshold 0	Rising edge	2.1	2.15	2.19	V
		Falling edge	2	2.05	2.1	
V_{PVD1}	PVD threshold 1	Rising edge	2.26	2.31	2.36	V
		Falling edge	2.15	2.20	2.25	

Table 31. Embedded reset and power control block characteristics (continued)

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
V_{PVD2}	PVD threshold 2	Rising edge	2.41	2.46	2.51	V
		Falling edge	2.31	2.36	2.41	
V_{PVD3}	PVD threshold 3	Rising edge	2.56	2.61	2.66	V
		Falling edge	2.47	2.52	2.57	
V_{PVD4}	PVD threshold 4	Rising edge	2.69	2.74	2.79	V
		Falling edge	2.59	2.64	2.69	
V_{PVD5}	PVD threshold 5	Rising edge	2.85	2.91	2.96	V
		Falling edge	2.75	2.81	2.86	
V_{PVD6}	PVD threshold 6	Rising edge	2.92	2.98	3.04	V
		Falling edge	2.84	2.90	2.96	
V_{hyst_BORH0}	Hysteresis voltage of BORH0	Hysteresis in continuous mode	-	20	-	mV
		Hysteresis in other mode	-	30	-	
$V_{hyst\_BOR\_PVD}$	Hysteresis voltage of BORH (except BORH0) and PVD	-	-	100	-	mV
I_{DD} (BOR_PVD)[2]	BOR[3] (except BOR0) and PVD consumption from V_{DD}	-	-	1.1	1.6	µA
V_{PVM3}	V_{DDA} peripheral voltage monitoring	Rising edge	1.61	1.65	1.69	V
		Falling edge	1.6	1.64	1.68	
V_{PVM4}	V_{DDA} peripheral voltage monitoring	Rising edge	1.78	1.82	1.86	V
		Falling edge	1.77	1.81	1.85	
V_{hyst_PVM3}	PVM3 hysteresis	-	-	10	-	mV
V_{hyst_PVM4}	PVM4 hysteresis	-	-	10	-	mV
I_{DD} (PVM1/PVM2) (2)	PVM1 and PVM2 consumption from V_{DD}	-	-	0.2	-	µA
I_{DD} (PVM3/PVM4) (2)	PVM3 and PVM4 consumption from V_{DD}	-	-	2	-	µA

1. Continuous mode means Run/Sleep modes, or temperature sensor enable in Low-power run/Low-power sleep modes.
2. Guaranteed by design.
3. BOR0 is enabled in all modes (except shutdown) and its consumption is therefore included in the supply current characteristics tables.

5.3.5 Embedded voltage reference

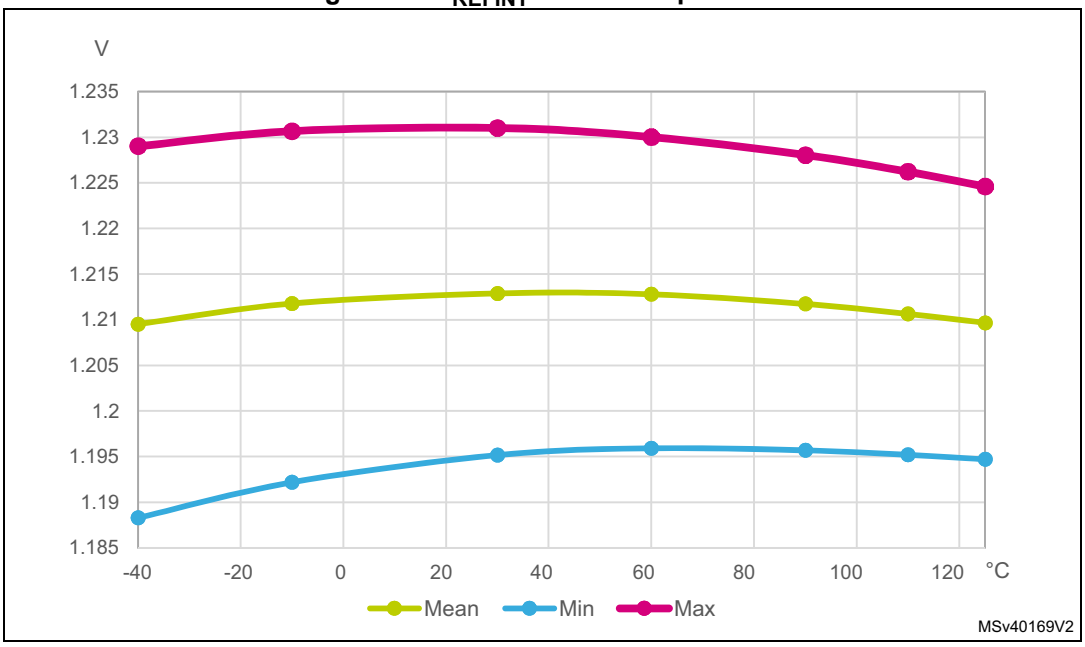
The parameters given in *Table 32* are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 27: General operating conditions*.

Table 32. Embedded internal voltage reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40 °C < T_A < +130 °C	1.182	1.212	1.232	V
$t_{S\_vrefint}$ (1)	ADC sampling time when reading the internal reference voltage	-	4(2)	-	-	µs
$t_{start\_vrefint}$	Start time of reference voltage buffer when ADC is enable	-	-	8	12(2)	µs
$I_{DD}(V_{REFINTBUF})$	V_{REFINT} buffer consumption from V_{DD} when converted by ADC	-	-	12.5	20(2)	µA
ΔV_{REFINT}	Internal reference voltage spread over the temperature range	V_{DD} = 3 V	-	5	7.5(2)	mV
T_{Coeff}	Average temperature coefficient	–40°C < T_A < +130°C	-	30	50(2)	ppm/°C
A_{Coeff}	Long term stability	1000 hours, T = 25°C	-	300	1000(2)	ppm
$V_{DDCoeff}$	Average voltage coefficient	3.0 V < V_{DD} < 3.6 V	-	250	1200(2)	ppm/V
V_{REFINT_DIV1}	1/4 reference voltage	-	24	25	26	% V_{REFINT}
V_{REFINT_DIV2}	1/2 reference voltage		49	50	51	
V_{REFINT_DIV3}	3/4 reference voltage		74	75	76	

1. The shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design.

Figure 32. V_{REFINT} versus temperature



5.3.6 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code

The current consumption is measured as described in *Section 5.1.7: Current consumption measurement*.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted with the minimum wait states number, depending on the f_{HCLK} frequency (refer to the table “Number of wait states according to CPU clock (HCLK) frequency” available in the RM0438 reference manual).
- When the peripherals are enabled $f_{PCLK} = f_{HCLK}$
- The voltage scaling range is adjusted to f_{HCLK} frequency as follows:
  - Voltage Range 0 for 80 MHz < f_{HCLK} <= 110 MHz
  - Voltage Range 1 for 26 MHz < f_{HCLK} <= 80 MHz
  - Voltage Range 2 for f_{HCLK} <= 26 MHz

The parameters given in *Table 33* to *Table 81* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 27: General operating conditions*.

Table 33. Current consumption in Run and Low-power run modes, code with data running from Flash in single Bank, ICACHE ON in 2-way

Symbol	Parameter	Conditions			TYP						
		-	Voltage scaling	f_{HCLK}	25°C	55°C	85°C	105°C	125°C	25°C	5
I_{DD} (Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disabled	Range 2	26 MHz	3.20	3.54	4.47	5.80	8.10	4.38	
				16 MHz	2.05	2.38	3.31	4.62	6.92	3.24	
				8 MHz	1.14	1.45	2.38	3.68	5.97	2.33	
				4 MHz	0.675	0.99	1.91	3.22	5.50	1.87	
				2 MHz	0.441	0.758	1.67	2.97	5.25	1.64	
				1 MHz	0.326	0.639	1.54	2.86	5.14	1.59	
				100 KHz	0.223	0.533	1.45	2.74	5.03	1.43	
			Range 0	110 MHz	16.7	17.3	18.7	20.5	23.7	19.07	2
			Range 1	80 MHz	11.4	11.9	13.2	14.8	17.7	13.33	1
				72 MHz	10.3	10.8	12.0	13.7	16.6	12.22	1
				64 MHz	9.20	9.68	10.9	12.6	15.4	11.10	1
				48 MHz	6.97	7.44	8.64	10.3	13.1	8.85	1
				32 MHz	4.73	5.18	6.36	7.97	10.8	6.61	1
				24 MHz	3.62	4.06	5.22	6.82	9.6	5.49	
				16 MHz	2.51	2.93	4.08	5.67	8.4	4.37	
I_{DD} (LPRun)	Supply current in Low-power run mode	$f_{HCLK} = f_{MSI}$ all peripherals disabled		2 MHz	424	779	1816	3274	5719	2026	5
				1 MHz	296	648	1686	3124	5588	1905	4
				400 KHz	192	561	1594	3047	5499	1832	4
				100 KHz	163	528	1559	3012	5469	1799	4

Table 34. Current consumption in Run and Low-power run modes, code with data running from Flash in single Bank, ICACHE ON in 1-way

Symbol	Parameter	Conditions			TYP						
		-	Voltage scaling	f_{HCLK}	25°C	55°C	85°C	105°C	125°C	25°C	55°C
I_{DD} (Run)	Supply current in Run mode	f_{HCLK} = f_{HSE} up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disabled	Range 2	26 MHz	3.10	3.44	4.37	5.69	8.01	4.28	6.74
				16 MHz	2.00	2.32	3.23	4.55	6.86	3.18	5.63
				8 MHz	1.11	1.42	2.33	3.64	5.93	2.30	4.73
				4 MHz	0.65	0.98	1.87	3.19	5.48	1.86	4.29
				2 MHz	0.43	0.74	1.65	2.97	5.24	1.64	4.06
				1 MHz	0.32	0.62	1.53	2.85	5.10	1.58	4.01
				100 KHz	0.22	0.52	1.43	2.75	5.01	1.43	3.85
			Range 0	110 MHz	16.1	16.7	18.2	20.0	23.2	18.54	22.63
			Range 1	80 MHz	11.0	11.5	12.8	14.5	17.3	12.97	16.53
				72 MHz	10.0	10.5	11.7	13.4	16.2	11.89	15.44
				64 MHz	8.90	9.38	10.6	12.3	15.1	10.81	14.35
				48 MHz	6.75	7.21	8.41	10.0	12.8	8.63	12.16
				32 MHz	4.59	5.03	6.22	7.82	10.6	6.46	9.97
				24 MHz	3.51	3.94	5.10	6.72	9.5	5.38	8.88
				16 MHz	2.43	2.85	3.99	5.59	8.4	4.3	7.8
I_{DD} (LPRun)	Supply current in Low-power run mode	f_{HCLK} = f_{MSI} all peripherals disabled		2 MHz	416	770	1781	3249	5708	2014	4968
				1 MHz	291	633	1659	3127	5575	1899	4930
				400 KHz	194	557	1583	3043	5502	1827	4765
				100 KHz	147	519	1542	3020	5462	1795	4584

Table 35. Current consumption in Run and Low-power run modes, code with data running from Flash in single Bank, ICACHE disabled

Symbol	Parameter	Conditions			TYP						
		-	Voltage scaling	f_{HCLK}	25°C	55°C	85°C	105°C	125°C	25°C	55°C
I_{DD} (Run)	Supply current in Run mode	f_{HCLK} = f_{HSE} up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disabled	Range 2	26 MHz	4.08	4.43	5.36	6.72	9.02	5.38	7.84
				16 MHz	2.65	2.98	3.91	5.22	7.55	3.93	6.38
				8 MHz	1.43	1.76	2.67	3.99	6.26	2.67	5.11
				4 MHz	0.82	1.14	2.05	3.36	5.65	2.04	4.48
				2 MHz	0.51	0.82	1.75	3.05	5.31	1.73	4.16
				1 MHz	0.36	0.68	1.59	2.89	5.16	1.65	4.08
				100 KHz	0.22	0.53	1.45	2.76	5.00	1.43	3.86
			Range 0	110 MHz	18.8	19.4	20.9	22.8	25.9	19.97	24.02
			Range 1	80 MHz	14.1	14.6	15.9	17.6	20.5	16.16	19.71
				72 MHz	12.8	13.3	14.5	16.2	19.1	14.80	18.34
				64 MHz	11.79	12.30	13.5	15.2	18.1	13.90	17.45
				48 MHz	8.87	9.37	10.63	12.3	15.1	10.97	14.51
				32 MHz	6.12	6.58	7.80	9.44	12.2	8.22	11.74
				24 MHz	4.66	5.11	6.29	7.92	10.7	6.70	10.20
				16 MHz	3.26	3.70	4.86	6.47	9.2	5.28	8.77
I_{DD} (LPRun)	Supply current in Low-power run mode	f_{HCLK} = f_{MSI} all peripherals disabled		2 MHz	511	866	1890	3353	5834	2122	5256
				1 MHz	344	692	1715	3168	5642	1949	5022
				400 KHz	203	591	1603	3062	5505	1852	4828
				100 KHz	159	531	1553	3018	5468	1802	4590

Table 36. Current consumption in Run mode, code with data processin running from Flash in single bank, ICACHE ON in 2-way and power supplied by internal SMPS step down converter

Symbol	Parameter	Conditions			TYP						
		-	Voltage scaling	f_{HCLK}	25°C	55°C	85°C	105°C	125°C	25°C	55
I_{DD} (Run)	Supply current in Run mode	f_{HCLK} = f_{HSE} up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disabled	Range 2 SMPS LP mode	26 MHz	1.87	1.95	2.41	3.09	5.03	1.92	2.
				16 MHz	1.23	1.33	1.78	2.45	4.33	1.31	2.
				8 MHz	0.72	0.83	1.28	1.95	3.79	0.81	1.
				4 MHz	0.46	0.58	1.03	1.69	3.52	0.56	1.
				2 MHz	0.33	0.46	0.91	1.55	3.38	0.44	1.
				1 MHz	0.27	0.39	0.84	1.49	3.311	0.41	1.
				100 KHz	0.21	0.34	0.78	1.44	3.25	0.32	1.
			Range 0 SMPS HP mode	110 MHz	11.21	11.76	12.72	13.98	17.58	11.49	13.
I_{DD} (Run)	Supply current in Run mode	f_{HCLK} = f_{HSE} up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disabled	Range 1 SMPS HP mode	80 MHz	7.00	7.28	8.37	9.41	11.92	7.52	8.
				72 MHz	6.34	6.61	7.57	8.67	11.20	6.87	8.
				64 MHz	5.68	5.94	6.73	7.96	10.44	6.19	7.
				48 MHz	4.36	4.61	5.28	6.49	8.97	4.82	6.
				32 MHz	3.03	3.25	3.91	4.86	7.48	3.43	4.
				24 MHz	2.36	2.57	3.21	4.13	6.73	2.73	4.
				16 MHz	1.69	1.90	2.53	3.43	5.97	2.03	3.

Table 37. Current consumption in Run mode, code with data processin running from Flash in single bank, ICACHE ON in 1-way and power supplied by internal SMPS step down converter

Symbol	Parameter	Conditions			TYP					
		-	Voltage scaling	f_{HCLK}	25°C	55°C	85°C	105°C	125°C	25°C
I_{DD} (Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disabled	Range 2 SMPS LP mode	26 MHz	1.82	1.90	2.36	3.03	4.96	1.88
				16 MHz	1.20	1.30	1.75	2.41	4.31	1.28
				8 MHz	0.70	0.82	1.27	1.93	3.75	0.8
				4 MHz	0.45	0.58	1.02	1.68	3.51	0.56
				2 MHz	0.33	0.45	0.90	1.55	3.37	0.44
				1 MHz	0.26	0.39	0.84	1.49	3.30	0.4
				100 KHz	0.21	0.33	0.78	1.43	3.24	0.32
			Range 0 SMPS HP mode	110 MHz	10.80	11.38	12.35	13.61	17.20	11.18
I_{DD} (Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disabled	Range 1 SMPS HP mode	80 MHz	6.79	7.06	8.152	9.17	11.65	7.32
				72 MHz	6.15	6.42	7.38	8.46	10.92	6.68
				64 MHz	5.51	5.77	6.62	7.77	10.22	6.02
				48 MHz	4.23	4.48	5.15	6.34	8.814	4.69
				32 MHz	2.94	3.17	3.82	4.76	7.341	3.34
				24 MHz	2.29	2.51	3.15	4.06	6.62	2.66
				16 MHz	1.65	1.85	2.49	3.39	5.89	1.99

Table 38. Current consumption in Run mode, code with data processin running from Flash in single bank, ICACHE disabled and power supplied by internal SMPS step down converter

Symbol	Parameter	Conditions			TYP					
		-	Voltage scaling	f_{HCLK}	25°C	55°C	85°C	105°C	125°C	25°C
I_{DD} (Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disabled	Range 2 SMPS LP mode	26 MHz	2.38	2.44	2.91	3.60	5.55	2.43
				16 MHz	1.57	1.66	2.11	2.79	4.68	1.64
				8 MHz	0.89	0.99	1.45	2.11	3.97	0.98
				4 MHz	0.54	0.67	1.11	1.77	3.59	0.65
				2 MHz	0.37	0.50	0.94	1.60	3.42	0.48
				1 MHz	0.29	0.41	0.86	1.52	3.33	0.44
				100 KHz	0.21	0.34	0.78	1.43	3.24	0.32
			Range 0 SMPS HP mode	110 MHz	12.87	13.29	14.25	15.62	18.91	13.02
			Range 1 SMPS HP mode	80 MHz	8.69	9.01	10.21	11.24	13.82	9.35
				72 MHz	7.88	8.23	9.30	10.34	12.83	8.53
				64 MHz	7.28	7.56	8.67	9.70	12.17	7.86
				48 MHz	5.56	5.81	6.66	7.79	10.30	6.1
				32 MHz	3.87	4.11	4.79	5.87	8.40	4.33
				24 MHz	2.99	3.21	3.87	4.84	7.41	3.41
				16 MHz	2.15	2.36	3.00	3.92	6.45	2.52

Table 39. Current consumption in Run and Low-power run modes, code with data running from Flash in dual bank, ICACHE ON in 2-way

Symbol	Parameter	Conditions			TYP						
		-	Voltage scaling	f_{HCLK}	25°C	55°C	85°C	105°C	125°C	25°C	55°C
I_{DD} (Run)	Supply current in Run mode	f_{HCLK} = f_{HSE} up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disabled	Range 2	26 MHz	3.19	3.53	4.57	6.08	8.87	4.38	6.84
				16 MHz	2.05	2.38	3.41	4.90	7.67	3.24	5.69
				8 MHz	1.13	1.45	2.47	3.95	6.71	2.33	4.77
				4 MHz	0.67	0.99	1.98	3.48	6.22	1.87	4.30
				2 MHz	0.43	0.75	1.76	3.24	5.97	1.64	4.07
				1 MHz	0.32	0.63	1.63	3.13	5.85	1.59	4.02
				100 KHz	0.22	0.53	1.53	3.00	5.75	1.43	3.85
			Range 0	110 MHz	16.66	17.28	18.84	20.97	24.75	19.07	23.1
			Range 1	80 MHz	11.39	11.91	13.30	15.22	18.68	13.33	16.8
				72 MHz	10.28	10.79	12.16	14.08	17.52	12.22	15.7
				64 MHz	9.18	9.68	11.02	12.93	16.35	11.10	14.6
				48 MHz	6.95	7.43	8.76	10.63	14.02	8.85	12.3
				32 MHz	4.72	5.17	6.48	8.33	11.68	6.61	10.1
				24 MHz	3.61	4.05	5.35	7.20	10.50	5.49	8.98
				16 MHz	2.50	2.92	4.20	6.04	9.33	4.37	7.85
I_{DD} (LPRun)	Supply current in Low-power run mode	f_{HCLK} = f_{MSI} all peripherals disabled		2 MHz	402.64	785.95	1919	3558	6501	2025	4984
				1 MHz	274.43	651.32	1775	3435	6367	1907	4958
				400 KHz	184.36	568.08	1697	3359	6278	1835	4759
				100 KHz	164.07	526.82	1660	3306	6238	1797	4578

Table 40. Current consumption in Run and Low-power run modes, code with data running from Flash in dual bank, ICACHE ON in 1-way

Symbol	Parameter	Conditions			TYP						
		-	Voltage scaling	f_{HCLK}	25°C	55°C	85°C	105°C	125°C	25°C	55°C
I_{DD} (Run)	Supply current in Run mode	f_{HCLK} = f_{HSE} up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disabled	Range 2	26 MHz	3.10	3.44	4.45	5.99	8.76	4.28	6.74
				16 MHz	1.99	2.32	3.33	4.84	7.60	3.18	5.63
				8 MHz	1.10	1.42	2.43	3.93	6.67	2.30	4.73
				4 MHz	0.65	0.97	1.96	3.47	6.19	1.86	4.29
				2 MHz	0.43	0.76	1.75	3.24	5.97	1.64	4.06
				1 MHz	0.31	0.63	1.63	3.14	5.84	1.58	4.01
				100 KHz	0.21	0.53	1.52	3.01	5.75	1.43	3.85
			Range 0	110 MHz	16.14	16.75	18.31	20.43	24.12	18.54	22.62
			Range 1	80 MHz	11.03	11.54	12.91	14.83	18.22	12.97	16.52
				72 MHz	9.96	10.46	11.81	13.73	17.10	11.89	15.44
				64 MHz	8.89	9.39	10.72	12.62	16.00	10.81	14.35
				48 MHz	6.74	7.21	8.52	10.41	13.77	8.63	12.16
				32 MHz	4.58	5.04	6.31	8.19	11.47	6.46	9.97
				24 MHz	3.50	3.94	5.22	7.07	10.36	5.38	8.87
				16 MHz	2.42	2.85	4.10	5.93	9.21	4.30	7.78
I_{DD} (LPRun)	Supply current in Low-power run mode	f_{HCLK} = f_{MSI} all peripherals disabled		2 MHz	395.28	772.83	1907	3571	6492	2013	4976
				1 MHz	289.98	641.73	1775	3418	6339	1907	4922
				400 KHz	186.68	557.53	1698	3343	6271	1823	4765
				100 KHz	165.54	523.33	1666	3299	6245	1799	4595

Table 41. Current consumption in Run and Low-power run modes, code with data running from Flash in dual bank, ICACHE disabled

Symbol	Parameter	Conditions			TYP						
		-	Voltage scaling	f_{HCLK}	25°C	55°C	85°C	105°C	125°C	25°C	55°C
I_{DD} (Run)	Supply current in Run mode	f_{HCLK} = f_{HSE} up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disabled	Range 2	26 MHz	4.17	4.52	5.55	7.10	9.86	5.38	7.84
				16 MHz	2.73	3.07	4.09	5.63	8.40	3.93	6.38
				8 MHz	1.47	1.80	2.81	4.32	7.05	2.67	5.11
				4 MHz	0.84	1.166	2.16	3.66	6.39	2.04	4.47
				2 MHz	0.52	0.84	1.84	3.33	6.05	1.73	4.16
				1 MHz	0.36	0.68	1.68	3.18	5.89	1.65	4.08
				100 KHz	0.22	0.53	1.53	3.03	5.74	1.43	3.86
			Range 0	110 MHz	17.20	17.81	19.35	21.47	25.17	19.96	24.02
			Range 1	80 MHz	13.93	14.47	15.86	17.80	21.23	16.17	19.70
				72 MHz	12.60	13.12	14.51	16.45	19.86	14.80	18.34
				64 MHz	11.82	12.34	13.73	15.65	19.05	13.90	17.45
				48 MHz	8.922	9.42	10.78	12.69	16.08	10.97	14.51
				32 MHz	6.24	6.72	8.03	9.92	13.28	8.22	11.74
				24 MHz	4.75	5.21	6.50	8.35	11.67	6.70	10.20
				16 MHz	3.38	3.83	5.09	6.93	10.22	5.28	8.77
I_{DD} (LPRun)	Supply current in Low-power run mode	f_{HCLK} = f_{MSI} all peripherals disabled		2 MHz	483.64	889.56	2022	3671	6622	2109	5283
				1 MHz	332.24	705.19	1836	3468	6424	1954	5032
				400 KHz	206.59	588.25	1722	3355	6314	1849	4802
				100 KHz	156.41	527.80	1666	3315	6247	1809	4600

Table 42. Current consumption in Run mode, code with data processir running from Flash in dual bank, ICACHE ON in 2-way and power supplied by internal SMPS step down converter

Symbol	Parameter	Conditions			TYP					
		-	Voltage scaling	f_{HCLK}	25°C	55°C	85°C	105°C	125°C	25°C
I_{DD} (Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disabled	Range 2 SMPS LP mode	26 MHz	1.85	1.94	2.41	3.14	4.40	1.93
				16 MHz	1.21	1.33	1.79	2.48	3.76	1.31
				8 MHz	0.70	0.83	1.29	1.98	3.25	0.81
				4 MHz	0.45	0.58	1.03	1.77	3.00	0.56
				2 MHz	0.32	0.46	0.90	1.60	2.88	0.44
				1 MHz	0.26	0.39	0.84	1.54	2.79	0.41
				100 KHz	0.20	0.33	0.79	1.51	2.74	0.32
			Range 0 SMPS HP mode	110 MHz	11.05	11.73	12.72	14.01	16.84	11.49
			Range 1 SMPS HP mode	80 MHz	6.96	7.27	8.38	9.46	11.35	7.53
				72 MHz	6.30	6.61	7.62	8.69	10.58	6.87
				64 MHz	5.65	5.94	6.80	8.00	9.88	6.19
				48 MHz	4.33	4.60	5.29	6.51	8.40	4.83
				32 MHz	3.00	3.25	3.92	4.92	6.92	3.43
				24 MHz	2.33	2.57	3.22	4.15	6.15	2.73
				16 MHz	1.67	1.89	2.53	3.47	5.33	2.03

Table 43. Current consumption in Run mode, code with data processir running from Flash in dual bank, ICACHE ON in 1-way and power supplied by internal SMPS step down converter

Symbol	Parameter	Conditions			TYP					
		-	Voltage scaling	f_{HCLK}	25°C	55°C	85°C	105°C	125°C	25°C
I_{DD} (Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disabled	Range 2 SMPS LP mode	26 MHz	1.80	1.89	2.37	3.07	4.35	1.88
				16 MHz	1.18	1.30	1.76	2.46	3.72	1.28
				8 MHz	0.69	0.82	1.27	1.98	3.23	0.8
				4 MHz	0.44	0.58	1.02	1.72	2.98	0.56
				2 MHz	0.32	0.46	0.90	1.59	2.86	0.44
				1 MHz	0.26	0.39	0.84	1.53	2.79	0.4
				100 KHz	0.20	0.33	0.78	1.48	2.73	0.32
			Range 0 SMPS HP mode	110 MHz	10.51	11.37	12.33	13.63	16.26	11.18
			Range 1 SMPS HP mode	80 MHz	6.75	7.06	8.15	9.21	11.07	7.33
				72 MHz	6.12	6.41	7.39	8.50	10.37	6.68
				64 MHz	5.48	5.77	6.65	7.82	9.68	6.02
				48 MHz	4.20	4.48	5.15	6.38	8.25	4.69
				32 MHz	2.92	3.16	3.82	4.79	6.81	3.34
				24 MHz	2.27	2.51	3.15	4.12	6.06	2.66
				16 MHz	1.63	1.85	2.49	3.44	5.26	1.99

Table 44. Current consumption in Run mode, code with data processin running from Flash in dual bank, ICACHE disabled and power supplied by internal SMPS step down converter

Symbol	Parameter	Conditions			TYP					
		-	Voltage scaling	f_{HCLK}	25°C	55°C	85°C	105°C	125°C	25°C
I_{DD} (Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disabled	Range 2 SMPS LP mode	26 MHz	2.40	2.49	2.97	3.67	4.94	2.47
				16 MHz	1.61	1.71	2.17	2.87	4.16	1.68
				8 MHz	0.90	1.02	1.47	2.18	3.44	1
				4 MHz	0.55	0.67	1.12	1.82	3.07	0.66
				2 MHz	0.37	0.51	0.95	1.64	2.89	0.49
				1 MHz	0.286	0.42	0.87	1.55	2.81	0.44
				100 KHz	0.20	0.34	0.79	1.48	2.74	0.32
			Range 0 SMPS HP mode	110 MHz	11.59	12.15	13.24	14.24	16.59	11.99
			Range 1 SMPS HP mode	80 MHz	8.53	8.95	10.06	11.12	13.07	9.31
				72 MHz	7.74	8.07	9.20	10.26	12.17	8.47
				64 MHz	7.26	7.57	8.71	9.75	11.64	7.95
				48 MHz	5.54	5.82	6.66	7.87	9.74	6.15
				32 MHz	3.92	4.18	4.85	5.98	7.91	4.42
				24 MHz	3.03	3.27	3.92	4.91	6.93	3.48
				16 MHz	2.20	2.43	3.07	4.03	5.95	2.59

Table 45. Current consumption in Run and Low-power run modes, code with data processing running from SRAM1

Symbol	Parameter	Conditions			TYP						
		-	Voltage scaling	f_{HCLK}	25°C	55°C	85°C	105°C	125°C	25°C	5
I_{DD} (Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disabled	Range 2	26 MHz	3.25	3.59	4.62	6.12	8.92	4.44	6
				16 MHz	2.08	2.41	3.43	4.93	7.69	3.27	5
				8 MHz	1.15	1.47	2.47	3.97	6.73	2.35	4
				4 MHz	0.68	1.00	1.99	3.51	6.23	1.88	4
				2 MHz	0.44	0.76	1.75	3.25	5.97	1.65	4
				1 MHz	0.32	0.64	1.64	3.14	5.86	1.59	4
				100 KHz	0.22	0.53	1.52	3.03	5.76	1.42	3
			Range 0	110 MHz	16.99	17.57	19.10	21.22	24.94	19.40	23
			Range 1	80 MHz	11.63	12.13	13.48	15.38	18.76	13.57	1
				72 MHz	10.50	10.99	12.33	14.22	17.62	12.42	15
				64 MHz	9.37	9.85	11.18	13.07	16.43	11.28	14
				48 MHz	7.10	7.56	8.87	10.74	14.10	8.99	1
				32 MHz	4.826	5.27	6.55	8.40	11.70	6.70	1
				24 MHz	3.68	4.11	5.37	7.23	10.54	5.55	9
				16 MHz	2.54	2.97	4.22	6.05	9.34	4.41	7
I_{DD} (LPRun)	Supply current in Low-power run mode	$f_{HCLK} = f_{MSI}$ all peripherals disabled FLASH in power-down		2 MHz	385.23	772.80	1911	3545	6506	2010	4
				1 MHz	271.61	633.31	1776	3405	6382	1896	4
				400 KHz	198.95	554.43	1694	3337	6298	1818	4
				100 KHz	142.82	517.78	1638	3286	6267	1423	3

Table 46. Current consumption in Run mode, code with data processing ru from SRAM1 and power supplied by internal SMPS step down converte

Symbol	Parameter	Conditions			TYP					
		-	Voltage scaling	f_{HCLK}	25°C	55°C	85°C	105°C	125°C	25°C
I_{DD} (Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disabled	Range 2 SMPS LP mode	26 MHz	1.88	1.99	2.46	3.15	4.42	1.96
				16 MHz	1.24	1.35	1.81	2.51	3.76	1.33
				8 MHz	0.72	0.85	1.29	1.99	3.24	0.82
				4 MHz	0.46	0.59	1.04	1.73	2.97	0.57
				2 MHz	0.32	0.46	0.91	1.60	2.85	0.44
				1 MHz	0.26	0.40	0.84	1.53	2.77	0.41
				100 KHz	0.20	0.34	0.78	1.48	2.71	0.32
			Range 0 SMPS HP mode	110 MHz	11.28	12.01	12.99	14.29	17.00	12.06
			Range 1 SMPS HP mode	80 MHz	7.10	7.42	8.55	9.55	11.47	8.33
				72 MHz	6.44	6.74	7.80	8.84	10.70	7.52
				64 MHz	5.76	6.05	6.89	8.10	9.95	6.8
				48 MHz	4.42	4.69	5.37	6.60	8.46	5.34
				32 MHz	3.06	3.31	3.96	4.93	6.93	3.86
				24 MHz	2.38	2.61	3.26	4.20	6.16	3.15
				16 MHz	1.70	1.92	2.55	3.51	5.32	2.45

Table 47. Current consumption in Run and Low-power run modes, code with data running from SRAM2

Symbol	Parameter	Conditions			TYP						
		-	Voltage scaling	f_{HCLK}	25°C	55°C	85°C	105°C	125°C	25°C	
I_{DD} (Run)	Supply current in Run mode	f_{HCLK} = f_{HSE} up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disabled	Range 2	26 MHz	3.20	3.53	4.55	6.08	8.86	4.33	
				16 MHz	2.05	2.38	3.40	4.90	7.67	3.19	
				8 MHz	1.13	1.45	2.46	3.97	6.71	2.28	
				4 MHz	0.67	0.99	1.99	3.47	6.21	1.82	
				2 MHz	0.43	0.76	1.75	3.24	5.97	1.59	
				1 MHz	0.32	0.63	1.63	3.13	5.86	1.53	
				100 KHz	0.22	0.53	1.53	3.01	5.74	1.37	
			Range 0	110 MHz	16.71	17.32	18.86	20.97	24.66	19.04	2
			Range 1	80 MHz	11.43	11.94	13.30	15.21	18.64	13.29	1
				72 MHz	10.32	10.82	12.16	14.07	17.48	12.17	1
				64 MHz	9.219	9.70	11.03	12.94	16.31	11.05	1
				48 MHz	6.98	7.44	8.77	10.63	13.98	8.79	1
				32 MHz	4.746	5.19	6.48	8.33	11.65	6.54	1
				24 MHz	3.62	4.06	5.33	7.17	10.49	5.42	
				16 MHz	2.50	2.93	4.19	6.02	9.29	4.29	
I_{DD}(LPRun)	Supply current in Low-power run mode	f_{HCLK} = f_{MSI} all peripherals disabled FLASH in power-down		2 MHz	386.41	774.71	1901	3546	6475	1946	2
				1 MHz	276.23	635.13	1767	3445	6360	1829	2
				400 KHz	196.75	552.97	1679	3339	6278	1757	2
				100 KHz	146.57	513.87	1644	3299	6249	1373	2

Table 48. Current consumption in Run mode, code with data processin running from SRAM2 and power supplied by internal SMPS step down con

Symbol	Parameter	Conditions			TYP					
		-	Voltage scaling	f_{HCLK}	25°C	55°C	85°C	105°C	125°C	25°C
I_{DD} (Run)	Supply current in Run mode	f_{HCLK} = f_{HSE} up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disabled	Range 2 SMPS LP mode	26 MHz	1.86	1.96	2.43	3.12	4.43	2.22
				16 MHz	1.22	1.33	1.79	2.50	3.75	1.61
				8 MHz	0.71	0.83	1.28	1.99	3.24	1.11
				4 MHz	0.456	0.58	1.03	1.74	2.99	0.86
				2 MHz	0.32	0.46	0.90	1.60	2.86	0.74
				1 MHz	0.26	0.40	0.84	1.54	2.79	0.71
				100 KHz	0.20	0.34	0.78	1.49	2.73	0.62
			Range 0 SMPS HP mode	110 MHz	11.04	11.78	12.75	14.05	16.87	12.16
			Range 1 SMPS HP mode	80 MHz	7.00	7.29	8.40	9.44	11.33	8.23
				72 MHz	6.34	6.62	7.64	8.72	10.59	7.49
				64 MHz	5.68	5.95	6.82	8.00	9.86	6.8
				48 MHz	4.35	4.61	5.30	6.51	8.38	5.39
				32 MHz	3.02	3.26	3.91	4.89	6.89	3.98
				24 MHz	2.35	2.58	3.22	4.18	6.11	3.28
				16 MHz	1.68	1.90	2.53	3.49	5.31	2.58

Table 49. Typical current consumption in Run and Low-power run mod with different codes running from Flash, ICACHE ON (2-way)

Symbol	Parameter	Conditions			TYP Single Bank Mode	TYP Dual Bank Mode
		-	Voltage scaling	Code	25°C	25°C
I_{DD} (Run)	Supply current in Run mode	$f_{HCLK}=f_{HSE}$ up to 48 MHZ included, bypass mode PLL ON above 48 MHz all peripherals disabled	Range2 f_{HCLK}=26MHz	Reduced code	3.20	3.19
				Coremark	3.43	3.43
				Dhrystone2.1	3.66	3.64
				Fibonacci	3.06	3.05
				While	2.77	2.77
			Range 1 fHCLK=80 MHz	Reduced code	11.4	11.4
				Coremark	12.2	12.2
				Dhrystone2.1	13.1	13.0
				Fibonacci	10.8	10.8
				While	9.9	9.9
			Range 0 f_{HCLK}= 110 MHz	Reduced code	16.7	16.7
				Coremark	18.0	18.0
				Dhrystone2.1	19.1	19.0
				Fibonacci	15.8	15.8
				While	14.5	14.5
I_{DD} (LPRun)	Supply current in Low-power run	f_{HCLK} = f_{MSI} = 2 MHz all peripherals disabled		Reduced code	424	403
				Coremark	447	415
				Dhrystone2.1	477	432
				Fibonacci	427	383
				While	350	369

Table 50. Typical current consumption in Run mode with SMPS, with different codes running from Flash, ICACHE ON (2-way)

Symbol	Parameter	Conditions			TYP Single Bank Mode	TYP Dual Bank Mode
		-	Voltage scaling	Code	25°C	25°C
I_{DD} (Run)	Supply current in Run mode	$f_{HCLK}=f_{HSE}$ up to 48 MHZ included, bypass mode PLL ON above 48 MHz all peripherals disabled	Range2, SMPS LP f_{HCLK}=26 MHz	Reduced code	1.88	1.85
				Coremark	2.00	1.98
				Dhrystone2.1	2.13	2.09
				Fibonacci	1.79	1.77
				While	1.65	1.64
			Range 1, SMPS HP fHCLK=80 MHz	Reduced code	7.0	7.0
				Coremark	7.5	7.5
				Dhrystone2.1	8.0	7.9
				Fibonacci	6.7	6.6
				While	6.1	6.1
			Range 0, SMPS HP f_{HCLK}= 110 MHz	Reduced code	11.2	11.1
				Coremark	12.2	12.1
				Dhrystone2.1	13.0	12.9
				Fibonacci	10.6	10.6
				While	9.3	9.3

Table 51. Typical current consumption in Run and Low-power run mod with different codes running from Flash, ICACHE ON (1-way)

Symbol	Parameter	Conditions			TYP Single Bank Mode	TYP Dual Bank Mode
		-	Voltage scaling	Code	25°C	25°C
I_{DD} (Run)	Supply current in Run mode	$f_{HCLK}=f_{HSE}$ up to 48 MHZ included, bypass mode PLL ON above 48 MHz all peripherals disabled	Range2 f_{HCLK}=26 MHz	Reduced code	3.10	3.10
				Coremark	3.26	3.26
				Dhrystone2.1	3.48	3.47
				Fibonacci	2.95	2.95
				While	2.73	2.72
			Range 1 fHCLK=80 MHz	Reduced code	11.0	11.0
				Coremark	11.6	11.6
				Dhrystone2.1	12.4	12.4
				Fibonacci	10.4	10.4
				While	9.7	9.7
			Range 0 f_{HCLK}= 110 MHz	Reduced code	16.1	16.1
				Coremark	17.0	17.0
				Dhrystone2.1	18.2	18.1
				Fibonacci	15.2	15.2
				While	14.2	14.2
I_{DD} (LPRun)	Supply current in Low-power run	f_{HCLK} = f_{MSI} = 2 MHz all peripherals disabled		Reduced code	416	395
				Coremark	425	389
				Dhrystone2.1	451	405
				Fibonacci	392	375
				While	355	372

Table 52. Typical current consumption in Run mode with SMPS, with different codes running from Flash, ICACHE ON (1-way)

Symbol	Parameter	Conditions			TYP Single Bank Mode	TYP Dual Bank Mode
		-	Voltage scaling	Code	25°C	25°C
I_{DD} (Run)	Supply current in Run mode	$f_{HCLK}=f_{HSE}$ up to 48 MHZ included, bypass mode PLL ON above 48 MHz all peripherals disabled	Range2, SMPS LP f_{HCLK}=26 MHz	Reduced code	1.82	1.80
				Coremark	1.91	1.89
				Dhrystone2.1	2.03	2.00
				Fibonacci	1.74	1.72
				While	1.63	1.61
			Range 1, SMPS HP fHCLK=80 MHz	Reduced code	6.8	6.8
				Coremark	7.1	7.1
				Dhrystone2.1	7.6	7.6
				Fibonacci	6.4	6.4
				While	6.0	6.0
			Range 0, SMPS HP f_{HCLK}= 110 MHz	Reduced code	10.8	10.5
				Coremark	11.5	11.4
				Dhrystone2.1	12.4	12.2
				Fibonacci	10.0	10.0
				While	9.2	9.1

Table 53. Typical current consumption in Run and Low-power run mod with different codes running from Flash, ICACHE disabled

Symbol	Parameter	Conditions			TYP Single Bank Mode	TYP Dual Bank Mode
		-	Voltage scaling	Code	25°C	25°C
I_{DD} (Run)	Supply current in Run mode	$f_{HCLK}=f_{HSE}$ up to 48 MHZ included, bypass mode PLL ON above 48 MHz all peripherals disabled	Range2 f_{HCLK}=26 MHz	Reduced code	4.08	4.17
				Coremark	4.42	4.22
				Dhrystone2.1	4.56	4.41
				Fibonacci	3.62	3.55
				While	3.04	3.14
			Range 1 fHCLK=80 MHz	Reduced code	14.1	13.9
				Coremark	13.6	12.2
				Dhrystone2.1	12.5	12.5
				Fibonacci	12.1	11.3
				While	10.9	11.3
			Range 0 f_{HCLK}= 110 MHz	Reduced code	18.8	17.2
				Coremark	17.5	15.2
				Dhrystone2.1	17.7	15.5
				Fibonacci	16.6	15.1
				While	15.9	16.5
I_{DD}(LPRun)	Supply current in Low-power run	f_{HCLK} = f_{MSI} = 2MHz all peripherals disabled		Reduced code	511	484
				Coremark	577	550
				Dhrystone2.1	599	551
				Fibonacci	470	462
				While	416	398

Table 54. Typical current consumption in Run mode with internal SMP with different codes running from Flash, ICACHE disabled

Symbol	Parameter	Conditions			TYP Single Bank Mode	TYP Dual Bank Mode
		-	Voltage scaling	Code	25°C	25°C
I_{DD} (Run)	Supply current in Run mode	$f_{HCLK}=f_{HSE}$ up to 48 MHZ included, bypass mode PLL ON above 48 MHz all peripherals disabled	Range2, SMPS LP f_{HCLK}=26 MHz	Reduced code	2.38	2.41
				Coremark	2.59	2.44
				Dhrystone2.1	2.67	2.55
				Fibonacci	2.13	2.07
				While	1.80	1.86
			Range 1, SMPS HP fHCLK=80 MHz	Reduced code	8.7	8.5
				Coremark	8.4	7.5
				Dhrystone2.1	8.6	7.7
				Fibonacci	7.5	7.0
				While	6.8	7.0
			Range 0, SMPS HP f_{HCLK}= 110 MHz	Reduced code	12.9	11.6
				Coremark	11.9	10.1
				Dhrystone2.1	12.0	10.4
				Fibonacci	11.3	10.1
				While	10.7	11.1

Table 55. Typical current consumption in Run and Low-power run mod with different codes running from SRAM1

Symbol	Parameter	Conditions			T
		-	Voltage scaling	Code	25
I_{DD} (Run)	Supply current in Run mode	$f_{HCLK}=f_{HSE}$ up to 48 MHZ included, bypass mode PLL ON above 48 MHz all peripherals disabled	Range2 f_{HCLK}=26MHz	Reduced code	3
				Coremark	3
				Dhrystone2.1	3
				Fibonacci	3
				While	3
			Range 1 fHCLK=80 MHz	Reduced code	1
				Coremark	12
				Dhrystone2.1	1
				Fibonacci	1
				While	13
			Range 0 f_{HCLK}= 110 MHz	Reduced code	1
				Coremark	17
				Dhrystone2.1	1
				Fibonacci	1
				While	2
I_{DD}(LPRun)	Supply current in Low-power run	f_{HCLK} = f_{MSI} = 2MHz all peripherals disabled		Reduced code	3
				Coremark	4
				Dhrystone2.1	3
				Fibonacci	4
				While	4

Table 56. Typical current consumption in Run mode with internal SMP with different codes running from SRAM1

Symbol	Parameter	Conditions			
		-	Voltage scaling	Code	
I_{DD} (Run)	Supply current in Run mode	$f_{HCLK}=f_{HSE}$ up to 48 MHZ included, bypass mode PLL ON above 48 MHz all peripherals disabled	Range2, LP f_{HCLK}=26MHz	Reduced code	
				Coremark	
				Dhrystone2.1	
				Fibonacci	
				While	
			Range 1, HP fHCLK=80 MHz	Reduced code	
				Coremark	
				Dhrystone2.1	
				Fibonacci	
				While	
			Range 0, HP f_{HCLK}= 110 MHz	Reduced code	
				Coremark	
				Dhrystone2.1	
				Fibonacci	
				While	

Table 57. Typical current consumption in Run and Low-power run mod with different codes running from SRAM2

Symbol	Parameter	Conditions			
		-	Voltage scaling	Code	
I_{DD} (Run)	Supply current in Run mode	$f_{HCLK}=f_{HSE}$ up to 48 MHZ included, bypass mode PLL ON above 48 MHz all peripherals disabled	Range2 f_{HCLK}=26MHz	Reduced code	
				Coremark	
				Dhrystone2.1	
				Fibonacci	
				While	
			Range 1 fHCLK=80 MHz	Reduced code	
				Coremark	
				Dhrystone2.1	
				Fibonacci	
				While	
			Range 0 f_{HCLK}= 110 MHz	Reduced code	
				Coremark	
				Dhrystone2.1	
				Fibonacci	
				While	
I_{DD} (LPRun)	Supply current in Low-power run	f_{HCLK} = f_{MSI} = 2MHz all peripherals disabled		Reduced code	
				Coremark	
				Dhrystone2.1	
				Fibonacci	
				While	

Table 58. Typical current consumption in Run mode with internal SMP with different codes running from SRAM2

Symbol	Parameter	Conditions			TYP
		-	Voltage scaling	Code	25°C
I_{DD} (Run)	Supply current in Run mode	$f_{HCLK}=f_{HSE}$ up to 48 MHZ included, bypass mode PLL ON above 48 MHz all peripherals disabled	Range2, LP f_{HCLK}=26MHz	Reduced code	1.90
				Coremark	2.08
				Dhrystone2.1	1.90
				Fibonacci	1.98
				While	2.14
			Range 1,HP fHCLK=80 MHz	Reduced code	7.0
				Coremark	7.0
				Dhrystone2.1	7.0
				Fibonacci	7.3
				While	8.05
			Range 0, HP f_{HCLK}= 110 MHz	Reduced code	11.0
				Coremark	11.1
				Dhrystone2.1	11.2
				Fibonacci	11.8
				While	13.1

Table 59. Current consumption in Sleep and Low-power sleep mode, Flas

Symbol	Parameter	Conditions			TYP						
		-	Voltage scaling	f_{HCLK}	25°C	55°C	85°C	105°C	125°C	25°C	55
I_{DD} (Sleep)	Supply current in Sleep mode	$f_{HCLK} = f_{HSE}$ up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disabled	Range 2	26 MHz	1.04	1.37	2.36	3.88	6.62	2.25	4.
				16 MHz	0.72	1.04	2.04	3.55	6.30	1.93	4.
				8 MHz	0.46	0.79	1.78	3.29	6.01	1.67	4.
				4 MHz	0.33	0.65	1.65	3.14	5.85	1.54	3.
				2 MHz	0.27	0.58	1.58	3.07	5.78	1.48	3.
				1 MHz	0.24	0.55	1.55	3.03	5.73	1.46	3.
				100 KHz	0.211	0.52	1.52	3.01	5.72	1.42	3.
			Range 0	110 MHz	4.73	5.23	6.62	8.65	12.21	7.00	11
			Range 1	80 MHz	3.31	3.74	5.01	6.88	10.19	5.20	8.
				72 MHz	3.01	3.44	4.71	6.56	9.86	4.90	8.
				64 MHz	2.71	3.14	4.41	6.26	9.56	4.60	8.
				48 MHz	2.10	2.53	3.79	5.62	8.92	3.98	7.
				32 MHz	1.49	1.91	3.17	4.98	8.27	3.37	6.
				24 MHz	1.18	1.60	2.84	4.67	7.93	3.06	6.
				16 MHz	0.88	1.29	2.53	4.34	7.60	2.75	6.
I_{DD}(LPSleep)	Supply current in Low-power sleep mode	$f_{HCLK} = f_{MSI}$ all peripherals disabled		2 MHz	205.22	584.41	1712	3383	6283	1843	47
				1 MHz	192.80	547.20	1678	3343	6248	1815	46
				400 KHz	143.73	520.85	1655	3313	6222	1793	45
				100 KHz	137.82	519.15	1650	3308	6219	1786	45

Table 60. Current consumption in Low-power sleep mode, Flash in power-

Symbol	Parameter	Conditions			TYP						
		-	Voltage scaling	f_{HCLK}	25°C	55°C	85°C	105°C	125°C	25°C	55°C
I_{DD} (LPSleep)	Supply current in Low-power sleep mode	$f_{HCLK} = f_{MSI}$ all peripherals disabled		2 MHz	197.64	567.40	1699	3374	6136	1839	4641
				1 MHz	165.99	540.66	1672	3313	6109	1805	4599
				400 KHz	145.78	510.80	1640	3312	6084	1785	4578
				100 KHz	143.34	506.41	1629	3288	6062	1423	3848

Table 61. Current consumption in Sleep mode, Flash ON and power supplied by internal SMPS step down converter

Symbol	Parameter	Conditions			TYP						
		-	Voltage scaling	f_{HCLK}	25°C	55°C	85°C	105°C	125°C	25°C	
I_{DD} (Sleep)	Supply current in Sleep mode	$f_{HCLK} = f_{HSE}$ up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disabled	Range 2 SMPS LP mode	26 MHz	0.69	0.82	1.27	1.99	3.22	0.8	
				16 MHz	0.50	0.64	1.09	1.80	3.05	0.62	
				8 MHz	0.35	0.48	0.93	1.65	2.88	0.47	
				4 MHz	0.27	0.40	0.85	1.55	2.81	0.39	
				2 MHz	0.23	0.37	0.82	1.52	2.77	0.35	
				1 MHz	0.21	0.35	0.79	1.50	2.73	0.34	
				100 KHz	0.20	0.33	0.78	1.48	2.73	0.32	
			Range 0 SMPS HP mode	110 MHz	3.22	3.49	4.24	5.40	7.70	3.81	
			Range 1 SMPS HP mode	80 MHz	2.22	2.44	3.09	4.06	5.98	2.6	
				72 MHz	2.04	2.26	2.90	3.89	5.78	2.41	
				64 MHz	1.85	2.07	2.71	3.70	5.53	2.22	
				48 MHz	1.48	1.70	2.34	3.31	5.11	1.83	
				32 MHz	1.10	1.32	1.94	2.91	4.62	1.44	
				24 MHz	0.91	1.12	1.74	2.71	4.40	1.24	
				16 MHz	0.72	0.93	1.55	2.52	4.18	1.04	

Table 62. Current consumption in Run mode, code with data processing running in single bank, ICACHE ON in 2-way and power supplied by external SM

Symbol	Parameter	Conditions(1)				
		-	VDD12	f_{HCLK}	25°C	55°C
I_{DD}(Run)	Supply current in Run mode	f_{HCLK} = f_{HSE} up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disabled	VDD12=1.2V	110 MHz	6.69	6.93
			VDD12=1.1V	80 MHz	4.1	4.77
				72 MHz	3.7	4.33
				64 MHz	3.31	3.88
				48 MHz	2.51	2.98
				32 MHz	1.7	2.08
				26 KHz	1.76	1.91
				16 MHz	1.14	1.29
				8 MHz	0.62	0.76
				4 MHz	0.35	0.49
				2 MHz	0.22	0.36
				1 MHz	0.16	0.29
				100 KHz	0.1	0.23

1. All values are obtained by calculation based on measurements done with internal voltage regulator and using following parameters = 85%.

Table 63. Current consumption in Run mode, code with data processing running in single bank, ICACHE ON in 1-way and power supplied by external SM

Symbol	Parameter	Conditions(1)				
		-	VDD12	fHCLK	25°C	55°
IDD(Run)	Supply current in Run mode	fHCLK = fHSE up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disabled	VDD12=1.2V	110 MHz	6.47	6.7
			VDD12=1.1V	80 MHz	3.97	4.1
				72 MHz	3.58	3.7
				64 MHz	3.2	3.3
				48 MHz	2.43	2.5
				32 MHz	1.65	1.8
				26 KHz	1.337	1.48
				16 MHz	0.863	1.00
				8 MHz	0.479	0.61
				4 MHz	0.285	0.42
				2 MHz	0.185	0.32
				1 MHz	0.138	0.27
				100 KHz	0.095	0.22

1. All values are obtained by calculation based on measurements done with internal voltage regulator and using following parameters = 85%.

Table 64. Current consumption in Run mode, code with data processing running in single bank, ICACHE disabled and power supplied by external SMPS

Symbol	Parameter	Conditions(1)				
		-	VDD12	f_{HCLK}	25°C	55°C
I_{DD}(Run)	Supply current in Run mode	f_{HCLK} = f_{HSE} up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disabled	VDD12=1.2V	110 MHz	7.55	7.8
			VDD12=1.1V	80 MHz	5.07	5.26
				72 MHz	4.58	4.77
				64 MHz	4.24	4.42
				48 MHz	3.19	3.37
				32 MHz	2.2	2.37
				26 KHz	1.76	1.91
				16 MHz	1.143	1.28
				8 MHz	0.617	0.75
				4 MHz	0.354	0.49
				2 MHz	0.22	0.35
				1 MHz	0.155	0.29
				100 KHz	0.099	0.23

1. All values are obtained by calculation based on measurements done with internal voltage regulator and using following parameters = 85%.

Table 65. Current consumption in Run mode, code with data processing running in dual bank, ICACHE on in 2-way and power supplied by external SMP

Symbol	Parameter	Conditions(1)				
		-	VDD12	f_{HCLK}	25°C	55°
I_{DD}(Run)	Supply current in Run mode	f_{HCLK} = f_{HSE} up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disabled	VDD12=1.2V	110 MHz	6.69	6.9
			VDD12=1.1V	80 MHz	4.09	4.2
				72 MHz	3.7	3.8
				64 MHz	3.3	3.4
				48 MHz	2.5	2.6
				32 MHz	1.7	1.8
				26 KHz	1.147	1.26
				16 MHz	0.737	0.85
				8 MHz	0.406	0.52
				4 MHz	0.241	0.35
				2 MHz	0.158	0.27
				1 MHz	0.115	0.2
				100 KHz	0.079	0.19

1. All values are obtained by calculation based on measurements done with internal voltage regulator and using following parameters = 85%.

Table 66. Current consumption in Run mode, code with data processing running in dual bank, ICACHE on in 1-way and power supplied by external SMP

Symbol	Parameter	Conditions(1)				
		-	VDD12	f_{HCLK}	25°C	55°
I_{DD}(Run)	Supply current in Run mode	f_{HCLK} = f_{HSE} up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disabled	VDD12=1.2V	110 MHz	6.47	6.7
			VDD12=1.1V	80 MHz	3.97	4.1
				72 MHz	3.58	3.7
				64 MHz	3.2	3.3
				48 MHz	2.42	2.5
				32 MHz	1.65	1.8
				26 KHz	1.114	1.23
				16 MHz	0.719	0.83
				8 MHz	0.399	0.51
				4 MHz	0.237	0.35
				2 MHz	0.155	0.27
				1 MHz	0.115	0.2
				100 KHz	0.079	0.19

1. All values are obtained by calculation based on measurements done with internal voltage regulator and using following parameters = 85%.

Table 67. Current consumption in Run mode, code with data processing running in dual bank, ICACHE disabled and power supplied by external SMPS

Symbol	Parameter	Conditions(1)				
		-	VDD12	f_{HCLK}	25°C	55°
I_{DD}(Run)	Supply current in Run mode	f_{HCLK} = f_{HSE} up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disabled	VDD12=1.2V	110 MHz	6.9	7.1
			VDD12=1.1V	80 MHz	5.01	5.2
				72 MHz	4.53	4.7
				64 MHz	4.25	4.4
				48 MHz	3.21	3.3
				32 MHz	2.25	2.4
				26 KHz	1.499	1.62
				16 MHz	0.985	1.10
				8 MHz	0.532	0.64
				4 MHz	0.302	0.42
				2 MHz	0.187	0.30
				1 MHz	0.133	0.24
				100 KHz	0.079	0.19

1. All values are obtained by calculation based on measurements done with internal voltage regulator and using following parameters = 85%.

Table 68. Current consumption in Run mode, code with data processing running and power supplied by external SMPS

Symbol	Parameter	Conditions(1)				
		-	VDD12	f_{HCLK}	25°C	55°
I_{DD}(Run)	Supply current in Run mode	f_{HCLK} = f_{HSE} up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disabled	VDD12=1.2V	110 MHz	6.81	7.05
			VDD12=1.1V	80 MHz	4.18	4.3
				72 MHz	3.78	3.95
				64 MHz	3.37	3.54
				48 MHz	2.55	2.72
				32 MHz	1.74	1.89
				26 KHz	1.172	1.29
				16 MHz	0.751	0.87
				8 MHz	0.413	0.53
				4 MHz	0.244	0.35
				2 MHz	0.158	0.27
				1 MHz	0.119	0.23
				100 KHz	0.079	0.19

1. All values are obtained by calculation based on measurements done with internal voltage regulator and using following parameters = 85%.

Table 69. Current consumption in Run mode, code with data processing running f and power supplied by external SMPS

Symbol	Parameter	Conditions(1)				
		-	VDD12	f_{HCLK}	25°C	55°C
I_{DD}(Run)	Supply current in Run mode	f_{HCLK} = f_{HSE} up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disabled	VDD12=1.2V	110 MHz	6.7	6.95
			VDD12=1.1V	80 MHz	4.11	4.29
				72 MHz	3.71	3.89
				64 MHz	3.31	3.49
				48 MHz	2.51	2.68
				32 MHz	1.71	1.87
				26 KHz	1.15	1.27
				16 MHz	0.741	0.85
				8 MHz	0.41	0.52
				4 MHz	0.241	0.35
				2 MHz	0.158	0.27
				1 MHz	0.115	0.23
				100 KHz	0.079	0.19

1. All values are obtained by calculation based on measurements done with internal voltage regulator and using following parameters = 85%.

Table 70. Current consumption in Sleep mode, Flash ON and power supplied by ex

Symbol	Parameter	Conditions(1)				
		-	VDD12	f_{HCLK}	25°C	55°
I_{DD}(Sleep)	Supply current in Sleep mode	f_{HCLK} = f_{HSE} up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disabled	VDD12=1.20V	110 MHz	1.90	2.1
			VDD12=1.10V	80 MHz	1.19	1.3
				72 MHz	1.08	1.2
				64 MHz	0.98	1.1
				48 MHz	0.76	0.9
				32 MHz	0.54	0.6
				26 MHz	0.453	0.59
				16 MHz	0.315	0.45
				8 MHZ	0.203	0.34
				4 MHz	0.147	0.28
				2MHz	0.116	0.25
				1 MHz	0.104	0.24
				100 Khz	0.091	0.22

1. All values are obtained by calculation based on measurements done with internal voltage regulator and using following parameters = 85%.

Table 71. Current consumption in Run mode, code with data processing running ICACHE on (2-way) and power supplied by external SMPS

Symbol	Parameter	Conditions(1)				TYP single bank mode	TYP single bank mode
		-	VDD12	fHCLK	code	25°C	25°C
IDD(Run)	Supply current in Run mode	fHCLK = fHSE up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disabled	VDD12=1.00V	fHCLK=26MHz	Reduced code	1.2	1.2
					Coremark	1.29	1.29
					Dhrystone2.1	1.37	1.37
					Fibonacci	1.15	1.14
					While(1)	1.04	1.04
			VDD12=1.10V	fHCLK=26MHz	Reduced code	1.45	1.45
					Coremark	1.56	1.56
					Dhrystone2.1	1.66	1.65
					Fibonacci	1.39	1.38
					While(1)	1.26	1.26
				fHCLK=80MHz	Reduced code	4.1	4.09
					Coremark	4.4	4.4
					Dhrystone2.1	4.7	4.68
					Fibonacci	3.88	3.88
					While(1)	3.55	3.55
			VDD12=1.20V	fHCLK=110MHz	Reduced code	6.69	6.69
					Coremark	7.2	7.2
					Dhrystone2.1	7.66	7.62
					Fibonacci	6.32	6.32
					While(1)	5.8	5.8

1. All values are obtained by calculation based on measurements done with internal voltage regulator and using following parameters: 85%.

Table 72. Current consumption in Run mode, code with data processing running ICACHE on (1-way) and power supplied by external SMPS

Symbol	Parameter	Conditions(1)				TYP Single Bank mode	TYP Single Bank mode
		-	VDD12	fHCLK	code	25°C	25°C
IDD(Run)	Supply current in Run mode	fHCLK = fHSE up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disabled	VDD12=1.00V	fHCLK=26MHz	Reduced code	1.16	1.16
					Coremark	1.22	1.22
					Dhrystone2.1	1.31	1.3
					Fibonacci	1.11	1.11
					While(1)	1.02	1.02
			VDD12=1.10V	fHCLK=26MHz	Reduced code	1.41	1.41
					Coremark	1.48	1.48
					Dhrystone2.1	1.58	1.58
					Fibonacci	1.34	1.34
					While(1)	1.24	1.24
				fHCLK=80MHz	Reduced code	3.97	3.97
					Coremark	4.16	4.16
					Dhrystone2.1	4.47	4.45
					Fibonacci	3.73	3.73
					While(1)	3.49	3.49
			VDD12=1.20V	fHCLK=110MHz	Reduced code	6.47	6.47
					Coremark	6.81	6.81
					Dhrystone2.1	7.28	7.25
					Fibonacci	6.09	6.09
					While(1)	5.71	5.7

1. All values are obtained by calculation based on measurements done with internal voltage regulator and using following parameters: 85%.

Table 73. Current consumption in Run mode, code with data processing running ICACHE disabled and power supplied by external SMPS

Symbol	Parameter	Conditions[1]				TYP Single Bank mode	TYP Single Bank mode
		-	VDD12	fHCLK	code	25°C	25°C
IDD(Run)	Supply current in Run mode	fHCLK = fHSE up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disabled	VDD12=1.00V	fHCLK=26MHz	Reduced code	1.53	1.56
					Coremark	1.66	1.58
					Dhrystone2.1	1.71	1.65
					Fibonacci	1.36	1.33
					While(1)	1.14	1.18
			VDD12=1.10V	fHCLK=26MHz	Reduced code	1.85	1.89
					Coremark	2.01	1.92
					Dhrystone2.1	2.07	2
					Fibonacci	1.64	1.61
					While(1)	1.38	1.43
				fHCLK=80MHz	Reduced code	5.07	5.01
					Coremark	4.91	4.37
					Dhrystone2.1	4.49	4.49
					Fibonacci	4.34	4.07
					While(1)	3.9	4.04
			VDD12=1.20V	fHCLK=110MHz	Reduced code	7.55	6.9
					Coremark	7.03	6.09
					Dhrystone2.1	7.08	6.2
					Fibonacci	6.64	6.07
					While(1)	6.39	6.63

1. All values are obtained by calculation based on measurements done with internal voltage regulator and using following parameters: 85%.

Table 74. Current consumption in Run mode, code with data processing running f and power supplied by external SMPS

Symbol	Parameter	Conditions(1)				
		-	VDD12	fHCLK	code	
IDD(Run)	Supply current in Run mode	fHCLK = fHSE up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disabled	VDD12=1.00V	fHCLK=26MHz	Reduced code	
					Coremark	
					Dhrystone2.1	
					Fibonacci	
					While(1)	
			VDD12=1.10V	fHCLK=26MHz	Reduced code	
					Coremark	
					Dhrystone2.1	
					Fibonacci	
					While(1)	
				fHCLK=80MHz	Reduced code	
					Coremark	
					Dhrystone2.1	
					Fibonacci	
					While(1)	
			VDD12=1.20V	fHCLK=110MHz	Reduced code	
					Coremark	
					Dhrystone2.1	
					Fibonacci	
					While(1)	

1. All values are obtained by calculation based on measurements done with internal voltage regulator and using following parameters: 85%.

Table 75. Current consumption in Run mode, code with data processing running f and power supplied by external SMPS

Symbol	Parameter	Conditions (1)			
		-	VDD12	f_{HCLK}	code
IDD(Run)	Supply current in Run mode	fHCLK = fHSE up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disabled	VDD12=1.00V	fHCLK=26MHz	Reduced code
					Coremark
					Dhrystone2.1
					Fibonacci
					While(1)
			VDD12=1.10V	fHCLK=26MHz	Reduced code
					Coremark
					Dhrystone2.1
					Fibonacci
					While(1)
				fHCLK=80MHz	Reduced code
					Coremark
					Dhrystone2.1
					Fibonacci
					While(1)
			VDD12=1.20V	fHCLK=110MHz	Reduced code
					Coremark
					Dhrystone2.1
					Fibonacci
					While(1)

1. All values are obtained by calculation based on measurements done with internal voltage regulator and using following parameters: 85%.

Table 76. Current consumption in Stop 2 mode

Symbol	Parameter	Conditions		TYP						
		-	V_{DD}	25°C	55°C	85°C	105°C	125°C	25°C	55°C
I_{DD} (Stop 2)	Supply current in Stop 2 mode, RTC disabled	-	1.8 V	3.07	16.61	68.35	158.43	332.53	19.03	67.1
			2.4 V	3.09	16.86	69.13	160.32	335.88	19.08	67.4
			3 V	3.13	17.24	69.5	161.75	341.1	19.18	67.7
			3.6 V	3.2	17.42	71.15	164.99	349.3	19.39	68.6
I_{DD} (Stop 2 with RTC)	Supply current in Stop 2 mode, RTC enabled	RTC clocked by LSI	1.8 V	3.66	17.32	68.52	159.57	333.56	19.7	67.8
			2.4 V	3.88	17.74	69.73	160.86	338.16	20.07	68.3
			3 V	4.2	17.94	70.57	163.39	342.82	20.37	68.6
			3.6 V	4.42	18.71	72.31	166.43	348.19	20.79	69.7
		RTC clocked by LSI with LPCAL = 1, ULPEN = 1	1.8 V	3.5	17.14	69.36	159.76	332.52	-	-
			2.4 V	3.62	17.68	70.03	161.58	336.53	-	-
			3 V	3.82	18.2	71	163.7	343.17	-	-
			3.6 V	4.06	18.8	72.72	168.58	351.22	-	-
		RTC clocked by LSE bypassed at 32768 Hz with LPCAL = 0, ULPEN = 0	1.8 V	3.44	17.15	68.39	159.57	333.37	-	-
			2.4 V	3.58	17.35	69.8	161.86	336.47	-	-
			3 V	3.79	17.77	70.33	163.41	342.2	-	-
			3.6 V	4.59	18.34	72.03	166.18	350.97	-	-
		RTC clocked by LSE bypassed at 32768 Hz with LPCAL = 1, ULPEN = 1	1.8 V	3.18	16.98	69.4	160.31	335.07	-	-
			2.4 V	3.27	17.29	69.65	161.79	339.1	-	-
			3 V	3.41	17.91	71.21	163.77	343.27	-	-
			3.6 V	4.16	18.5	72.62	167.08	350.59	-	-

Table 76. Current consumption in Stop 2 mode (continued)

Symbol	Parameter	Conditions		TYP						
		-	V_{DD}	25°C	55°C	85°C	105°C	125°C	25°C	55°C
I_{DD} (Stop 2 with RTC) (continued)	Supply current in Stop 2 mode, RTC enabled (continued)	RTC clocked by LSE quartz in low drive mode	1.8 V	3.48	16.53	66.1	151.2	295.85	-	-
			2.4 V	3.58	16.86	66.79	153.07	299.45	-	-
			3 V	3.71	17.18	67.57	155.09	302.75	-	-
			3.6 V	3.91	17.74	68.97	158.26	309.93	-	-
		RTC clocked by LSE quartz in low drive mode with LPCAL = 1, ULPEN = 1	1.8 V	3.16	16.68	66.32	151.87	296.04	-	-
			2.4 V	3.21	16.99	66.91	153.42	299.34	-	-
			3 V	3.27	17.39	68.27	155.45	304.73	-	-
			3.6 V	3.42	17.93	69.41	158.77	310.4	-	-
I_{DD} (wakeup from Stop 2)	Supply current during wakeup from Stop 2 mode	Wakeup clock is MSI = 48 MHz, voltage Range 1	3 V	1.96	-	-	-	-	-	-
		Wakeup clock is MSI = 4 MHz, voltage Range 2	3 V	1.09	-	-	-	-	-	-
		Wakeup clock is HSI = 16 MHz, voltage Range 1	3 V	1.72	-	-	-	-	-	-

Table 77. Current consumption in Stop 1 mode

Symbol	Parameter	Conditions		TYP						
		-	V_{DD}	25°C	55°C	85°C	105°C	125°C	25°C	55°C
I_{DD} (Stop 1)	Supply current in Stop 1 mode, RTC disabled	-	1.8 V	91.47	372.36	1243	2527	4611	1196	3403
			2.4 V	91.94	375.16	1251	2531	4652	1199	3418
			3 V	92.51	375.46	1249	2549	4675	1204	3427
			3.6 V	93.26	380.59	1270	2567	4721	1215	3433
I_{DD} (Stop 1 with RTC)	Supply current in Stop 1 mode, RTC enabled	RTC clocked by LSI	1.8 V	92.46	373.25	1248	2518	4617	1196	3405
			2.4 V	92.48	372.19	1250	2528	4643	1201	3433
			3 V	93.34	374.54	1253	2541	4683	1206	3424
			3.6 V	93.38	378.64	1267	2559	4712	1213	3434
		RTC clocked by LSE bypassed at 32768 Hz	1.8 V	92.35	371.81	1248	2518	4605	-	-
			2.4 V	92.31	374.21	1245	2521	4640	-	-
			3 V	93.59	375.92	1256	2534	4673	-	-
			3.6 V	93.19	377.07	1262	2551	4713	-	-
		RTC clocked by LSE quartz in low drive mode	1.8 V	100.67	381.08	1214	2442	-	-	-
			2.4 V	101.20	380.64	1224	2447	-	-	-
			3 V	102.04	378.49	1228	2466	-	-	-
			3.6 V	103.34	387.73	1239	2480	-	-	-

Table 77. Current consumption in Stop 1 mode (continued)

Symbol	Parameter	Conditions		TYP						
		-	V_{DD}	25°C	55°C	85°C	105°C	125°C	25°C	55°C
I_{DD} (wakeup from Stop 1)	Supply current during wakeup from Stop 1 mode	Wakeup clock is MSI = 48 MHz, voltage Range 1	3 V	2.02	-	-	-	-	-	-
		Wakeup clock is MSI = 4 MHz, voltage Range 2	3 V	0.58	-	-	-	-	-	-
		Wakeup clock is HSI = 16 MHz, voltage Range 1	3 V	1.27	-	-	-	-	-	-

Table 78. Current consumption in Stop 0 mode

Symbol	Parameter	Conditions		TYP							
		-	V_{DD}	25°C	55°C	85°C	105°C	125°C	25°C	55°C	
I_{DD} (Stop 0)	Supply current in Stop 0 mode, RTC disabled	-	1.8 V	192.69	494.92	1425	2797	5106	1395	3797	
		-	2.4 V	194.69	495.31	1430	2804	5108	1396	3798	
		-	3 V	196.09	495.47	1431	2812	5124	1397	3799	
		-	3.6 V	197.54	497.36	1434	2814	5155	1399	3802	

Table 79. Current consumption in Standby mode

Symbol	Parameter	Conditions		TYP						
		-	V_{DD}	25°C	55°C	85°C	105°C	125°C	25°C	55°C
I_{DD} (Standby)	Supply current in Standby mode (backup registers retained), RTC disabled	No independent watchdog	1.8 V	108	382	2374	7132	19259	237	2269
			2.4 V	119	476	2795	8332	22151	361	2497
			3 V	134	591	3215	9665	26746	411	2716
			3.6 V	183	827	4232	12128	31763	558	3214
		With independent watchdog	1.8 V	347	-	-	-	-	572	2578
			2.4 V	405	-	-	-	-	708	2832
			3 V	483	-	-	-	-	609	2913
			3.6 V	596	-	-	-	-	999	3466

Table 79. Current consumption in Standby mode (continued)

Symbol	Parameter	Conditions		TYP						
		-	V_{DD}	25°C	55°C	85°C	105°C	125°C	25°C	55°C
I_{DD} (Standby with RTC)	Supply current in Standby mode (backup registers retained), RTC enabled	RTC clocked by LSI, no independent watchdog	1.8 V	717	971	2924	7693	19714	930	2760
			2.4 V	887	1266	3589	9054	22856	1224	3096
			3 V	1113	1584	4206	10666	27521	1303	3509
			3.6 V	1394	2059	5515	13394	32693	1828	3889
		RTC clocked by LSI, no independent watchdog with LPCAL = 1, ULPEN = 1	1.8 V	457	779	3075	8179	20106	-	-
			2.4 V	582	1080	4082	9786	23298	-	-
			3 V	740	1425	5195	11380	28044	-	-
			3.6 V	955	1905	6884	14210	33407	-	-
		RTC clocked by LSI, with independent watchdog	1.8 V	766	-	-	-	-	847	2549
			2.4 V	948	-	-	-	-	1267	3171
			3 V	1196	-	-	-	-	1561	3610
			3.6 V	1492	-	-	-	-	1896	4136
		RTC clocked by LSE bypassed at 32768 Hz	1.8 V	435	711	2650	7592	19645	-	-
			2.4 V	569	954	3254	8972	22787	-	-
			3 V	768	1247	3963	10303	27154	-	-
			3.6 V	1024	1686	5174	13141	32293	-	-
		RTC clocked by LSE bypassed at 32768 Hz with LPCAL = 1, ULPEN = 1	1.8 V	166	-	-	-	-	-	-
			2.4 V	236	-	-	-	-	-	-
			3 V	356	-	-	-	-	-	-
			3.6 V	575	-	-	-	-	-	-

Table 79. Current consumption in Standby mode (continued)

Symbol	Parameter	Conditions		TYP						
		-	V_{DD}	25°C	55°C	85°C	105°C	125°C	25°C	55°C
I_{DD} (Standby with RTC) (continued)	Supply current in Standby mode (backup registers retained), RTC enabled (continued)	RTC clocked by LSE quartz in low drive mode	1.8 V	491	-	-	-	-	-	-
			2.4 V	574	-	-	-	-	-	-
			3 V	696	-	-	-	-	-	-
			3.6 V	870	-	-	-	-	-	-
		RTC clocked by LSE quartz in low drive mode with LPCAL = 1, ULPEN = 1	1.8 V	222	-	-	-	-	-	-
			2.4 V	250	-	-	-	-	-	-
			3 V	297	-	-	-	-	-	-
			3.6 V	403	-	-	-	-	-	-
I_{DD} (SRAM2)	Supply current to be added in Standby mode when Full SRAM2 (64KB) is retained	-	1.8 V	668	3089	13834	34240	75362	1834	8192
			2.4 V	704	3193	14412	35468	78515	1859	8376
			3 V	739	3283	14722	36843	82664	1907	8514
			3.6 V	840	3571	15867	38708	88150	1973	8919
I_{DD} (SRAM)	Supply current to be added in Standby mode when partial SRAM2 (4 KB) is retained	-	1.8 V	164	658	3378	9485	23856	518	2685
			2.4 V	201	764	3853	10707	26844	585	2758
			3 V	231	871	4319	12043	31160	606	3243
			3.6 V	326	1128	5250	14470	36553	723	3570
I_{DD} (wakeup from Standby)	Supply current during wakeup from Standby mode	Wakeup clock is MSI = 4 MHz	3 V	1.11	-	-	-	-	-	-

Table 80. Current consumption in Shutdown mode

Symbol	Parameter	Conditions		TYP						
		-	V_{DD}	25°C	55°C	85°C	105°C	125°C	25°C	55°C
I_{DD} (Shutdown)	Supply current in Shutdown mode (backup registers retained) RTC disabled	-	1.8 V	17.0	198	1533	5195	15336	99	590
			2.4 V	18.0	269	1803	6166	17522	115	679
			3 V	44.0	361	2314	7212	21381	141	800
			3.6 V	127.0	587	3159	9534	26115	196	990
I_{DD} (Shutdown with RTC)	Supply current in Shutdown mode (backup registers retained) RTC enabled	RTC clocked by LSE bypassed at 32768 Hz with LPCAL = 0	1.8 V	307	525	1905	5592	15801	-	-
			2.4 V	485	746	2363	6676	18041	-	-
			3 V	689	1015	2905	7919	22214	-	-
			3.6 V	974	1435	4082	10392	26856	-	-
		RTC clocked by LSE bypassed at 32768 Hz with LPCAL = 1	1.8 V	116	325	1711	5423	15551	-	-
			2.4 V	221	491	2100	6395	17909	-	-
			3 V	339	656	2636	7450	21753	-	-
			3.6 V	535	996	3645	9998	26420	-	-
		RTC clocked by LSE quartz in low drive mode with LPCAL = 0	1.8 V	405	-	-	-	-	-	-
			2.4 V	486	-	-	-	-	-	-
			3 V	604	-	-	-	-	-	-
			3.6 V	768	-	-	-	-	-	-
		RTC clocked by LSE quartz in low drive mode with LPCAL = 1	1.8 V	207	-	-	-	-	-	-
			2.4 V	232	-	-	-	-	-	-
			3 V	272	-	-	-	-	-	-
			3.6 V	345	-	-	-	-	-	-

Table 80. Current consumption in Shutdown mode (continued)

Symbol	Parameter	Conditions		TYP						
		-	V_{DD}	25°C	55°C	85°C	105°C	125°C	25°C	55°C
I_{DD} (wakeup from Shutdown)	Supply current during wakeup from Shutdown mode	Wakeup clock is MSI = 4 MHz	3 V	0.53	-	-	-	-	-	-

Table 81. Current consumption in VBAT mode

Symbol	Parameter	Conditions		TYP						
		-	V_{BAT}	25°C	55°C	85°C	105°C	125°C	25°C	
I_{DD} (VBAT)	Backup domain supply current	RTC disabled	1.8 V	3.4	45	307	966	2699	-	
			2.4 V	3.9	55	358	1097	2995	-	
			3 V	5.9	73	447	1350	3699	-	
			3.6 V	13.4	136	786	2303	6528	-	
		RTC enabled and clocked by LSE bypassed at 32768 Hz with LPCAL = 0	1.8 V	330	369	654	1303	-	-	
			2.4 V	446	528	843	1595	-	-	
			3 V	632	727	1119	2045	-	-	
			3.6 V	867	996	1680	3247	-	-	
		RTC enabled and clocked by LSE bypassed at 32768 Hz with LPCAL=1	1.8 V	130	381	692	1369	-	-	
			2.4 V	183	406	738	1499	-	-	
			3 V	288	441	841	1761	-	-	
			3.6 V	392	518	1163	2707	-	-	
		RTC enabled and clocked by LSE quartz with LPCAL = 0	1.8 V	387	-	-	-	-	-	
			2.4 V	461	-	-	-	-	-	
			3 V	568	-	-	-	-	-	
			3.6 V	700	-	-	-	-	-	
		RTC enabled and clocked by LSE quartz with LPCAL = 1	1.8 V	187	-	-	-	-	-	
			2.4 V	202	-	-	-	-	-	
			3 V	229	-	-	-	-	-	
			3.6 V	275	-	-	-	-	-	

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 102: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption measured previously (see), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the I/O supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DDIOx} \times f_{SW} \times C$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DDIOx} is the I/O supply voltage

f_{SW} is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT} + C_S$

C_S is the PCB board capacitance including the pad pin.

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in *Table 82*. The MCU is placed under the following conditions:

- All I/O pins are in Analog mode
- The given value is calculated by measuring the difference of the current consumptions:
  - when the peripheral is clocked on
  - when the peripheral is clocked off
- Ambient operating temperature and supply voltage conditions summarized in *Table 24: Voltage characteristics*
- The power consumption of the digital part of the on-chip peripherals is given in *Table 82*. The power consumption of the analog part of the peripherals (where applicable) is indicated in each related section of the datasheet.

Table 82. Peripheral current consumption

Peripheral		Range 0	Range 1	Range 2	Low-power run and sleep	Unit
AHB	Bus matrix	5.85	5.47	4.09	5.36	µA/MHz
	DMA1	3.67	3.38	2.54	3.16	
	DMA2	3.71	3.43	2.56	3.20	
	DMAMUX1	7.11	6.64	4.96	6.16	
	FLASH	5.32	4.95	3.69	4.59	
	SRAM1	2.03	1.90	1.43	1.75	
	CRC	1.05	0.99	0.76	0.95	
	TSC	1.77	1.67	1.24	1.49	
	GTZC	0.38	0.36	0.27	0.35	
	ICACHE	0.38	0.38	0.27	1.00	
	GPIOA	0.40	0.41	0.30	0.32	
	GPIOB	0.25	0.23	0.17	0.22	
	GPIOC	0.31	0.27	0.21	0.37	
	GPIOD	0.30	0.26	0.21	0.26	
	GPIOE	0.19	0.17	0.16	0.21	
	GPIOF	0.21	0.18	0.14	0.19	
	GPIOG	0.32	0.26	0.22	0.31	
	GPIOH	0.29	0.27	0.21	0.25	
	SRAM2	3.32	3.08	2.34	2.90	
	ADC AHB clock domain	5.92	5.49	4.16	5.11	
	ADC independent clock domain	0.15	0.14	0.08	0.14	

Table 82. Peripheral current consumption (continued)

Peripheral		Range 0	Range 1	Range 2	Low-power run and sleep	Unit
AHB (Cont)	HASH	3.91	3.64	2.74	3.44	µA/MHz
	RNG AHB clock domain	2.44	2.27	NA	NA	
	RNG independent clock domain	4.55	6.12	NA	NA	
	SDMMC1 AHB clock domain	20.52	19.07	NA	NA	µA/MHz
	SDMMC1 independent clock domain	4.92	6.63	NA	NA	
	FMC	11.17	10.39	7.82	9.90	
	OSPI1 AHB clock domain	10.77	10.00	7.61	9.57	
	OPSPI1 independent clock domain	0.12	0.11	0.04	1.00	
	ALL AHB peripherals	47.58	47.47	55.06	350.76	
APB1	AHB to APB1 bridge	0.41	0.43	0.36	0.61	µA/MHz
	TIM2	6.65	6.19	4.67	5.81	
	TIM3	5.46	5.08	3.82	4.75	
	TIM4	5.38	5.02	3.78	4.73	
	TIM5	6.92	6.47	4.86	6.08	
	TIM6	1.12	1.04	0.79	0.98	
	TIM7	1.24	1.16	0.86	0.98	
	RTCAPB	3.50	3.32	2.50	3.08	
	WWDG	0.58	0.52	0.40	0.48	
	SPI2	2.52	2.34	1.78	2.25	
	SPI3	2.39	2.22	1.69	2.16	
	USART2 APB clock domain	3.40	3.14	2.39	3.03	
	USART2 independent clock domain	6.41	5.99	4.50	5.53	
	USART3 APB clock domain	2.96	2.73	2.12	2.57	
	USART3 independent clock domain	6.96	6.49	4.86	6.09	
	UART4 APB clock domain	2.81	2.60	1.99	2.48	
	UART4 independent clock domain	5.59	5.26	3.95	4.85	
	UART5 APB clock domain	2.75	2.58	1.99	2.45	

Table 82. Peripheral current consumption (continued)

Peripheral		Range 0	Range 1	Range 2	Low-power run and sleep	Unit
APB1 (Cont)	UART5 independent clock domain	5.59	5.19	3.90	4.79	µA/MHz
	I2C1 APB clock domain	1.42	1.34	1.00	1.22	
	I2C1 independent clock domain	3.47	3.22	2.46	3.12	
	I2C2 APB clock domain	1.32	1.24	0.93	1.10	
	I2C2 independent clock domain	3.33	3.11	2.37	3.06	
	I2C3 APB clock domain	1.14	1.05	0.81	0.90	
	I2C3 independent clock domain	2.75	2.58	1.97	2.61	
	CRS	0.35	0.30	0.22	0.50	
	PWR	1.54	1.44	1.03	1.22	
	DAC1	2.89	2.69	2.03	2.43	
	OPAMP	0.34	0.36	0.23	1.00	
	LPTIM1 APB clock domain	1.10	1.01	0.78	0.87	
	LPTIM1 independent clock domain	3.37	3.18	2.39	3.07	
	LPUART1 APB clock domain	1.66	1.54	1.19	1.61	
	LPUART1 independent clock domain	3.43	3.24	2.44	2.99	
	I2C4 APB clock domain	1.40	1.28	0.97	1.24	
	I2C4 independent clock domain	3.31	3.11	2.34	2.90	
	LPTIM2 APB clock domain	1.36	1.26	0.96	1.15	
	LPTIM2 independent clock domain	3.80	3.58	2.66	3.35	
	LPTIM3 APB clock domain	1.02	0.93	0.74	0.94	
	LPTIM3 independent clock domain	3.16	2.98	2.21	2.80	
	FDCAN APB clock domain	7.99	7.41	5.56	6.70	
	FDCAN independent clock domain	0.16	0.22	3.20	4.05	
	USBFS APB clock domain	3.51	3.25	NA	NA	
	USBFS independent clock domain	4.53	6.08	NA	NA	
	UCPD1	2.67	2.46	1.84	NA(1)	
APB2	AHB to APB2 bridge	6.64	6.16	4.68	8.43	µA/MHz
	SYSCFG	0.75	0.71	0.54	0.67	
	TIM1	9.40	8.74	6.57	8.33	
	SPI1	2.69	2.51	1.90	2.43	
	TIM8	8.94	8.34	6.29	8.06	
	USART1 APB clock domain	3.16	2.92	2.23	3.09	

Table 82. Peripheral current consumption (continued)

Peripheral		Range 0	Range 1	Range 2	Low-power run and sleep	Unit
APB2 (Cont)	USART1 independent clock domain	7.01	6.54	4.91	6.01	µA/MHz
	TIM15	4.93	4.60	3.45	4.45	
	TIM16	3.27	3.05	2.29	2.83	
	TIM17	3.76	3.49	2.62	3.40	
	SAI1 APB clock domain	3.04	2.84	2.12	0.50	
	SAI1 independent clock domain	2.20	2.92	2.85	2.5	
	SAI2 APB clock domain	3.32	3.07	2.30	2.99	
	SAI2 independent clock domain	2.14	2.94	3	3	
	DFSDM1	8.18	7.61	5.73	7.42	
ALL	-	275.73	256.25	188.42	233	

1. The UCPD1 is always clocked by the HSI16.

5.3.7 Wakeup time from low-power modes and voltage scaling transition times

The wakeup times given in *Table 83* are the latency between the event and the execution of the first user instruction.

The device goes in low-power mode after the WFE (wait for event) instruction.

Table 83. Low-power mode wakeup timings(1)

-	Parameter	Conditions		Typ	Max	Unit
Sleep	Wakeup time from Sleep mode to Run mode	-		14	17	Number of CPU cycles
	Wakeup time from Low-power sleep mode to Low-power run mode	Sleep Power Down (SLEEP_PD=1 in FLASH_ACR) and with clock MSI = 2 MHz		14	17	
Stop 0	Flash	Range 1	MSI48	5.83	6.26	µs
			HSI16	5.23	5.46	
		Range 2	MSI24	18.48	18.96	
			HSI16	17.56	17.94	
			MSI4	23.36	24.59	
	SRAM1	Range 1	MSI48	1.79	2.16	
			HSI16	2.79	3.01	
		Range 2	MSI24	2.43	2.82	
			HSI16	2.80	3.03	
			MSI4	9.66	10.88	
Stop 1	Flash	Range 1	MSI48	9.74	10.22	
			HSI16	9.22	9.67	
		Range 2	MSI24	21.84	22.63	
			HSI16	20.98	21.81	
			MSI4	25.48	26.34	
	SRAM1	Range 1	MSI48	5.58	5.95	
			HSI16	6.68	7.06	
		Range 2	MSI24	5.69	6.24	
			HSI16	6.18	6.88	
			MSI4	11.04	11.99	
	Flash	Low Power Run (LPR=1)	MSI2	81.2	82.5	
	SRAM1			17.8	19	

Table 83. Low-power mode wakeup timings(1) (continued)

-	Parameter	Conditions		Typ	Max	Unit
Stop 2	Flash	Range 1	MSI48	11.20	11.64	µs
			HSI16	10.35	10.77	
		Range 2	MSI24	23.76	24.15	
			HSI16	22.24	22.62	
			MSI4	27.81	28.46	
	SRAM1	Range 1	MSI48	6.19	6.61	
			HSI16	7.33	7.75	
		Range 2	MSI24	6.31	6.64	
			HSI16	6.89	7.22	
			MSI4	11.69	12.36	
Standby	Flash	Range 2	MSI8	52.5	55.73	
			MSI4	52.58	55.78	
	Flash with SRAM2	Range 2	MSI8	52.5	55.74	
			MSI4	52.60	55.73	
Shutdown	Flash	Range 2	MSI4	276.48	292.42	

1. Guaranteed by characterization results.

Table 84. Regulator modes transition times(1)

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WULPRUN}$	Wakeup time from Low- power run mode to Run mode(2)	Code run with MSI 2 MHz	5	7	µs
t_{VOST}	Regulator transition time from Range 2 to Range 1 or Range 1 to Range 2(3)	Code run with MSI 24 MHz	20	40	

1. Guaranteed by characterization results.
2. Time until REGLPF flag is cleared in PWR_SR2.
3. Time until VOSF flag is cleared in PWR_SR2.

Table 85. Wakeup time using USART/LPUART(1)

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WUUSART}$ $t_{WULPUART}$	Wakeup time needed to calculate the maximum USART/LPUART baudrate allowing to wakeup up from stop mode when USART/LPUART clock source is HSI	Stop mode 0	-	1.7	µs
		Stop mode 1/2	-	8.5	

1. Guaranteed by design.

5.3.8 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO.

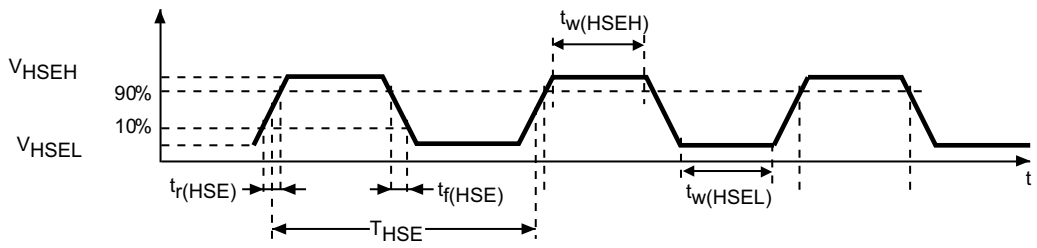
The external clock signal has to respect the I/O characteristics in *Section 5.3.15*. However, the recommended clock input waveform is shown in *Figure 33: High-speed external clock source AC timing diagram*.

Table 86. High-speed external user clock characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	Voltage scaling Range 0 and 1	-	8	48	MHz
		Voltage scaling Range 2	-	8	26	
V_{HSEH}	OSC_IN input pin high level voltage	-	0.7 V_{DDIOx}	-	V_{DDIOx}	V
V_{HSEL}	OSC_IN input pin low level voltage	-	V_{SS}	-	0.3 V_{DDIOx}	
$t_{w(HSEH)}$ $t_{w(HSEL)}$	OSC_IN high or low time	Voltage scaling Range 0 and 1	7	-	-	ns
		Voltage scaling Range 2	18	-	-	

1. Guaranteed by design.

Figure 33. High-speed external clock source AC timing diagram



Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO.

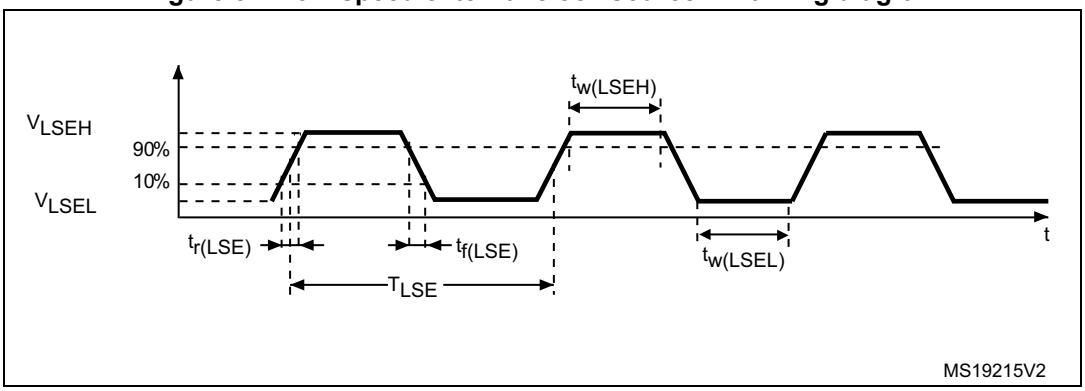
The external clock signal has to respect the I/O characteristics in *Section 5.3.15*. However, the recommended clock input waveform is shown in *Figure 34*.

Table 87. Low-speed external user clock characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	-	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage	-	0.7 V_{DDIOx}	-	V_{DDIOx}	V
V_{LSEL}	OSC32_IN input pin low level voltage	-	V_{SS}	-	0.3 V_{DDIOx}	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time	-	250	-	-	ns

1. Guaranteed by design.

Figure 34. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 48 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 88*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 88. HSE oscillator characteristics(1)

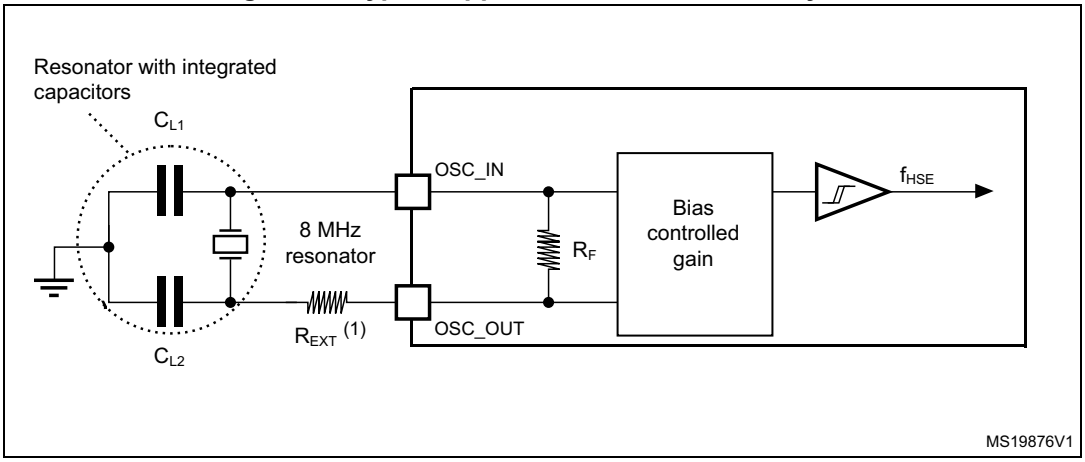
Symbol	Parameter	Conditions(2)	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	48	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
$I_{DD(HSE)}$	HSE current consumption	During startup(3)	-	-	5.5	mA
		V_{DD} = 3 V, Rm = 30 Ω, CL = 10 pF@8 MHz	-	0.44	-	
		V_{DD} = 3 V, Rm = 45 Ω, CL = 10 pF@8 MHz	-	0.45	-	
		V_{DD} = 3 V, Rm = 30 Ω, CL = 5 pF@48 MHz	-	0.68	-	
		V_{DD} = 3 V, Rm = 30 Ω, CL = 10 pF@48 MHz	-	0.94	-	
		V_{DD} = 3 V, Rm = 30 Ω, CL = 20 pF@48 MHz	-	1.77	-	
G_m	Maximum critical crystal transconductance	Startup	-	-	1.5	mA/V
$t_{SU(HSE)}$(4)	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Guaranteed by design.
2. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
3. This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 20 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 35*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 35. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 89*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

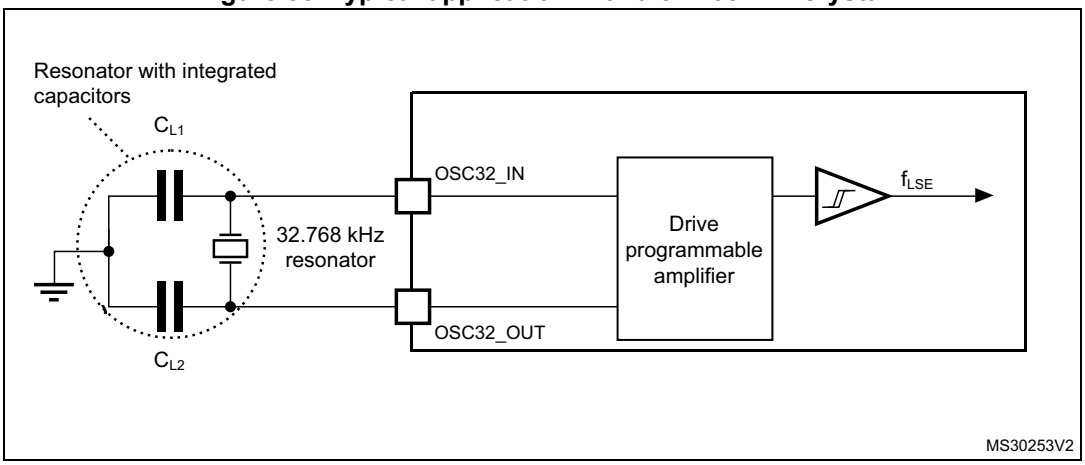
Table 89. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)(1)

Symbol	Parameter	Conditions(2)	Min	Typ	Max	Unit
$I_{DD(LSE)}$	LSE current consumption	LSEDRV[1:0] = 00 Low drive capability	-	250	-	nA
		LSEDRV[1:0] = 01 Medium low drive capability	-	315	-	
		LSEDRV[1:0] = 10 Medium high drive capability	-	500	-	
		LSEDRV[1:0] = 11 High drive capability	-	630	-	
$Gm_{critmax}$	Maximum critical crystal gm	LSEDRV[1:0] = 00 Low drive capability	-	-	0.5	µA/V
		LSEDRV[1:0] = 01 Medium low drive capability	-	-	0.75	
		LSEDRV[1:0] = 10 Medium high drive capability	-	-	1.7	
		LSEDRV[1:0] = 11 High drive capability	-	-	2.7	
$t_{SU(LSE)}$(3)	Startup time	V_{DD} is stabilized	-	2	-	s

1. Guaranteed by design.
2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Figure 36. Typical application with a 32.768 kHz crystal



Note: An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.

5.3.9 Internal clock source characteristics

The parameters given in *Table 90* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 27: General operating conditions*. The provided curves are characterization results, not tested in production.

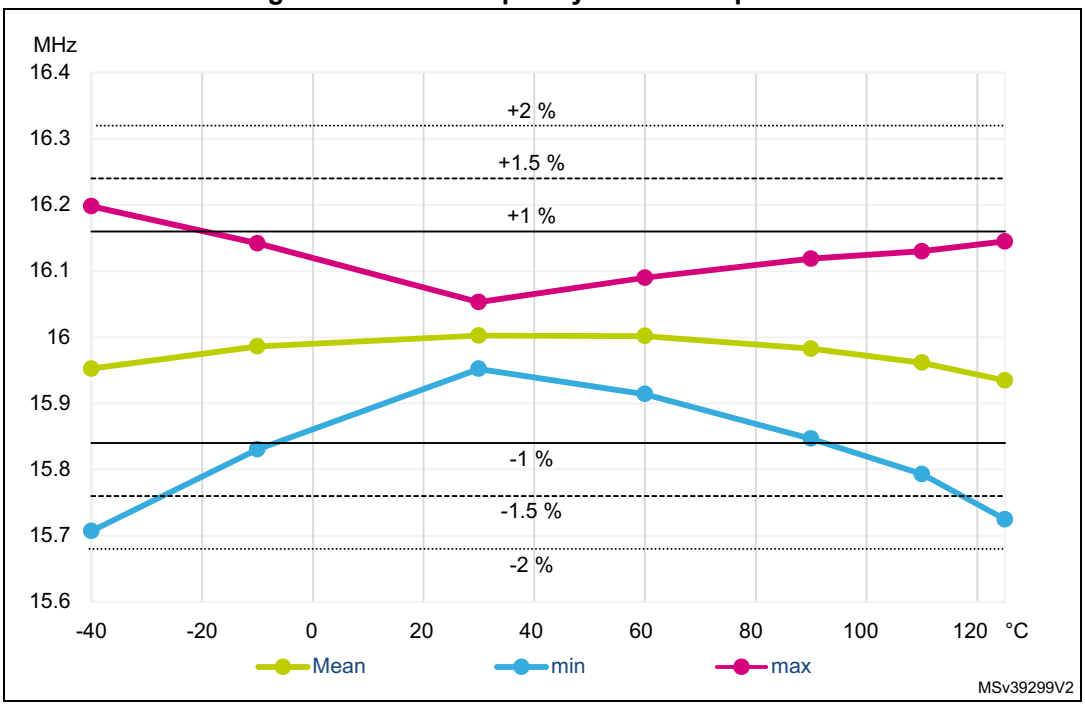
High-speed internal (HSI16) RC oscillator

Table 90. HSI16 oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI16}	HSI16 Frequency	V_{DD}=3.0 V, T_A=30 °C	15.88	-	16.08	MHz
TRIM	HSI16 user trimming step	Trimming code is not a multiple of 64	0.2	0.3	0.4	%
		Trimming code is a multiple of 64	-4	-6	-8	
DuCy(HSI16)(2)	Duty Cycle	-	45	-	55	%
Δ_{Temp}(HSI16)	HSI16 oscillator frequency drift over temperature	T_A= 0 to 85 °C	-1	-	1	%
		T_A= -40 to 125 °C	-2	-	1.5	%
Δ_{VDD}(HSI16)	HSI16 oscillator frequency drift over V_{DD}	V_{DD}=1.62 V to 3.6 V	-0.1	-	0.05	%
t_{su}(HSI16)(2)	HSI16 oscillator start-up time	-	-	0.8	1.2	µs
t_{stab}(HSI16)(2)	HSI16 oscillator stabilization time	-	-	3	5	µs
I_{DD}(HSI16)(2)	HSI16 oscillator power consumption	-	-	155	190	µA

1. Guaranteed by characterization results.
2. Guaranteed by design.

Figure 37. HSI16 frequency versus temperature



Multi-speed internal (MSI) RC oscillator

Table 91. MSI oscillator characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{MSI}	MSI frequency after factory calibration, done at V_{DD}=3 V and T_A=30 °C	MSI mode	Range 0	98.7	100	101.3	kHz
			Range 1	197.4	200	202.6	
			Range 2	394.8	400	405.2	
			Range 3	7896	800	810.4	
			Range 4	0.987	1	1.013	MHz
			Range 5	1.974	2	2.026	
			Range 6	3.948	4	4.052	
			Range 7	7.896	8	8.104	
			Range 8	15.79	16	16.21	
			Range 9	23.69	24	24.31	
			Range 10	31.58	32	32.42	
			Range 11	47.38	48	48.62	
		PLL mode XTAL= 32.768 kHz	Range 0	-	98.304	-	kHz
			Range 1	-	196.608	-	
			Range 2	-	393.216	-	
			Range 3	-	786.432	-	
			Range 4	-	1.016	-	MHz
			Range 5	-	1.999	-	
			Range 6	-	3.998	-	
			Range 7	-	7.995	-	
			Range 8	-	15.991	-	
			Range 9	-	23.986	-	
			Range 10	-	32.014	-	
			Range 11	-	48.005	-	
Δ_{TEMP}(MSI)(2)	MSI oscillator frequency drift over temperature	MSI mode	T_A= -0 to 85 °C	-3.5	-	3	%
			T_A= -40 to 125 °C	-8	-	6	

Table 91. MSI oscillator characteristics(1) (continued)

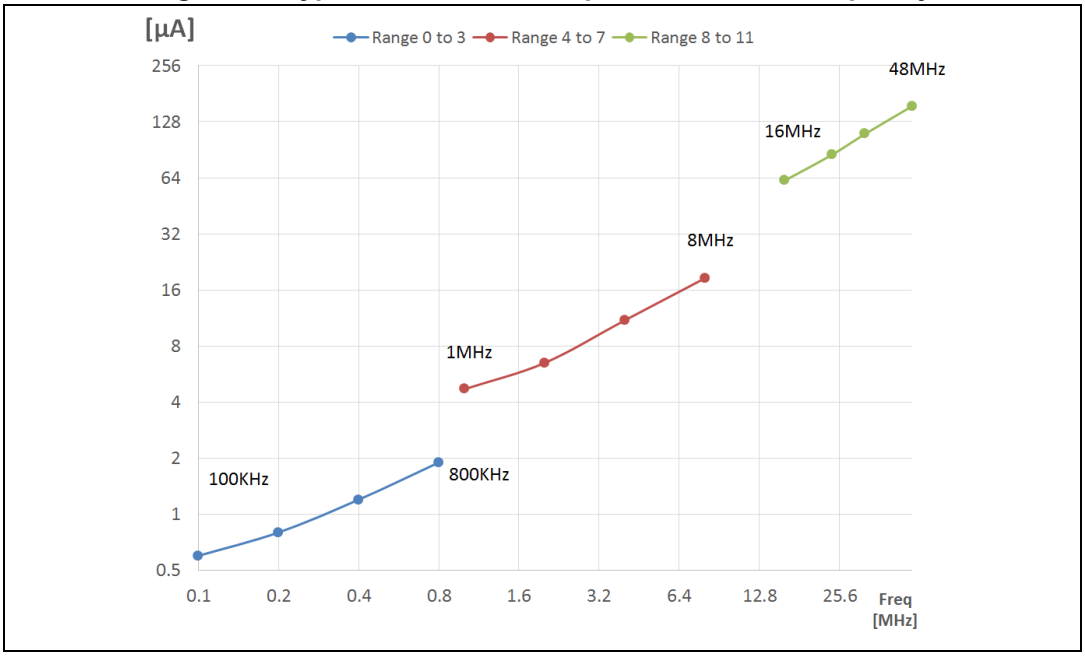
Symbol	Parameter	Conditions			Min	Typ	Max	Unit
$\Delta_{VDD}(MSI)^{(2)}$	MSI oscillator frequency drift over V_{DD} (reference is 3 V)	MSI mode	Range 0 to 3	V_{DD}=1.62 V to 3.6 V	-1.2	-	0.5	%
				V_{DD}=2.4 V to 3.6 V	-0.5	-		
			Range 4 to 7	V_{DD}=1.62 V to 3.6 V	-2.5	-	0.7	
				V_{DD}=2.4 V to 3.6 V	-0.8	-		
			Range 8 to 11	V_{DD}=1.62 V to 3.6 V	-5	-	1	
				V_{DD}=2.4 V to 3.6 V	-1.6	-		
$\Delta F_{SAMPLING}(MSI)^{(2)(4)}$	Frequency variation in sampling mode(3)	MSI mode	T_A= -40 to 85 °C		-	1	2	%
			T_A= -40 to 125 °C		-	2	4	
CC jitter(MSI)(4)	RMS cycle-to-cycle jitter	PLL mode Range 11		-	-	60	-	ps
P jitter(MSI)(4)	RMS Period jitter	PLL mode Range 11		-	-	50	-	ps
$t_{SU}(MSI)^{(4)}$	MSI oscillator start-up time	Range 0		-	-	10	20	us
		Range 1		-	-	5	10	
		Range 2		-	-	4	8	
		Range 3		-	-	3	7	
		Range 4 to 7		-	-	3	6	
		Range 8 to 11		-	-	2.5	6	
$t_{STAB}(MSI)^{(4)}$	MSI oscillator stabilization time	PLL mode Range 11	10 % of final frequency	-	-	0.25	0.5	ms
			5 % of final frequency	-	-	0.5	1.25	
			1 % of final frequency	-	-	-	2.5	

Table 91. MSI oscillator characteristics(1) (continued)

Symbol	Parameter	Conditions			Min	Typ	Max	Unit
I_{DD}(MSI)(4)	MSI oscillator power consumption	MSI and PLL mode	Range 0	-	-	0.6	1	µA
			Range 1	-	-	0.8	1.2	
			Range 2	-	-	1.2	1.7	
			Range 3	-	-	1.9	2.5	
			Range 4	-	-	4.7	6	
			Range 5	-	-	6.5	9	
			Range 6	-	-	11	15	
			Range 7	-	-	18.5	25	
			Range 8	-	-	62	80	
			Range 9	-	-	85	110	
			Range 10	-	-	110	130	
			Range 11	-	-	155	190	

1. Guaranteed by characterization results.
2. This is a deviation for an individual part once the initial frequency has been measured.
3. Sampling mode means Low-power run/Low-power sleep modes with Temperature sensor disable.
4. Guaranteed by design.

Figure 38. Typical current consumption versus MSI frequency



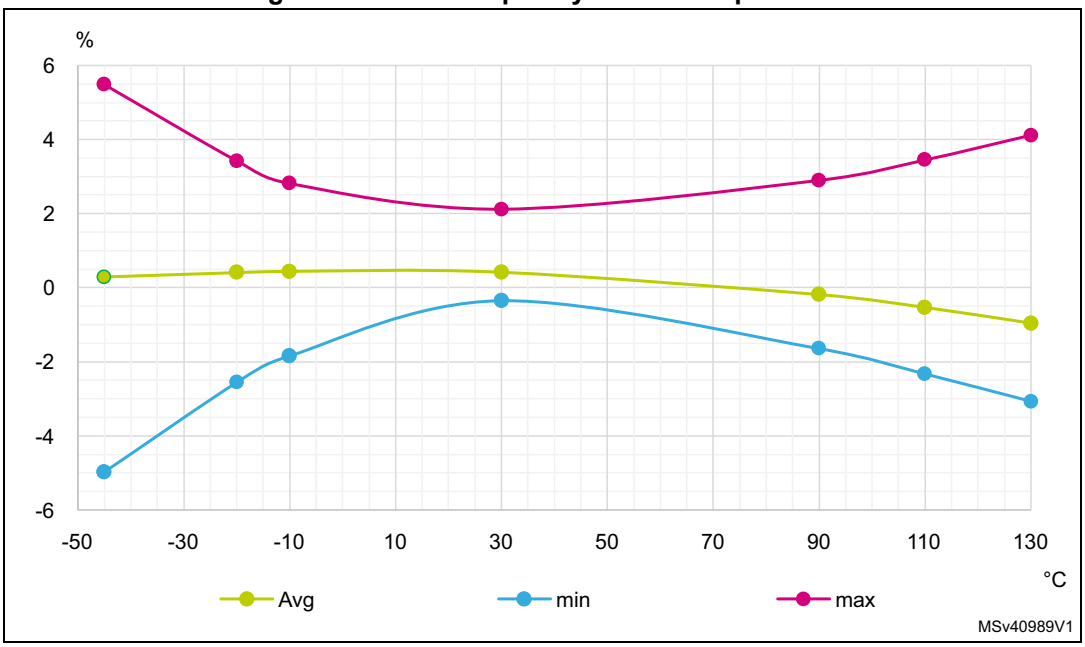
High-speed internal 48 MHz (HSI48) RC oscillator

Table 92. HSI48 oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI48}	HSI48 Frequency	V_{DD}=3.0V, T_A=30°C	-	48	-	MHz
TRIM	HSI48 user trimming step	-	-	0.11(2)	0.18(2)	%
USER TRIM COVERAGE	HSI48 user trimming coverage	±32 steps	±3(3)	±3.5(3)	-	%
DuCy(HSI48)	Duty Cycle	-	45(2)	-	55(2)	%
ACC_{HSI48_REL}	Accuracy of the HSI48 oscillator over temperature (factory calibrated)	V_{DD} = 3.0 V to 3.6 V, T_A = –15 to 85 °C	-	-	±3(3)	%
		V_{DD} = 1.65 V to 3.6 V, T_A = –40 to 125 °C	-	-	±4.5(3)	
D_{VDD}(HSI48)	HSI48 oscillator frequency drift with V_{DD}	V_{DD} = 3 V to 3.6 V	-	0.025(3)	0.05(3)	%
		V_{DD} = 1.65 V to 3.6 V	-	0.05(3)	0.1(3)	
t_{su}(HSI48)	HSI48 oscillator start-up time	-	-	2.5(2)	6(2)	µs
I_{DD}(HSI48)	HSI48 oscillator power consumption	-	-	340(2)	380(2)	µA
N_T jitter	Next transition jitter Accumulated jitter on 28 cycles(4)	-	-	+/-0.15(2)	-	ns
P_T jitter	Paired transition jitter Accumulated jitter on 56 cycles(4)	-	-	+/-0.25(2)	-	ns

1. V_{DD} = 3 V, T_A = –40 to 125°C unless otherwise specified.
2. Guaranteed by design.
3. Guaranteed by characterization results.
4. Jitter measurement are performed without clock source activated in parallel.

Figure 39. HSI48 frequency versus temperature



Low-speed internal (LSI) RC oscillator

Table 93. LSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	LSI Frequency	V_{DD} = 3.0 V, T_A = 30 °C	31.04	-	32.96	kHz
		V_{DD} = 1.62 to 3.6 V, T_A = -40 to 125 °C	29.5	-	34	
$t_{SU}(LSI)$(2)	LSI oscillator start-up time	-	-	80	130	µs
$t_{STAB}(LSI)$(2)	LSI oscillator stabilization time	5% of final frequency	-	125	180	µs
$I_{DD}(LSI)$(2)	LSI oscillator power consumption	-	-	110	180	nA

1. Guaranteed by characterization results.
2. Guaranteed by design.

5.3.10 PLL characteristics

The parameters given in *Table 94* are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in *Table 27: General operating conditions*.

Table 94. PLL, PLLSAI1, PLLSAI2 characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock(2)	-	2.66	-	16	MHz
	PLL input clock duty cycle	-	45	-	55	%
$f_{PLL\_P\_OUT}$	PLL multiplier output clock P	Voltage scaling Range 1	2.0645	-	80	MHz
		Voltage scaling Range 0	2.0645	-	110	
		Voltage scaling Range 2	2.0645	-	26	
$f_{PLL\_Q\_OUT}$	PLL multiplier output clock Q	Voltage scaling Range 1	8	-	80	
		Voltage scaling Range 0	8	-	110	
		Voltage scaling Range 2	8	-	26	
$f_{PLL\_R\_OUT}$	PLL multiplier output clock R	Voltage scaling Range 1	8	-	80	
		Voltage scaling Range 0	8	-	110	
		Voltage scaling Range 2	8	-	26	
f_{VCO_OUT}	PLL VCO output	Voltage scaling Range 1	64	-	344	
		Voltage scaling Range 2	64	-	128	
t_{LOCK}	PLL lock time	-	-	15	40	µs
Jitter	RMS cycle-to-cycle jitter	System clock 80 MHz	-	40	-	±ps
	RMS period jitter		-	30	-	
I_{DD}(PLL)	PLL power consumption on V_{DD}(1)	VCO freq = 64 MHz	-	150	200	µA
		VCO freq = 96 MHz	-	200	260	
		VCO freq = 192 MHz	-	300	380	
		VCO freq = 344 MHz	-	520	650	

1. Guaranteed by design.
2. Take care of using the appropriate division factor M to obtain the specified PLL input clock values. The M factor is shared between the 3 PLLs.

5.3.11 Flash memory characteristics

Table 95. Flash memory characteristics(1)

Symbol	Parameter	Conditions	Typ	Max	Unit
t_{prog}	64-bit programming time	-	81.69	83.35	µs
t_{prog_row}	One row (64 double word) programming time	Normal programming	2.61	2.67	ms
		Fast programming	NA	NA	
t_{prog_page}	One page (4 Kbytes) programming time	Normal programming	20.91	21.34	
		Fast programming	NA	NA	
t_{ERASE}	Page (4 Kbytes) erase time	-	22.02	24.47	
t_{prog_bank}	One bank (1 Mbyte) programming time	Normal programming	2.68	2.73	s
		Fast programming	NA	NA	
t_{ME}	Mass erase time (one or two banks)	-	22.13	24.59	ms
I_{DD}	Average consumption from V_{DD}	Write mode	3.1	NA	mA
		Erase mode	3.1	NA	
	Maximum current (peak)	Write mode	NA	NA	
		Erase mode	NA	NA	

1. Guaranteed by design.

Table 96. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Min(1)	Unit
N_{END}	Endurance	T_A = –40 to +105 °C	10	kcycles
t_{RET}	Data retention	1 kcycle(2) at T_A = 85 °C	30	Years
		1 kcycle(2) at T_A = 105 °C	15	
		1 kcycle(2) at T_A = 125 °C	7	
		10 kcycles(2) at T_A = 55 °C	30	
		10 kcycles(2) at T_A = 85 °C	15	
		10 kcycles(2) at T_A = 105 °C	10	

1. Guaranteed by characterization results.
2. Cycling performed over the whole temperature range.

5.3.12 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 97*. They are based on the EMS levels and classes defined in application note AN1709.

Table 97. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{HCLK} = 110 MHz, conforming to IEC 61000-4-2	3B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{HCLK} = 110 MHz, conforming to IEC 61000-4-4	5A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 98. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs [f_{HSE}/f_{HCLK}]	Unit
				8 MHz / 110 MHz	
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = 25°C, LQFP144 package compliant with IEC 61967-2	0.1 MHz to 30 MHz	4	dBµV
			30 MHz to 130 MHz	0	
			130 MHz to 1 GHz	16	
			1 GHz to 2 GHz	11	
			EMI Level	3.5	-

5.3.13 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the ANSI/JEDEC standard.

Table 99. ESD absolute maximum ratings

Symbol	Ratings	Conditions		Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to ANSI/ESDA/JEDEC JS-001		2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to ANSI/ESDA/JEDEC JS-002	LQFP144, LQFP100, WLCSP81	C1	250	
			Other packages	C2a	500	

1. Guaranteed by characterization results.

Static latch-up

Two complementary static tests are required on three parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with EIA/JESD 78E IC latch-up standard.

Table 100. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78E	Class II level A

5.3.14 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DDIOx} (for standard, 3.3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of the -5 µA/+0 µA range) or other functional failure (for example reset occurrence or oscillator frequency deviation).

The characterization results are given in *Table 101*.

Negative induced leakage current is caused by negative injection and positive induced leakage current is caused by positive injection.

Table 101. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}(1)	Injected current on all pins except TT_a, PB0, PB15, PE9, PG0	-5	NA	mA
	Injected current on pins PB0, PB15, PE9, PG0	0	NA	
	Injected current on TT_a pins	-5	0	

1. Guaranteed by characterization.

5.3.15 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 102* are derived from tests performed in *Table 27: General operating conditions*. All I/Os are designed as CMOS- and TTL-compliant.

Table 102. I/O static characteristics

Symbol	Parameter	Conditions		Min
V_{IL}(1)	I/O input low level voltage	All IOs except FT_c	1.62 V < V_{DDIOx} < 3.6 V	-
			1.62 V < V_{DDIOx} < 3.6 V	-
			1.08 V < V_{DDIOx} < 1.62 V	-
		FT_c	1.62 V < V_{DDIOx} < 3.6 V	-
			1.62 V < V_{DDIOx} < 3.6 V	-
			1.08 V < V_{DDIOx} < 1.62 V	-
V_{IH}(1)	I/O input high level voltage	All IOs except FT_c	1.62 V < V_{DDIOx} < 3.6 V	$0.7\times V_{DDIOx}$(2)
			1.62 V < V_{DDIOx} < 3.6 V	$0.49\times V_{DDIOX}$+0.26
			1.08 V < V_{DDIOx} < 1.62 V	$0.61\times V_{DDIOX}$+0.05
		FT_c	1.62 V < V_{DDIOx} < 3.6 V	$0.7\times V_{DDIOX}$(2)
			1.08 V < V_{DDIOx} < 1.62 V	$0.7\times V_{DDIOX}$(2)
V_{hys}(2)	Input hysteresis	TT_xx, FT_xx and NRST	1.62 V < V_{DDIOx} < 3.6 V	-
		FT_sx	1.08 V < V_{DDIOx} < 1.62 V	-

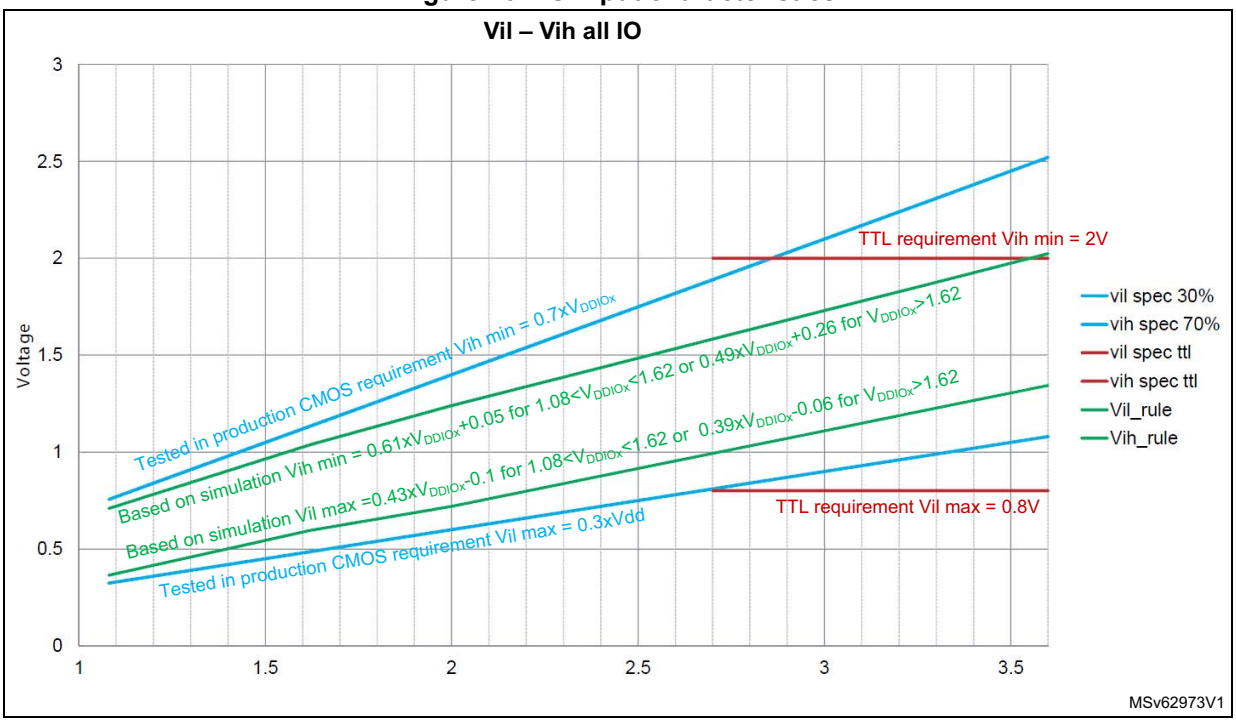
Table 102. I/O static characteristics (continued)

Symbol	Parameter	Conditions		Min
I_{lkg}	Input leakage current	FT_xx(3)	$0 < V_{IN} \le Max(V_{DDXXX})$(4)(5)	-
			$Max(V_{DDXXX}) \le V_{IN} \le Max(V_{DDXXX}) + 1\ V$(4)(5)	-
			$Max(V_{DDXXX}) + 1\ V < V_{IN} \le 5.5\ V$(4)(5)	-
		FT_u	$0 < V_{IN} \le Max(V_{DDXXX})$(4)(5)	-
			$Max(V_{DDXXX}) \le V_{IN} \le Max(V_{DDXXX}) + 1\ V$(4)(5)	-
			$Max(V_{DDXXX}) + 1\ V < VIN \le 5.5\ V$(4)(5)(7)	-
		TT_xx	$V_{IN} \le Max(V_{DDXXX})$(5)	-
			$Max(V_{DDXXX}) \le V_{IN} < 3.6\ V$(5)	-
		OPAMPx_VINM(x=1,2)	-	-
		FT_c	$0 < V_{IN} \le Max(V_{DDXXX})$(3)	-
			$Max(V_{DDXXX}) < V_{IN} \le 5\ V$(3)(5)(6)	-
		FT_d	$0 < V_{IN} \le Max(V_{DDXXX})$(5)	-
			$Max(V_{DDXXX}) < V_{IN} \le 5.5\ V$(3)(4)(5)	-
R_{PU}	Weak pull-up equivalent resistor		$V_{IN} = V_{SS}$	25
R_{PD}	Weak pull-down equivalent resistor		$V_{IN} = V_{DDIOx}$	25
C_{IO}	I/O pin capacitance		-	-

1. Refer to *Figure 40: I/O input characteristics*.
2. Guaranteed by design.
3. All FT_xx IO except FT_u and FT_c.
4. This value represents the pad leakage of the IO itself. The total product pad leakage is provided by this formula: $I_{Total\_Ileak\_max}$ = 10 applied on the pad] × I_{lkg}(Max).
5. Max(V_{DDXXX}) is the maximum value of all the I/O supplies. Refer to *Table: Legend/Abbreviations used in the pinout table*.
6. To sustain a voltage higher than MIN(V_{DD}, V_{DDA}, V_{DDIO2} and V_{DDUSB}) +0.3 V, the internal Pull-up and Pull-Down resistors must be
7. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS co minimal (~10% order).
8. Refer to I_{bias} in *Table 119: OPAMP characteristics* for the values of the OPAMP dedicated input leakage current.

All I/Os are CMOS- and TTL-compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 40* for standard I/Os, and in *Figure 40* for 5 V tolerant I/Os.

Figure 40. I/O input characteristics



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ± 20 mA (with a relaxed V_{OL}/V_{OH}).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 5.2*:

- The sum of the currents sourced by all the I/Os on V_{DDIOx}, plus the maximum consumption of the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating ΣI_{VDD} (see *Table 24: Voltage characteristics*).
- The sum of the currents sunk by all the I/Os on V_{SS}, plus the maximum consumption of the MCU sunk on V_{SS}, cannot exceed the absolute maximum rating ΣI_{VSS} (see *Table 24: Voltage characteristics*).

Output voltage levels

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 27: General operating conditions*. All I/Os are CMOS- and TTL-compliant (FT OR TT unless otherwise specified).

Table 103. Output voltage characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level voltage for an I/O pin	CMOS port(2) $\|I_{IO}\|$ = 2 mA for FT_c $\|I_{IO}\|$ = 8 mA for other I/Os V_{DDIOx} ≥ 2.7 V	-	0.4	V
V_{OH}	Output high level voltage for an I/O pin		V_{DDIOx}-0.4	-	
V_{OL}(3)	Output low level voltage for an I/O pin	TTL port(2) $\|I_{IO}\|$ = 2 mA for FT_c $\|I_{IO}\|$= 8 mA for other I/Os V_{DDIOx} ≥ 2.7 V	-	0.4	
V_{OH}(3)	Output high level voltage for an I/O pin		2.4	-	
V_{OL}(3)	Output low level voltage for an I/O pin	All I/Os except FT_c $\|I_{IO}\|$ = 20 mA V_{DDIOx} ≥ 2.7 V	-	1.3	
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DDIOx}-1.3	-	
V_{OL}(3)	Output low level voltage for an I/O pin	$\|I_{IO}\|$ = 1 mA for FT_c $\|I_{IO}\|$ = 4 mA for other I/Os 1.62 V ≤ V_{DDIOx} ≤ 3.6 V	-	0.4	
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DDIOx}-0.45	-	
V_{OL}(3)	Output low level voltage for an I/O pin	$\|I_{IO}\|$ = 1 mA for FT_c $\|I_{IO}\|$ = 2 mA for other I/Os 1.08 V ≤ V_{DDIOx} < 1.62 V	-	0.35 x V_{DDIOx}	
V_{OH}(3)	Output high level voltage for an I/O pin		0.65xV_{DDIOx}	-	
V_{OLFM+}(3)	Output low level voltage for an FT I/O pin in FM+ mode (FT I/O with "f" option)	$\|I_{IO}\|$ = 20 mA V_{DDIOx} ≥ 2.7 V	-	0.4	
		$\|I_{IO}\|$ = 10 mA 1.62 V ≤ V_{DDIOx} ≤ 3.6 V	-	0.4	
		$\|I_{IO}\|$ = 2 mA 1.08 V ≤ V_{DDIOx} < 1.62 V	-	0.4	

1. The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in *Table 24: Voltage characteristics*, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣI_{IO}.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. Guaranteed by design.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 41* and *Table 104*, respectively.

Unless otherwise specified, the parameters given are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 27: General operating conditions*.

Table 104. I/O AC characteristics (All I/Os except FT_c)(1)(2)

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
00	Fmax	Maximum frequency	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	5	MHz
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	1	
			C=50 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	0.1	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	10	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	1.5	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	0.1	
	Tr/Tf	Output rise and fall time	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	25	ns
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	52	
			C=50 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	140	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	17	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	37	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	110	
01	Fmax	Maximum frequency	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	25	MHz
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	10	
			C=50 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	1	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	50	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	15	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	1	
	Tr/Tf	Output rise and fall time	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	9	ns
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	16	
			C=50 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	40	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	4.5	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	9	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	21	

Table 104. I/O AC characteristics (All I/Os except FT_c)(1)(2) (continued)

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
10	Fmax	Maximum frequency	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	50	MHz
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	25	
			C=50 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	5	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	100	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	37.5	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	5	
	Tr/Tf	Output rise and fall time	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	5.8	ns
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	11	
			C=50 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	28	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	2.5	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	5	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	12	
11	Fmax	Maximum frequency	C=30 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	110	MHz
			C=30 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	50	
			C=30 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	10	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	180(3)	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	75	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	10	
	Tr/Tf	Output rise and fall time	C=30 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	3.3	ns
			C=30 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	6	
			C=30 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	16	
Fm+	Fmax	Maximum frequency	C=50 pF, 1.6 V≤V_{DDIOx}≤3.6 V	-	1	MHz
	Tf	Output fall time(4)		-	5	ns

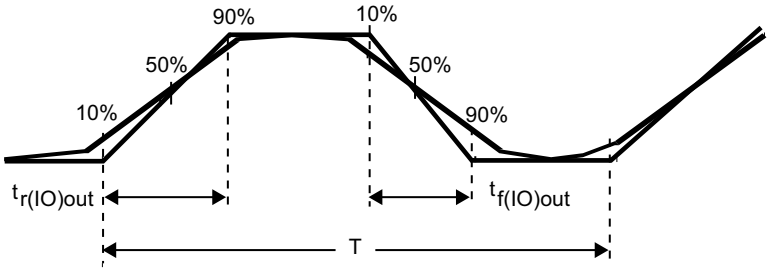
1. The I/O speed is configured using the OSPEEDRy[1:0] bits. The Fm+ mode is configured in the SYSCFG_CFGR1 register. Refer to the RM0438 reference manual for a description of GPIO Port configuration register.
2. Guaranteed by design.
3. This value represents the I/O capability but the maximum system frequency is limited to 110 MHz.
4. The fall time is defined between 70% and 30% of the output waveform accordingly to I^2C specification.

Table 105. FT_c I/O AC characteristics(1)(2)

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
0	Fmax	Maximum frequency	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	2	MHz
			C=50 pF, 1.6 V≤V_{DDIOx}≤2.7 V	-	1	
			C=50 pF, 1.08 V≤V_{DDIOx}≤3.6 V	-	0.1	
	Tr/Tf	Output rise and fall time	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	170	ns
			C=50 pF, 1.6 V≤V_{DDIOx}≤2.7 V	-	330	
			C=50 pF, 1.08 V≤V_{DDIOx}≤3.6 V	-	3300	
1	Fmax	Maximum frequency	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	10	MHz
			C=50 pF, 1.6 V≤V_{DDIOx}≤2.7 V	-	5	
			C=50 pF, 1.08 V≤V_{DDIOx}≤3.6 V	-	0.7	
	Tr/Tf	Output rise and fall time	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	35	ns
			C=50 pF, 1.6 V≤V_{DDIOx}≤2.7 V	-	65	
			C=50 pF, 1.08 V≤V_{DDIOx}≤3.6 V	-	400	

1. The I/O speed is configured using the OSPEEDRy[0] bit. Refer to the RM0438 reference manual for a description of GPIO Port configuration register.
2. Guaranteed by design.

Figure 41. I/O AC characteristics definition(1)



Maximum frequency is achieved if (t_r + t_f (≤ 2/3)T and if the duty cycle is (45-55%) when loaded by the specified capacitance.

MS32132V2

1. Refer to *Table 104: I/O AC characteristics (All I/Os except FT_c)*.

5.3.16 NRST pin characteristics

The NRST pin input driver uses the CMOS technology. It is connected to a permanent pull-up resistor, R_{PU}.

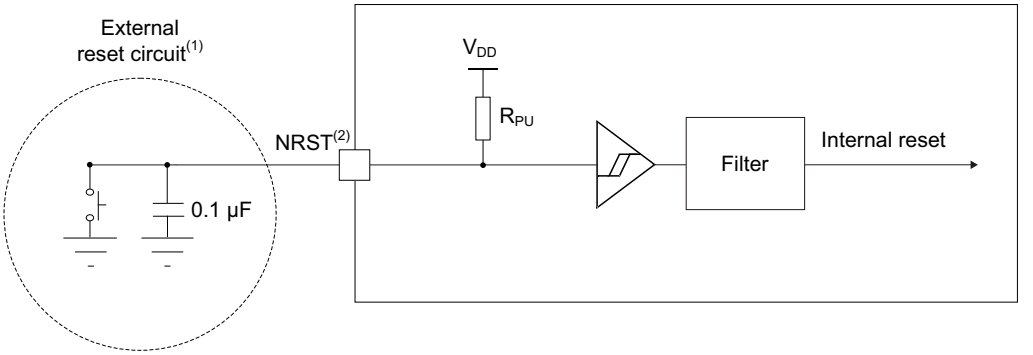
Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 27: General operating conditions*.

Table 106. NRST pin characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage	-	-	-	$0.3_x V_{DDIOx}$	V
$V_{IH(NRST)}$	NRST input high level voltage	-	$0.7_x V_{DDIOx}$	-	-	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	25	40	55	kΩ
$V_{F(NRST)}$	NRST input filtered pulse	-	-	-	70	ns
$V_{NF(NRST)}$	NRST input not filtered pulse	1.71 V ≤ V_{DD} ≤ 3.6 V	350	-	-	ns

1. Guaranteed by design.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimal (~10% order).

Figure 42. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 106: NRST pin characteristics*. Otherwise the reset is not taken into account by the device.
3. The external capacitor on NRST must be placed as close as possible to the device.

5.3.17 Extended interrupt and event controller input (EXTI) characteristics

The pulse on the interrupt input must have a minimal length in order to guarantee that it is detected by the event controller.

Table 107. EXTI input characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PLEC	Pulse length to event controller	-	20	-	-	ns

1. Guaranteed by design.

5.3.18 Analog switches booster

Table 108. Analog switches booster characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply voltage	1.62	-	3.6	V
$t_{SU(BOOST)}$	Booster startup time	-	-	240	µs
$I_{DD(BOOST)}$	Booster consumption for 1.62 V ≤ V_{DD} ≤ 2.0 V	-	-	250	µA
	Booster consumption for 2.0 V ≤ V_{DD} ≤ 2.7 V	-	-	500	
	Booster consumption for 2.7 V ≤ V_{DD} ≤ 3.6 V	-	-	900	

1. Guaranteed by design.

5.3.19 Analog-to-digital converter characteristics

Unless otherwise specified, the parameters given in *Table 109* are preliminary values derived from tests performed under ambient temperature, f_{PCLK} frequency and V_{DDA} supply voltage conditions summarized in *Table 27: General operating conditions*.

Note: It is recommended to perform a calibration after each power-up.

Table 109. ADC characteristics(1) (2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	1.62	-	3.6	V
V_{REF+}	Positive reference voltage	$V_{DDA} \geq 2$ V	2	-	V_{DDA}	V
		$V_{DDA} < 2$ V	V_{DDA}			V
V_{REF-}	Negative reference voltage	-	V_{SSA}			V
f_{ADC}	ADC clock frequency	Range 0 and 1	-	-	80	MHz
		Range 2	-	-	26	
f_s	Sampling rate for FAST channels	Resolution = 12 bits	-	-	5.33	Msps
		Resolution = 10 bits	-	-	6.15	
		Resolution = 8 bits	-	-	7.27	
		Resolution = 6 bits	-	-	8.88	
	Sampling rate for SLOW channels	Resolution = 12 bits	-	-	4.21	
		Resolution = 10 bits	-	-	4.71	
		Resolution = 8 bits	-	-	5.33	
		Resolution = 6 bits	-	-	6.15	
f_{TRIG}	External trigger frequency	f_{ADC} = 80 MHz Resolution = 12 bits	-	-	5.33	MHz
		Resolution = 12 bits	-	-	15	$1/f_{ADC}$
V_{AIN} (3)	Conversion voltage range(2)	-	0	-	V_{REF+}	V
R_{AIN}	External input impedance	-	-	-	50	kΩ
C_{ADC}	Internal sample and hold capacitor	-	-	5	-	pF
t_{STAB}	Power-up time	-	1			conversion cycle
t_{CAL}	Calibration time	f_{ADC} = 80 MHz	1.45			µs
		-	116			$1/f_{ADC}$

Table 109. ADC characteristics(1) (2) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{LATR}	Trigger conversion latency Regular and injected channels without conversion abort	CKMODE = 00	1.5	2	2.5	$1/f_{ADC}$
		CKMODE = 01	-	-	2.0	
		CKMODE = 10	-	-	2.25	
		CKMODE = 11	-	-	2.125	
$t_{LATRINJ}$	Trigger conversion latency Injected channels aborting a regular conversion	CKMODE = 00	2.5	3	3.5	$1/f_{ADC}$
		CKMODE = 01	-	-	3.0	
		CKMODE = 10	-	-	3.25	
		CKMODE = 11	-	-	3.125	
t_s	Sampling time	f_{ADC} = 80 MHz	0.03125	-	8.00625	µs
		-	2.5	-	640.5	$1/f_{ADC}$
$t_{ADCVREG\_STUP}$	ADC voltage regulator start-up time	-	-	-	20	µs
t_{CONV}	Total conversion time (including sampling time)	f_{ADC} = 80 MHz Resolution = 12 bits	0.1875	-	8.1625	µs
		Resolution = 12 bits	ts + 12.5 cycles for successive approximation = 15 to 653			$1/f_{ADC}$
I_{DDA}(ADC)	ADC consumption from the V_{DDA} supply	fs = 5 Msps	-	730	830	µA
		fs = 1 Msps	-	160	220	
		fs = 10 ksps	-	16	50	
I_{DDV_S}(ADC)	ADC consumption from the V_{REF+} single ended mode	fs = 5 Msps	-	130	160	µA
		fs = 1 Msps	-	30	40	
		fs = 10 ksps	-	0.6	2	
I_{DDV_D}(ADC)	ADC consumption from the V_{REF+} differential mode	fs = 5 Msps	-	260	310	µA
		fs = 1 Msps	-	60	70	
		fs = 10 ksps	-	1.3	3	

1. Guaranteed by design
2. The I/O analog switch voltage booster is enable when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4V). It is disable when V_{DDA} ≥ 2.4 V.
3. V_{REF+} can be internally connected to V_{DDA} and V_{REF-} can be internally connected to V_{SSA}, depending on the package.
   Refer to *Section 4: Pinouts and pin description* for further details.

The maximum value of R_{AIN} can be found in *Table 110: Maximum ADC RAIN*.

Table 110. Maximum ADC R_{AIN}(1)(2)

Resolution	Sampling cycle @80 MHz	Sampling time [ns] @80 MHz	R_{AIN} max (Ω)	
			Fast channels(3)	Slow channels(4)
12 bits	2.5	31.25	100	N/A
	6.5	81.25	330	100
	12.5	156.25	680	470
	24.5	306.25	1500	1200
	47.5	593.75	2200	1800
	92.5	1156.25	4700	3900
	247.5	3093.75	12000	10000
	640.5	8006.75	39000	33000
10 bits	2.5	31.25	120	N/A
	6.5	81.25	390	180
	12.5	156.25	820	560
	24.5	306.25	1500	1200
	47.5	593.75	2200	1800
	92.5	1156.25	5600	4700
	247.5	3093.75	12000	10000
	640.5	8006.75	47000	39000
8 bits	2.5	31.25	180	N/A
	6.5	81.25	470	270
	12.5	156.25	1000	680
	24.5	306.25	1800	1500
	47.5	593.75	2700	2200
	92.5	1156.25	6800	5600
	247.5	3093.75	15000	12000
	640.5	8006.75	50000	50000
6 bits	2.5	31.25	220	N/A
	6.5	81.25	560	330
	12.5	156.25	1200	1000
	24.5	306.25	2700	2200
	47.5	593.75	3900	3300
	92.5	1156.25	8200	6800
	247.5	3093.75	18000	15000
	640.5	8006.75	50000	50000

1. Guaranteed by design.
2. The I/O analog switch voltage booster is enable when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4V). It is disable when V_{DDA} ≥ 2.4 V.
3. Fast channels are: PC0, PC1, PC2, PC3, PA0.
4. Slow channels are: all ADC inputs except the fast channels.

Table 111. ADC accuracy - limited test conditions 1(1)(2)(3)

Sym-bol	Parameter	Conditions(4)			Min	Typ	Max	Unit
ET	Total unadjusted error	ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, V_{DDA} = VREF+ = 3 V, TA = 25 °C (ADC clock frequency ≤ 58 MHz for LQFP144)	Single ended	Fast channel (max speed)	-	4	5	LSB
				Slow channel (max speed)	-	4	5	
			Differential	Fast channel (max speed)	-	3.5	4.5	
				Slow channel (max speed)	-	3.5	4.5	
EO	Offset error		Single ended	Fast channel (max speed)	-	1	2.5	
				Slow channel (max speed)	-	1	2.5	
			Differential	Fast channel (max speed)	-	1.5	2.5	
				Slow channel (max speed)	-	1.5	2.5	
EG	Gain error		Single ended	Fast channel (max speed)	-	2.5	4.5	
				Slow channel (max speed)	-	2.5	4.5	
			Differential	Fast channel (max speed)	-	2.5	3.5	
				Slow channel (max speed)	-	2.5	3.5	
ED	Differential linearity error		Single ended	Fast channel (max speed)	-	1	3.5	
				Slow channel (max speed)	-	1	3.5	
			Differential	Fast channel (max speed)	-	1	2	
				Slow channel (max speed)	-	1	2	
EL	Integral linearity error		Single ended	Fast channel (max speed)	-	1.5	2.5	
				Slow channel (max speed)	-	1.5	2.5	
			Differential	Fast channel (max speed)	-	1	2	
				Slow channel (max speed)	-	1	2	
ENOB	Effective number of bits		Single ended	Fast channel (max speed)	10.4	10.5	-	bits
				Slow channel (max speed)	10.4	10.5	-	
			Differential	Fast channel (max speed)	10.8	10.9	-	
				Slow channel (max speed)	10.8	10.9	-	
SINAD	Signal-to-noise and distortion ratio		Single ended	Fast channel (max speed)	64.4	65	-	dB
				Slow channel (max speed)	64.4	65	-	
			Differential	Fast channel (max speed)	66.8	67.4	-	
				Slow channel (max speed)	66.8	67.4	-	
SNR	Signal-to-noise ratio		Single ended	Fast channel (max speed)	65	66	-	
				Slow channel (max speed)	65	66	-	
			Differential	Fast channel (max speed)	67	68	-	
				Slow channel (max speed)	67	68	-	

Table 111. ADC accuracy - limited test conditions 1(1)(2)(3) (continued)

Sym-bol	Parameter	Conditions(4)			Min	Typ	Max	Unit
THD	Total harmonic distortion	ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, $V_{DDA} = V_{REF+}$ = 3 V, TA = 25 °C (ADC clock frequency ≤ 58 MHz for LQFP144)	Single ended	Fast channel (max speed)	-	-74	-73	dB
				Slow channel (max speed)	-	-74	-73	
			Differential	Fast channel (max speed)	-	-79	-76	
				Slow channel (max speed)	-	-79	-76	

1. Guaranteed by design.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
4. The I/O analog switch voltage booster is enable when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4 V). It is disable when V_{DDA} ≥ 2.4 V. No oversampling.

Table 112. ADC accuracy - limited test conditions 2(1)(2)(3)

Sym-bol	Parameter	Conditions(4)			Min	Typ	Max	Unit
ET	Total unadjusted error	ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, 2 V ≤ V_{DDA} (ADC clock frequency ≤ 58 MHz for LQFP144)	Single ended	Fast channel (max speed)	-	4	6.5	LSB
				Slow channel (max speed)	-	4	6.5	
			Differential	Fast channel (max speed)	-	3.5	5.5	
				Slow channel (max speed)	-	3.5	5.5	
EO	Offset error		Single ended	Fast channel (max speed)	-	1	4.5	
				Slow channel (max speed)	-	1	5	
			Differential	Fast channel (max speed)	-	1.5	3	
				Slow channel (max speed)	-	1.5	3	
EG	Gain error		Single ended	Fast channel (max speed)	-	2.5	6	
				Slow channel (max speed)	-	2.5	6	
			Differential	Fast channel (max speed)	-	2.5	3.5	
				Slow channel (max speed)	-	2.5	3.5	
ED	Differential linearity error		Single ended	Fast channel (max speed)	-	1	3.5	
				Slow channel (max speed)	-	1	3.5	
			Differential	Fast channel (max speed)	-	1	2	
				Slow channel (max speed)	-	1	2	
EL	Integral linearity error		Single ended	Fast channel (max speed)	-	2.5	4.5	
				Slow channel (max speed)	-	2.5	4.5	
			Differential	Fast channel (max speed)	-	1	3	
				Slow channel (max speed)	-	1	2.5	
ENOB	Effective number of bits		Single ended	Fast channel (max speed)	10	10.5	-	bits
				Slow channel (max speed)	10	10.5	-	
			Differential	Fast channel (max speed)	10.7	10.9	-	
				Slow channel (max speed)	10.7	10.9	-	
SINAD	Signal-to-noise and distortion ratio		Single ended	Fast channel (max speed)	62	65	-	dB
				Slow channel (max speed)	62	65	-	
			Differential	Fast channel (max speed)	66	67.4	-	
				Slow channel (max speed)	66	67.4	-	
SNR	Signal-to-noise ratio		Single ended	Fast channel (max speed)	64	66	-	
				Slow channel (max speed)	64	66	-	
			Differential	Fast channel (max speed)	66.5	68	-	
				Slow channel (max speed)	66.5	68	-	

Table 112. ADC accuracy - limited test conditions 2(1)(2)(3) (continued)

Sym-bol	Parameter	Conditions(4)			Min	Typ	Max	Unit
THD	Total harmonic distortion	ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, 2 V ≤ V_{DDA} (ADC clock frequency ≤ 58 MHz for LQFP144)	Single ended	Fast channel (max speed)	-	-74	-65	dB
				Slow channel (max speed)	-	-74	-67	
			Differential	Fast channel (max speed)	-	-79	-70	
				Slow channel (max speed)	-	-79	-71	

1. Guaranteed by design.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
4. The I/O analog switch voltage booster is enable when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4 V). It is disable when V_{DDA} ≥ 2.4 V. No oversampling.

Table 113. ADC accuracy - limited test conditions 3(1)(2)(3)

Sym-bol	Parameter	Conditions(4)			Min	Typ	Max	Unit
ET	Total unadjusted error	ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, 1.65 V ≤ V_{DDA} = V_{REF+} ≤ 3.6 V, Voltage scaling Range 1 (ADC clock frequency ≤ 58 MHz for LQFP144)	Single ended	Fast channel (max speed)	-	5.5	7.5	LSB
				Slow channel (max speed)	-	4.5	6.5	
			Differential	Fast channel (max speed)	-	4.5	7.5	
				Slow channel (max speed)	-	4.5	5.5	
EO	Offset error		Single ended	Fast channel (max speed)	-	2	5	
				Slow channel (max speed)	-	2.5	5	
			Differential	Fast channel (max speed)	-	2	3.5	
				Slow channel (max speed)	-	2.5	3	
EG	Gain error		Single ended	Fast channel (max speed)	-	4.5	7	
				Slow channel (max speed)	-	3.5	6	
			Differential	Fast channel (max speed)	-	3.5	4	
				Slow channel (max speed)	-	3.5	5	
ED	Differential linearity error		Single ended	Fast channel (max speed)	-	1	3.5	
				Slow channel (max speed)	-	1	3.5	
			Differential	Fast channel (max speed)	-	1	2	
				Slow channel (max speed)	-	1	2	
EL	Integral linearity error		Single ended	Fast channel (max speed)	-	2.5	4.5	
				Slow channel (max speed)	-	2.5	4.5	
			Differential	Fast channel (max speed)	-	2	2.5	
				Slow channel (max speed)	-	2	2.5	
ENOB	Effective number of bits		Single ended	Fast channel (max speed)	10	10.4	-	bits
				Slow channel (max speed)	10	10.4	-	
			Differential	Fast channel (max speed)	10.6	10.7	-	
				Slow channel (max speed)	10.6	10.7	-	
SINAD	Signal-to-noise and distortion ratio		Single ended	Fast channel (max speed)	62	64	-	dB
				Slow channel (max speed)	62	64	-	
			Differential	Fast channel (max speed)	65	66	-	
				Slow channel (max speed)	65	66	-	
SNR	Signal-to-noise ratio		Single ended	Fast channel (max speed)	63	65	-	
				Slow channel (max speed)	63	65	-	
			Differential	Fast channel (max speed)	66	67	-	
				Slow channel (max speed)	66	67	-	

Table 113. ADC accuracy - limited test conditions 3(1)(2)(3) (continued)

Sym-bol	Parameter	Conditions(4)			Min	Typ	Max	Unit
THD	Total harmonic distortion	ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, 1.65 V ≤ V_{DDA} = V_{REF+} ≤ 3.6 V, Voltage scaling Range 1 (ADC clock frequency ≤ 58 MHz for LQFP144)	Single ended	Fast channel (max speed)	-	-69	-67	dB
				Slow channel (max speed)	-	-71	-67	
			Differential	Fast channel (max speed)	-	-72	-71	
				Slow channel (max speed)	-	-72	-71	

1. Guaranteed by design.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
4. The I/O analog switch voltage booster is enable when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4 V). It is disable when V_{DDA} ≥ 2.4 V. No oversampling.

Table 114. ADC accuracy - limited test conditions 4(1)(2)(3)

Sym-bol	Parameter	Conditions(4)			Min	Typ	Max	Unit
ET	Total unadjusted error	ADC clock frequency ≤ 26 MHz, 1.65 V ≤ V_{DDA} = VREF+ ≤ 3.6 V, Voltage scaling Range 2	Single ended	Fast channel (max speed)	-	5	5.4	LSB
				Slow channel (max speed)	-	4	5	
			Differential	Fast channel (max speed)	-	4	5	
				Slow channel (max speed)	-	3.5	4.5	
EO	Offset error		Single ended	Fast channel (max speed)	-	2	4	
				Slow channel (max speed)	-	2	4	
			Differential	Fast channel (max speed)	-	2	3.5	
				Slow channel (max speed)	-	2	3.5	
EG	Gain error		Single ended	Fast channel (max speed)	-	4	4.5	
				Slow channel (max speed)	-	4	4.5	
			Differential	Fast channel (max speed)	-	3	4	
				Slow channel (max speed)	-	3	4	
ED	Differential linearity error		Single ended	Fast channel (max speed)	-	1	1.5	
				Slow channel (max speed)	-	1	1.5	
			Differential	Fast channel (max speed)	-	1	1.2	
				Slow channel (max speed)	-	1	1.2	
EL	Integral linearity error		Single ended	Fast channel (max speed)	-	2.5	3	
				Slow channel (max speed)	-	2.5	3	
			Differential	Fast channel (max speed)	-	2	2.5	
				Slow channel (max speed)	-	2	2.5	
ENOB	Effective number of bits		Single ended	Fast channel (max speed)	10.2	10.5	-	bits
				Slow channel (max speed)	10.2	10.5	-	
			Differential	Fast channel (max speed)	10.6	10.7	-	
				Slow channel (max speed)	10.6	10.7	-	
SINAD	Signal-to-noise and distortion ratio		Single ended	Fast channel (max speed)	63	65	-	dB
				Slow channel (max speed)	63	65	-	
			Differential	Fast channel (max speed)	65	66	-	
				Slow channel (max speed)	65	66	-	
SNR	Signal-to-noise ratio		Single ended	Fast channel (max speed)	64	65	-	
				Slow channel (max speed)	64	65	-	
			Differential	Fast channel (max speed)	66	67	-	
				Slow channel (max speed)	66	67	-	

Table 114. ADC accuracy - limited test conditions 4(1)(2)(3) (continued)

Sym-bol	Parameter	Conditions(4)			Min	Typ	Max	Unit
THD	Total harmonic distortion	ADC clock frequency ≤ 26 MHz, 1.65 V ≤ V_{DDA} = VREF+ ≤ 3.6 V, Voltage scaling Range 2	Single ended	Fast channel (max speed)	-	-71	-69	dB
				Slow channel (max speed)	-	-71	-69	
			Differential	Fast channel (max speed)	-	-73	-72	
				Slow channel (max speed)	-	-73	-72	

1. Guaranteed by design.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
4. The I/O analog switch voltage booster is enable when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4 V). It is disable when V_{DDA} ≥ 2.4 V. No oversampling.

Figure 43. ADC accuracy characteristics

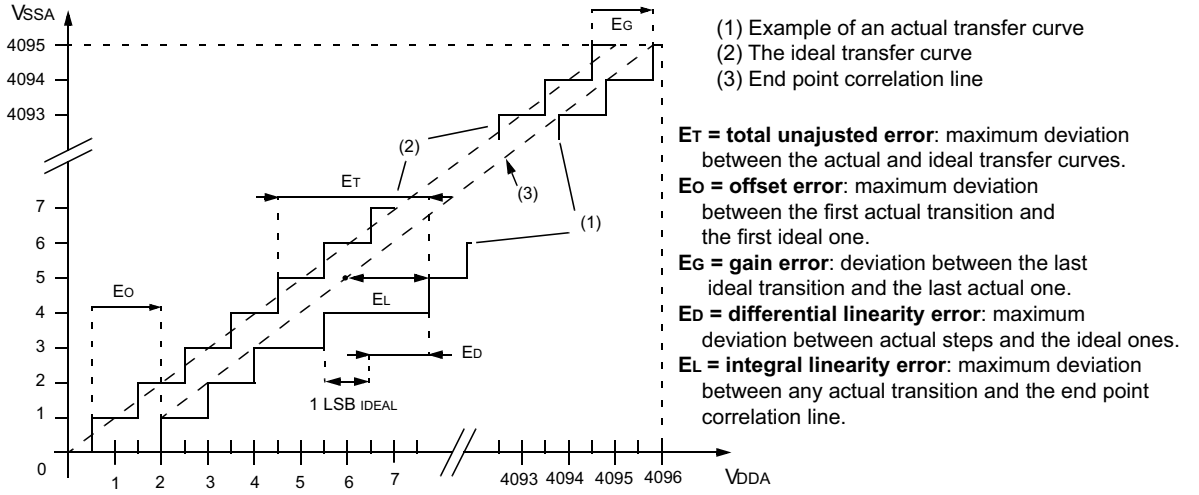
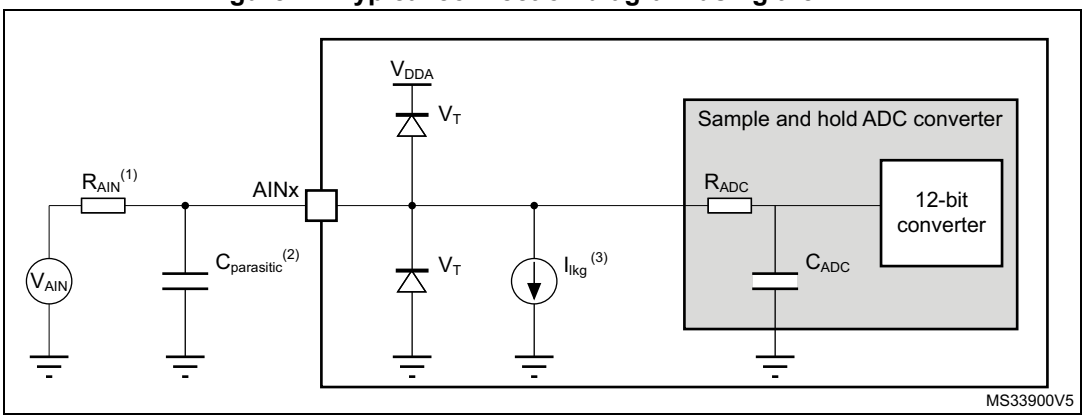


Figure 44. Typical connection diagram using the ADC



1. Refer to *Table 109: ADC characteristics* for the values of R_{AIN} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (refer to *Table 102: I/O static characteristics* for the value of the pad capacitance). A high $C_{parasitic}$ value downgrades the conversion accuracy. To remedy this, f_{ADC} should be reduced.
3. Refer to *Table 102: I/O static characteristics* for the values of I_{lkg}.

General PCB design guidelines

Power supply decoupling should be performed as shown in the corresponding power supply scheme. The 10 nF capacitor should be ceramic (good quality) and it should be placed as close as possible to the chip.

5.3.20 Digital-to-Analog converter characteristics

Table 115. DAC characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage for DAC ON	DAC output buffer OFF, DAC_OUT pin not connected (internal connection only)		1.71	-	3.6	V
		Other modes		1.80	-		
V_{REF+}	Positive reference voltage	DAC output buffer OFF, DAC_OUT pin not connected (internal connection only)		1.71	-	V_{DDA}	
		Other modes		1.80	-		
V_{REF-}	Negative reference voltage	-		V_{SSA}			
R_L	Resistive load	DAC output buffer ON	connected to V_{SSA}	5	-	-	kΩ
			connected to V_{DDA}	25	-	-	
R_O	Output Impedance	DAC output buffer OFF		9.6	11.7	13.8	kΩ
R_{BON}	Output impedance sample and hold mode, output buffer ON	V_{DD} = 2.7 V		-	-	2	kΩ
		V_{DD} = 2.0 V		-	-	3.5	
R_{BOFF}	Output impedance sample and hold mode, output buffer OFF	V_{DD} = 2.7 V		-	-	16.5	kΩ
		V_{DD} = 2.0 V		-	-	18.0	
C_L	Capacitive load	DAC output buffer ON		-	-	50	pF
C_{SH}		Sample and hold mode		-	0.1	1	µF
V_{DAC_OUT}	Voltage on DAC_OUT output	DAC output buffer ON		0.2	-	V_{REF+} – 0.2	V
		DAC output buffer OFF		0	-	V_{REF+}	
$t_{SETTLING}$	Settling time (full scale: for a 12-bit code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±0.5LSB, ±1 LSB, ±2 LSB, ±4 LSB, ±8 LSB)	Normal mode DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ	±0.5 LSB	-	1.7	3	µs
			±1 LSB	-	1.6	2.9	
			±2 LSB	-	1.55	2.85	
			±4 LSB	-	1.48	2.8	
			±8 LSB	-	1.4	2.75	
		Normal mode DAC output buffer OFF, ±1LSB, CL = 10 pF		-	2	2.5	
t_{WAKEUP}(2)	Wakeup time from off state (setting the ENx bit in the DAC Control register) until final value ±1 LSB	Normal mode DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		-	4.2	7.5	µs
		Normal mode DAC output buffer OFF, CL ≤ 10 pF		-	2	5	
PSRR	V_{DDA} supply rejection ratio	Normal mode DAC output buffer ON CL ≤ 50 pF, RL = 5 kΩ, DC		-	-80	-28	dB

Table 115. DAC characteristics(1) (continued)

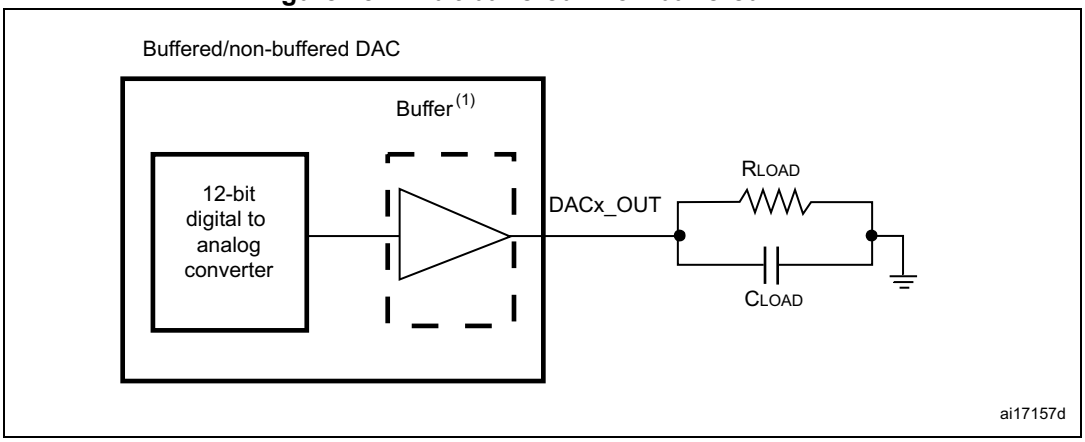
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$T_{W\_to\_W}$	Minimal time between two consecutive writes into the DAC_DORx register to guarantee a correct DAC_OUT for a small variation of the input code (1 LSB) DAC_MCR:MODEx[2:0] = 000 or 001 DAC_MCR:MODEx[2:0] = 010 or 011	CL ≤ 50 pF, RL ≥ 5 kΩ CL ≤ 10 pF		1 1.4	-	-	µs
t_{SAMP}	Sampling time in sample and hold mode (code transition between the lowest input code and the highest input code when DACOUT reaches final value ±1LSB)	DAC_OUT pin connected	DAC output buffer ON, C_{SH} = 100 nF	-	0.7	3.5	ms
			DAC output buffer OFF, C_{SH} = 100 nF	-	10.5	18	
		DAC_OUT pin not connected (internal connection only)	DAC output buffer OFF	-	2	3.5	µs
I_{leak}	Output leakage current	Sample and hold mode, DAC_OUT pin connected		-	-	-(3)	nA
CI_{int}	Internal sample and hold capacitor	-		5.2	7	8.8	pF
t_{TRIM}	Middle code offset trim time	DAC output buffer ON		50	-	-	µs
V_{offset}	Middle code offset for 1 trim code step	V_{REF+} = 3.6 V		-	1500	-	µV
		V_{REF+} = 1.8 V		-	750	-	
I_{DDA}(DAC)	DAC consumption from V_{DDA}	DAC output buffer ON	No load, middle code (0x800)	-	315	500	µA
			No load, worst code (0xF1C)	-	450	670	
		DAC output buffer OFF	No load, middle code (0x800)	-	-	0.2	
		Sample and hold mode, C_{SH} = 100 nF		-	315 x Ton/(Ton +Toff) (4)	670 x Ton/(Ton +Toff) (4)	

Table 115. DAC characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{DDV}(DAC)	DAC consumption from V_{REF+}	DAC output buffer ON	No load, middle code (0x800)	-	185	240	µA
			No load, worst code (0xF1C)	-	340	400	
		DAC output buffer OFF	No load, middle code (0x800)	-	155	205	
		Sample and hold mode, buffer ON, C_{SH} = 100 nF, worst case		-	185 x Ton/(Ton +Toff) (4)	400 x Ton/(Ton +Toff) (4)	
		Sample and hold mode, buffer OFF, C_{SH} = 100 nF, worst case		-	155 x Ton/(Ton +Toff) (4)	205 x Ton/(Ton +Toff) (4)	

1. Guaranteed by design.
2. In buffered mode, the output can overshoot above the final value for low input code (starting from min value).
3. Refer to *Table 102: I/O static characteristics*.
4. Ton is the Refresh phase duration. Toff is the Hold phase duration. Refer to RM0351 reference manual for more details.

Figure 45. 12-bit buffered / non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

Table 116. DAC accuracy ranges 0/1(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
DNL	Differential non linearity (2)	DAC output buffer ON		-	-	±2	LSB
		DAC output buffer OFF		-	-	±2	
-	monotonicity	10 bits		guaranteed			
INL	Integral non linearity(3)	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		-	-	±4	
		DAC output buffer OFF CL ≤ 50 pF, no RL		-	-	±4	
Offset	Offset error at code 0x800(3)	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ	V_{REF+} = 3.6 V	-	-	±12	
			V_{REF+} = 1.8 V	-	-	±25	
		DAC output buffer OFF CL ≤ 50 pF, no RL		-	-	±8	
Offset1	Offset error at code 0x001(4)	DAC output buffer OFF CL ≤ 50 pF, no RL		-	-	±5	
OffsetCal	Offset Error at code 0x800 after calibration	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ	V_{REF+} = 3.6 V	-	-	±5	
			V_{REF+} = 1.8 V	-	-	±7	
Gain	Gain error(5)	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		-	-	±0.5	%
		DAC output buffer OFF CL ≤ 50 pF, no RL		-	-	±0.5	
TUE	Total unadjusted error	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		-	-	±30	LSB
		DAC output buffer OFF CL ≤ 50 pF, no RL		-	-	±12	
TUECal	Total unadjusted error after calibration	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		-	-	±23	LSB
SNR	Signal-to-noise ratio	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ 1 kHz, BW 500 kHz		-	71.2	-	dB
		DAC output buffer OFF CL ≤ 50 pF, no RL, 1 kHz BW 500 kHz		-	71.6	-	
THD	Total harmonic distortion	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ, 1 kHz		-	-78	-	dB
		DAC output buffer OFF CL ≤ 50 pF, no RL, 1 kHz		-	-79	-	

Table 116. DAC accuracy ranges 0/1(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SINAD	Signal-to-noise and distortion ratio	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ, 1 kHz	-	70.4	-	dB
		DAC output buffer OFF CL ≤ 50 pF, no RL, 1 kHz	-	71	-	
ENOB	Effective number of bits	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ, 1 kHz	-	11.4	-	bits
		DAC output buffer OFF CL ≤ 50 pF, no RL, 1 kHz	-	11.5	-	

1. Guaranteed by design.
2. Difference between two consecutive codes - 1 LSB.
3. Difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 4095.
4. Difference between the value measured at Code (0x001) and the ideal value.
5. Difference between ideal slope of the transfer function and measured slope computed from code 0x000 and 0xFFF when buffer is OFF, and from code giving 0.2 V and (V_{REF+} – 0.2) V when buffer is ON.

5.3.21 Voltage reference buffer characteristics

Table 117. VREFBUF characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	Normal mode	V_{RS} = 0	2.4	-	3.6	V
			V_{RS} = 1	2.8	-	3.6	
		Degraded mode(2)	V_{RS} = 0	1.65	-	2.4	
			V_{RS} = 1	1.65	-	2.8	
V_{REFBUF_OUT}	Voltage reference output	Normal mode I_{load}=100 µA/T=30°C	V_{RS} = 0	2.044	2.048	2.052	
			V_{RS} = 1	2.496	2.5	2.504	
		Degraded mode(2)	V_{RS} = 0	V_{DDA}-250 mV	-	V_{DDA}	
			V_{RS} = 1	V_{DDA}-250 mV	-	V_{DDA}	
ΔV_{REFOUT_VDD}	Voltage reference output spread over the main supply range	Normal mode	VRS=0	-	-	5	mV
			VRS=1	-	-	4	mV
TRIM	Trim step resolution	-	-	-	±0.05	±0.1	%
CL	Load capacitor	-	-	0.5	1	1.5	µF
esr	Equivalent Serial Resistor of Cload	-	-	-	-	2	Ω
I_{load}	Static load current	-	-	-	-	4	mA
I_{line_reg}	Line regulation	2.8 V ≤ V_{DDA} ≤ 3.6 V	I_{load} = 500 µA	-	-	2000	ppm/V
			I_{load} = 4 mA	-	100	500	
I_{load_reg}	Load regulation	500 µA ≤ I_{load} ≤4 mA	Normal mode	-	50	500	ppm/mA
T_{Coeff}	Temperature coefficient	-40 °C < TJ < +125 °C		-	-	$T_{coeff\_vrefint}$ + 50	ppm/ °C
		0 °C < TJ < +50 °C		-	-	$T_{coeff\_vrefint}$ + 50	
PSRR	Power supply rejection	DC		40	55	-	dB
		100 kHz		25	40	-	
t_{START}	Start-up time	CL = 0.5 µF(3)		-	300	350	µs
		CL = 1.1 µF(3)		-	500	650	
		CL = 1.5 µF(3)		-	650	800	

Table 117. VREFBUF characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{INRUSH}	Control of maximum DC current drive on VREFBUF_OUT during start-up phase (4)	-	-	-	8	-	mA
I_{DDA}(VREFBUF)	VREFBUF consumption from V_{DDA}	I_{load} = 0 µA		-	16	25	µA
		I_{load} = 500 µA		-	18	30	
		I_{load} = 4 mA		-	35	50	

1. Guaranteed by design and characterization result, unless otherwise specified.
2. In degraded mode, the voltage reference buffer can not maintain accurately the output voltage which follows (V_{DDA} - drop voltage).
3. The capacitive load must include a 100 nF capacitor in order to cut-off the high frequency noise.
4. To correctly control the VREFBUF inrush current during start-up phase and scaling change, the V_{DDA} voltage should be in the range [2.4 V to 3.6 V] and [2.8 V to 3.6 V] respectively for V_{RS} = 0 and V_{RS} = 1.

Figure 46. VREFBUF in case VRS = 0

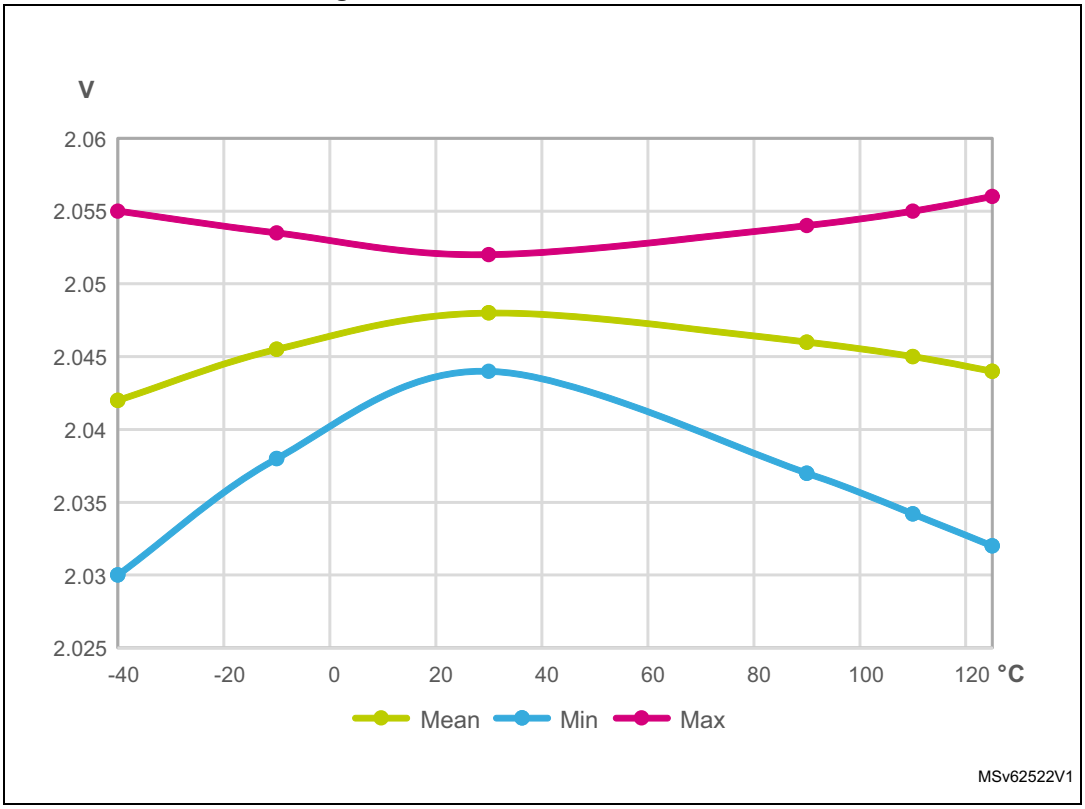
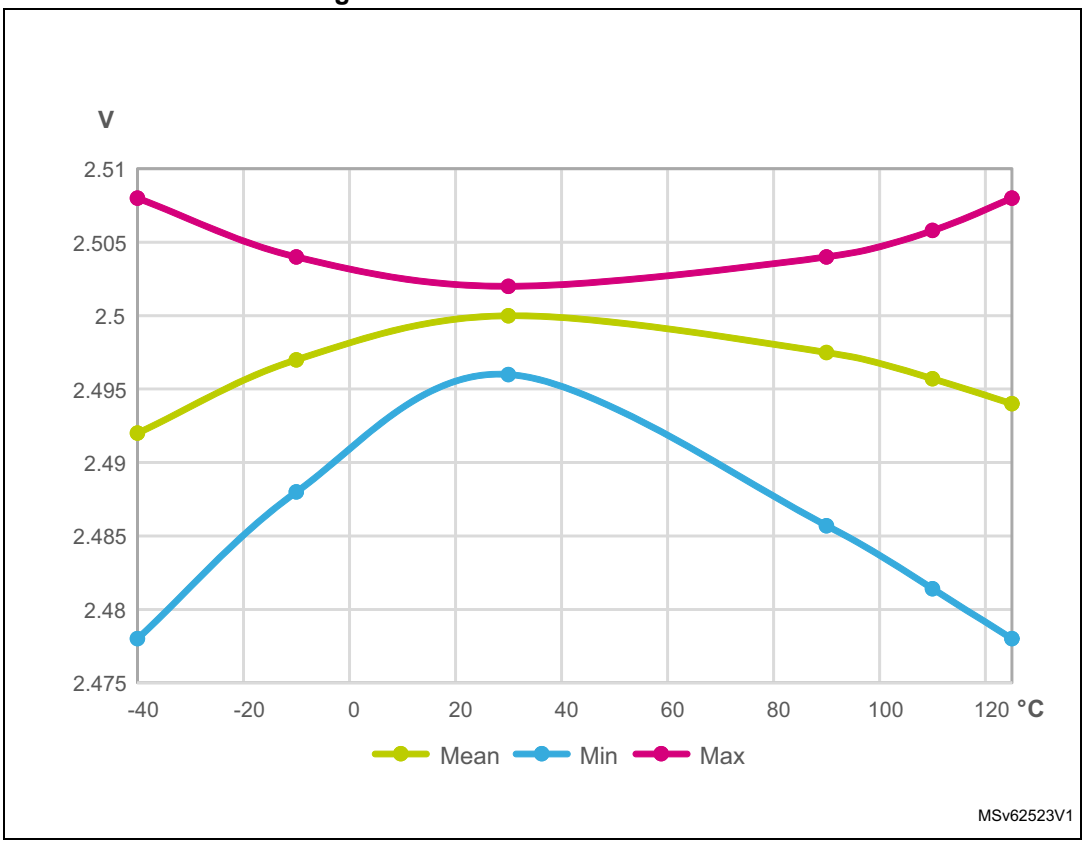


Figure 47. VREFBUF in case VRS = 1



5.3.22 Comparator characteristics

Table 118. COMP characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-		1.62	-	3.6	V
V_{IN}	Comparator input voltage range	-		0	-	V_{DDA}	V
V_{BG}(2)	Scaler input voltage	-		V_{REFINT}			V
V_{SC}	Scaler offset voltage	-		-	±5	±10	mV
I_{DDA}(SCALER)	Scaler static consumption from V_{DDA}	BRG_EN=0 (bridge disable)		-	200	300	nA
		BRG_EN=1 (bridge enable)		-	0.8	1	µA
t_{START_SCALER}	Scaler startup time	-		-	100	200	µs
t_{START}	Comparator startup time to reach propagation delay specification	High-speed mode	$V_{DDA} \geq 2.7$ V	-	-	5	µs
			$V_{DDA} < 2.7$ V	-	-	7	
		Medium mode	$V_{DDA} \geq 2.7$ V	-	-	15	
			$V_{DDA} < 2.7$ V	-	-	25	
		Ultra-low-power mode		-	-	80	
t_D(3)	Propagation delay for 200 mV step with 100 mV overdrive	High-speed mode	$V_{DDA} \geq 2.7$ V	-	55	80	ns
			$V_{DDA} < 2.7$ V	-	65	100	
		Medium mode	$V_{DDA} \geq 2.7$ V	-	0.55	0.9	µs
			$V_{DDA} < 2.7$ V	-	0.65	1	
		Ultra-low-power mode		-	5	12	
V_{offset}	Comparator offset error	Full common mode range	-	-	±5	±20	mV
V_{hys}	Comparator hysteresis	No hysteresis		-	0	-	mV
		Low hysteresis		-	8	-	
		Medium hysteresis		-	15	-	
		High hysteresis		-	27	-	

Table 118. COMP characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{DDA}(COMP)	Comparator consumption from V_{DDA}	Ultra-low-power mode	Static	-	400	600	nA
			With 50 kHz ±100 mV overdrive square signal	-	1200	-	
		Medium mode	Static	-	5	7	µA
			With 50 kHz ±100 mV overdrive square signal	-	6	-	
		High-speed mode	Static	-	70	100	
			With 50 kHz ±100 mV overdrive square signal	-	75	-	
I_{bias}	Comparator input bias current	-		-	-	-(4)	nA

1. Guaranteed by design, unless otherwise specified.
2. Refer to *Table 32: Embedded internal voltage reference*.
3. Guaranteed by characterization results.
4. Mostly I/O leakage when used in analog mode. Refer to I_{lkg} parameter in *Table 102: I/O static characteristics*.

5.3.23 Operational amplifiers characteristics

Table 119. OPAMP characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	1.8	-	3.6	V
CMIR	Common mode input range	-	0	-	V_{DDA}	V
VI_{OFFSET}	Input offset voltage	25 °C, No Load on output.	-	-	±1.5	mV
		All voltage/Temp.	-	-	±3	
ΔVI_{OFFSET}	Input offset voltage drift	Normal mode	-	±5	-	µV/°C
		Low-power mode	-	±10	-	
TRIMOFFSETP TRIMLPOFFSETP	Offset trim step at low common input voltage (0.1 x V_{DDA})	-	-	0.8	1.1	mV
TRIMOFFSETN TRIMLPOFFSETN	Offset trim step at high common input voltage (0.9 x V_{DDA})	-	-	1	1.35	

Table 119. OPAMP characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{LOAD}	Drive current	Normal mode	$V_{DDA} \geq 2$ V	-	-	500	µA
		Low-power mode		-	-	100	
I_{LOAD_PGA}	Drive current in PGA mode	Normal mode	$V_{DDA} \geq 2$ V	-	-	450	
		Low-power mode		-	-	50	
R_{LOAD}	Resistive load (connected to VSSA or to VDDA)	Normal mode	$V_{DDA} < 2$ V	4	-	-	kΩ
		Low-power mode		20	-	-	
R_{LOAD_PGA}	Resistive load in PGA mode (connected to VSSA or to V_{DDA})	Normal mode	$V_{DDA} < 2$ V	4.5	-	-	
		Low-power mode		40	-	-	
C_{LOAD}	Capacitive load	-		-	-	50	pF
CMRR	Common mode rejection ratio	Normal mode		-	-85	-	dB
		Low-power mode		-	-90	-	
PSRR	Power supply rejection ratio	Normal mode	$C_{LOAD} \leq 50$ pf, $R_{LOAD} \geq 4$ kΩ DC	70	85	-	dB
		Low-power mode	$C_{LOAD} \leq 50$ pf, $R_{LOAD} \geq 20$ kΩ DC	72	90	-	
GBW	Gain Bandwidth Product	Normal mode	$V_{DDA} \geq 2.4$ V (OPA_RANGE = 1)	550	1600	2200	kHz
		Low-power mode		100	420	600	
		Normal mode	$V_{DDA} < 2.4$ V (OPA_RANGE = 0)	250	700	950	
		Low-power mode		40	180	280	
SR(2)	Slew rate (from 10 and 90% of output voltage)	Normal mode	$V_{DDA} \geq 2.4$ V	-	700	-	V/ms
		Low-power mode		-	180	-	
		Normal mode	$V_{DDA} < 2.4$ V	-	300	-	
		Low-power mode		-	80	-	
AO	Open loop gain	Normal mode		55	110	-	dB
		Low-power mode		45	110	-	
V_{OHSAT}(2)	High saturation voltage	Normal mode	I_{load} = max or R_{load} = min Input at V_{DDA}.	V_{DDA} - 100	-	-	mV
		Low-power mode		V_{DDA} - 50	-	-	
V_{OLSAT}(2)	Low saturation voltage	Normal mode	I_{load} = max or R_{load} = min Input at 0.	-	-	100	
		Low-power mode		-	-	50	
φ_m	Phase margin	Normal mode		-	74	-	°
		Low-power mode		-	66	-	

Table 119. OPAMP characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
GM	Gain margin	Normal mode		-	13	-	dB
		Low-power mode		-	20	-	
t_{WAKEUP}	Wake up time from OFF state.	Normal mode	C_{LOAD} ≤ 50 pf, R_{LOAD} ≥ 4 kΩ follower configuration	-	5	10	µs
		Low-power mode	C_{LOAD} ≤ 50 pf, R_{LOAD} ≥ 20 kΩ follower configuration	-	10	30	
I_{bias}	OPAMP input bias current	General purpose input (all packages except UFBGA132)		-	-	(3)	nA
		Dedicated input (UFBGA132)	T_J ≤ 75 °C	-	-	1	
			T_J ≤ 85 °C	-	-	3	
			T_J ≤ 105 °C	-	-	8	
			T_J ≤ 125 °C	-	-	15	
PGA gain(2)	Non inverting gain value	-		-	2	-	-
				-	4	-	
				-	8	-	
				-	16	-	
$R_{network}$	R2/R1 internal resistance values in PGA mode(4)	PGA Gain = 2		-	80/80	-	kΩ/kΩ
		PGA Gain = 4		-	120/ 40	-	
		PGA Gain = 8		-	140/ 20	-	
		PGA Gain = 16		-	150/ 10	-	
Delta R	Resistance variation (R1 or R2)	-		-15	-	15	%
PGA gain error	PGA gain error	-		-1	-	1	%
PGA BW	PGA bandwidth for different non inverting gain	Gain = 2	-	-	GBW/ 2	-	MHz
		Gain = 4	-	-	GBW/ 4	-	
		Gain = 8	-	-	GBW/ 8	-	
		Gain = 16	-	-	GBW/ 16	-	

Table 119. OPAMP characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
en	Voltage noise density	Normal mode	at 1 kHz, Output loaded with 4 kΩ	-	500	-	nV/√Hz
		Low-power mode	at 1 kHz, Output loaded with 20 kΩ	-	600	-	
		Normal mode	at 10 kHz, Output loaded with 4 kΩ	-	180	-	
		Low-power mode	at 10 kHz, Output loaded with 20 kΩ	-	290	-	
I_{DDA}(OPAMP)(2)	OPAMP consumption from V_{DDA}	Normal mode	no Load, quiescent mode	-	120	260	µA
		Low-power mode		-	45	100	

1. Guaranteed by design, unless otherwise specified.
2. Guaranteed by characterization results.
3. Mostly I/O leakage, when used in analog mode. Refer to I_{lkg} parameter in *Table 102: I/O static characteristics*.
4. R2 is the internal resistance between OPAMP output and OPAMP inverting input. R1 is the internal resistance between OPAMP inverting input and ground. The PGA gain =1+R2/R1

5.3.24 Temperature sensor characteristics

Table 120. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L[1]	V_{TS} linearity with temperature	-	±1	±2	°C
Avg_Slope[2]	Average slope	2.3	2.5	2.7	mV/°C
V_{30}	Voltage at 30°C (±5 °C)[3]	0.742	0.76	0.785	V
t_{START} (TS_BUF)[1]	Sensor Buffer Start-up time in continuous mode[4]	-	8	15	µs
t_{START}[1]	Start-up time when entering in continuous mode[4]	-	70	120	µs
t_{S_temp}[1]	ADC sampling time when reading the temperature	5	-	-	µs
I_{DD}(TS)[1]	Temperature sensor consumption from V_{DD}, when selected by ADC	-	4.7	7	µA

1. Guaranteed by design.
2. Guaranteed by characterization results.
3. Measured at V_{DDA} = 3.0 V ±10 mV. The V_{30} ADC conversion result is stored in the TS_CAL1 byte. Refer to *Table 14: Temperature sensor calibration values*.
4. Continuous mode means Run/Sleep modes, or temperature sensor enable in Low-power run/Low-power sleep modes.

5.3.25 V_{BAT} monitoring characteristics

Table 121. V_{BAT} monitoring characteristics[1]

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	39	-	kΩ
Q	Ratio on V_{BAT} measurement	-	3	-	-
Er[2]	Error on Q	-10	-	10	%
t_{S_vbat}[2]	ADC sampling time when reading the VBAT	12	-	-	µs

1. 1.55 V < V_{BAT} < 3.6 V
2. Guaranteed by design.

Table 122. V_{BAT} charging characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{BC}	Battery charging resistor	VBRS = 0	-	5	-	kΩ
		VBRS = 1	-	1.5	-	

5.3.26 Temperature and V_{DD} thresholds monitoring

Temperature and upper V_{DD} voltage monitoring characteristics for tamper detection are detailed in the table below:

Table 123. Temp and V_{DD} monitoring characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$TEMP_{high}$	High temperature threshold monitoring	-	115	123(1)	130	°C
$TEMP_{low}$	Low temperature threshold monitoring	-	-45	-36(1)	-30	
VDD_{high}	High VDD supply monitoring	-	3.6	3.65(1)	3.7	V
$TPWM_{on}$	Minimum PWM ON time in case of periodic monitoring	-	-	400(2)	-	µs

1. Guaranteed by characterization results.
2. Guaranteed by design.

5.3.27 DFSDM characteristics

Unless otherwise specified, the parameters given in *Table 124* for DFSDM are derived from tests performed under the ambient temperature, f_{APB2} frequency and V_{DD} supply voltage conditions summarized in *Table 27: General operating conditions*.

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 x V_{DD}

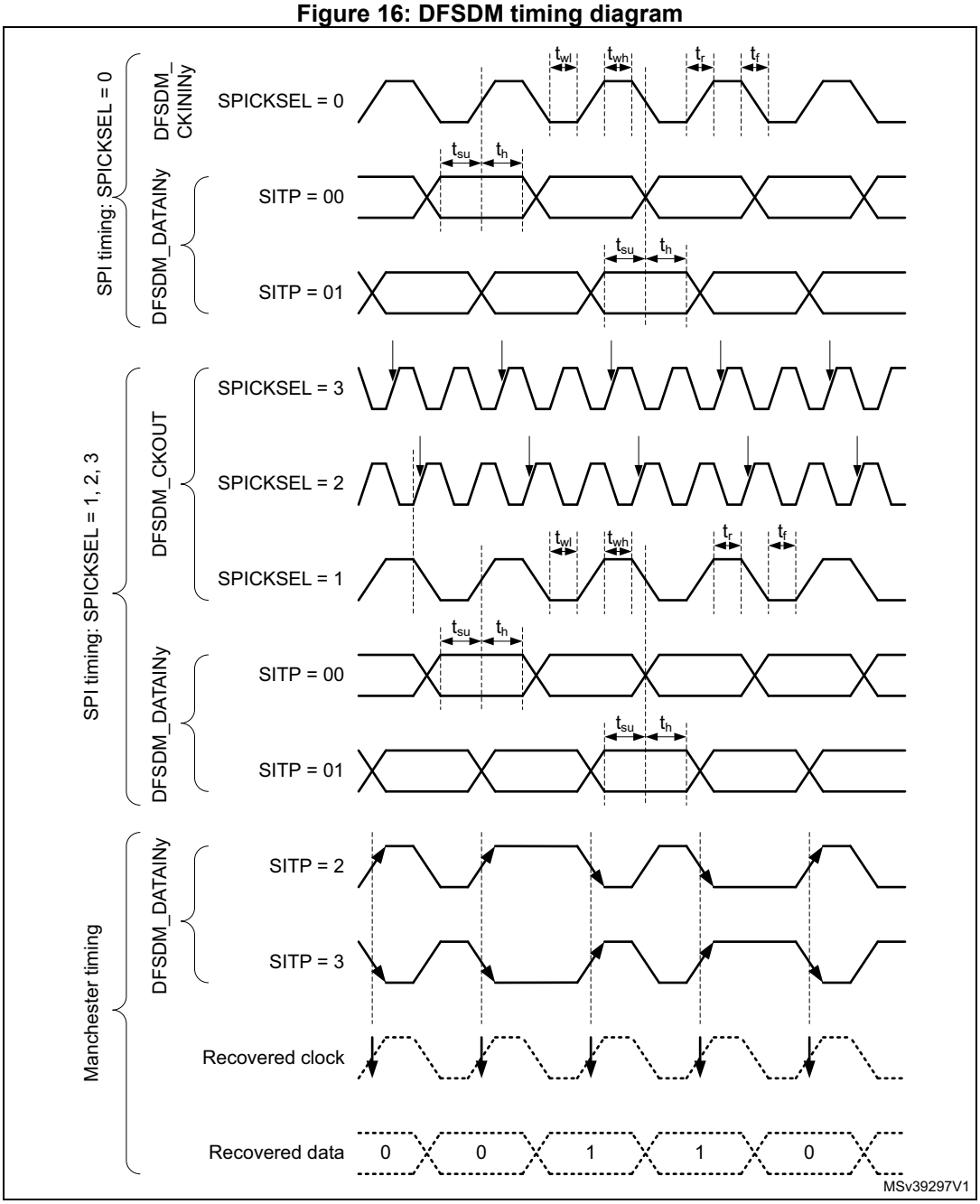
Refer to *Section 5.3.15: I/O port characteristics* for more details on the input/output alternate function characteristics (DFSDM1_CKINy, DFSDM1_DATINy, DFSDM1_CKOUT for DFSDM).

Table 124. DFSDM measured timing 1.71 to 3.6 V(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{DFSDMCLK}$	DFSDM clock	1.71 < V_{DD} < 3.6 V	-	-	f_{SYSCLK}	MHz
f_{CKIN} ($1/T_{CKIN}$)	Input clock frequency	SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0), 1.71 < V_{DD} < 3.6 V	-	-	20	
		SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0), 2.7 < V_{DD} < 3.6 V	-	-	20	
		SPI mode (SITP[1:0]=0,1), Internal clock mode (SPICKSEL[1:0]≠0), 1.71 < V_{DD} < 3.6 V	-	-	20	
		SPI mode (SITP[1:0]=0,1), Internal clock mode (SPICKSEL[1:0]≠0), 2.7 < V_{DD} < 3.6 V	-	-	20	
f_{CKOUT}	Output clock frequency	1.71 < V_{DD} < 3.6 V	-	-	20	
$DuCy_{CKOUT}$	Output clock frequency duty cycle	1.71 < V_{DD} < 3.6 V	45	50	55	%
$t_{wh(CKIN)}$ $t_{wl(CKIN)}$	Input clock high and low time	SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0), 1.71 < V_{DD} < 3.6 V	TCKIN/2-0.5	T_{CKIN}/2	-	ns
t_{su}	Data input setup time	SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0), 1.71 < V_{DD} < 3.6 V	3	-	-	
t_h	Data input hold time	SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0), 1.71 < V_{DD} < 3.6 V	2.5	-	-	
$T_{Manchester}$	Manchester data period (recovered clock period)	Manchester mode (SITP[1:0]=2,3), Internal clock mode (SPICKSEL[1:0]≠0), 1.71 < V_{DD} < 3.6 V	(CKOUTDIV +1) * $T_{DFSDMCLK}$	-	(2*CKOUTDIV) * $T_{DFSDMCLK}$	

1. Data based on characterization results, not tested in production.

Figure 16: DFSDM timing diagram



5.3.28 Timer characteristics

The parameters given in the following tables are guaranteed by design.

Refer to *Section 5.3.15: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 125. TIMx(1) characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 110 MHz	8.33	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 110 MHz	0	55	MHz
Res_{TIM}	Timer resolution	TIMx (except TIM2 and TIM5)	-	16	bit
		TIM2 and TIM5	-	32	
$t_{COUNTER}$	16-bit counter clock period	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 110 MHz	0.009	595.78	µs
t_{MAX_COUNT}	Maximum possible count with 32-bit counter	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 110 MHz	-	39.045	s

1. TIMx, is used as a general term in which x stands for 1,2,3,4,5,6,7,8,15,16 or 17.

Table 126. IWDG min/max timeout period at 32 kHz (LSI)(1)

Prescaler divider	PR[2:0] bits	Min timeout RL[11:0]= 0x000	Max timeout RL[11:0]= 0xFFF	Unit
/4	0	0.125	512	ms
/8	1	0.250	1024	
/16	2	0.500	2048	
/32	3	1.0	4096	
/64	4	2.0	8192	
/128	5	4.0	16384	
/256	6 or 7	8.0	32768	

1. The exact timings still depend on the phasing of the APB interface clock versus the LSI clock so that there is always a full RC period of uncertainty.

Table 127. WWDG min/max timeout value at 110 MHz (PCLK)

Prescaler	WDGTB	Min timeout value	Max timeout value	Unit
1	0	0.037	2.368	ms
2	1	0.074	4.736	
4	2	0.149	9.536	
8	3	0.298	19.072	

5.3.29 Communication interfaces characteristics

I²C interface characteristics

The I2C interface meets the timings requirements of the I²C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+): with a bit rate up to 1 Mbit/s.

The I2C timings requirements are guaranteed by design when the I2C peripheral is properly configured (refer to RM0351 reference manual).

The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DDIOx} is disabled, but is still present. Only FT_f I/O pins support Fm+ low level output current maximum requirement. Refer to *Section 5.3.15: I/O port characteristics* for the I2C I/Os characteristics.

All I2C SDA and SCL I/Os embed an analog filter. Refer to *Table 128* below for the analog filter characteristics:

Table 128. I2C analog filter characteristics(1)

Symbol	Parameter	Min	Max	Unit
t_{AF}	Maximum pulse width of spikes that are suppressed by the analog filter	50(2)	260(3)	ns

1. Guaranteed by design.
2. Spikes with widths below $t_{AF(min)}$ are filtered.
3. Spikes with widths above $t_{AF(max)}$ are not filtered

SPI characteristics

Unless otherwise specified, the parameters given in *Table 129* for SPI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and supply voltage conditions summarized in *Table 27: General operating conditions*.

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to *Section 5.3.15: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

Table 129. SPI characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max(2)	Unit
fSCK 1/tc(SCK)	SPI clock frequency	Master mode 2.7<VDD<3.6 Voltage ranges 0/1	-	-	55	MHz
		Master mode 1.71<VDD<3.6 Voltage ranges 0/1			44	
		Master transmitter mode 1.71<VDD<3.6 Voltage ranges 0/1			55	
		Slave receiver mode 1.71<VDD<3.6 Voltage ranges 0/1			55	
		Slave mode transmitter/full duplex 2.7<VDD<3.6 Voltage ranges 0/1			36	
		Slave mode transmitter/full duplex 1.71<VDD<3.6 Voltage ranges 0/1			23	
		Slave mode transmitter/full duplex 1.71<VDD<3.6 Voltage range 2			20	
		Slave mode transmitter/full duplex 1.08<VDD<1.32(3)			12	
tsu(NSS)	NSS setup time	Slave mode, SPI presc = 2	4×Tpclk	-	-	-
th(NSS)	NSS hold time	Slave mode, SPI presc = 2	2TTpclk	-	-	
tw(SCKH) tw(SCKL)	SCK high and low time	Master mode	Tpclk-1	Tpclk	Tpclk+1	

Table 129. SPI characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max(2)	Unit
tsu(MI)	Data input setup time	Master mode	2	-	-	ns
tsu(SI)		Slave mode	1.5	-	-	
th(MI)	Data input hold time	Master mode	7.5	-	-	
th(SI)		Slave mode	3	-	-	
ta(SO)	Data output access time	Slave mode	9	-	34	
tdis(SO)	Data output disable time	Slave mode	9	-	16	
tv(SO)	Data output valid time	Slave mode 2.7<VDD<3.6V Voltage ranges 0/1	-	9	13.75	
		Slave mode 1.71<VDD<3.6V Voltage ranges 0/1	-	9	21.5	
		Slave mode 1.71<VDD<3.6V Voltage range 2	-	11.5	24.5	
		Slave mode(3) 1.08<VDD<1.32V	-	28.5	40.5	
tv(MO)		Master mode	-	0	1	
th(SO)	Data output hold time	Slave mode 1.71<VDD<3.6V	7.5	-	-	
		Slave mode(3) 1.08<VDD<1.32V	21	-	-	
th(MO)		Master mode	0	-	-	

1. Guaranteed by characterization results.
2. Maximum frequency in Slave transmitter mode is determined by the sum of tv(SO) and tsu(MI) which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having tsu(MI) = 0 while Duty(SCK) = 50%.
3. SPI mapped on GPIOG port which is supplied by VDDIO2 specified down to 1.08 V. SPI is tested in this voltage.

Figure 48. SPI timing diagram - slave mode and CPHA = 0

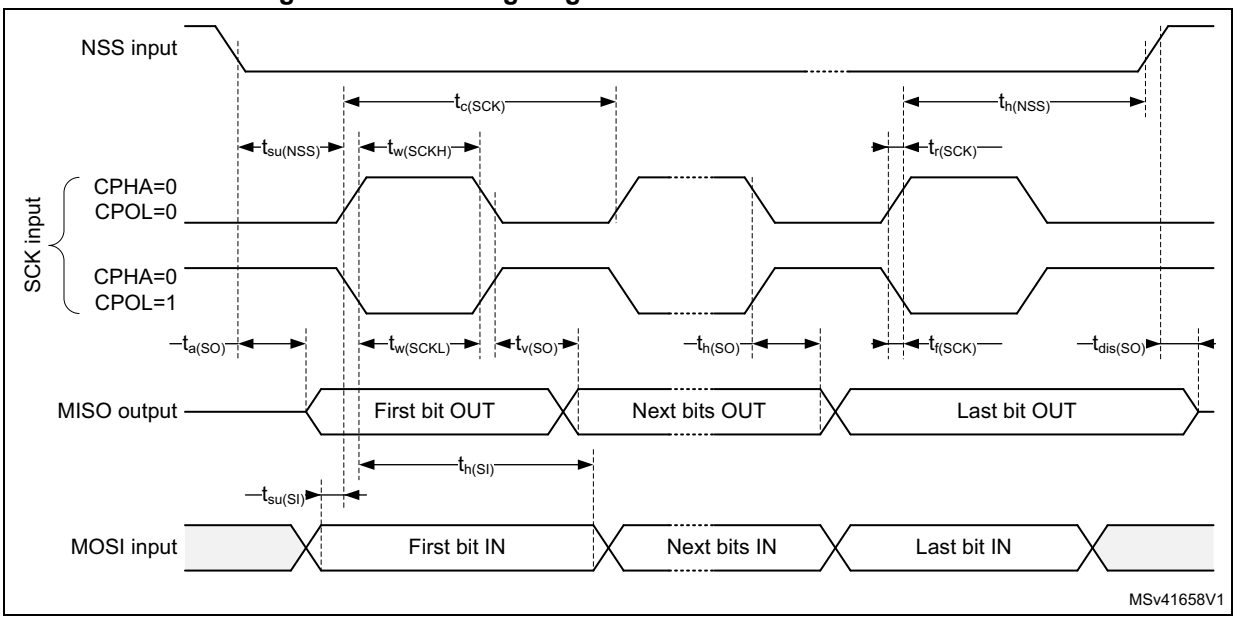
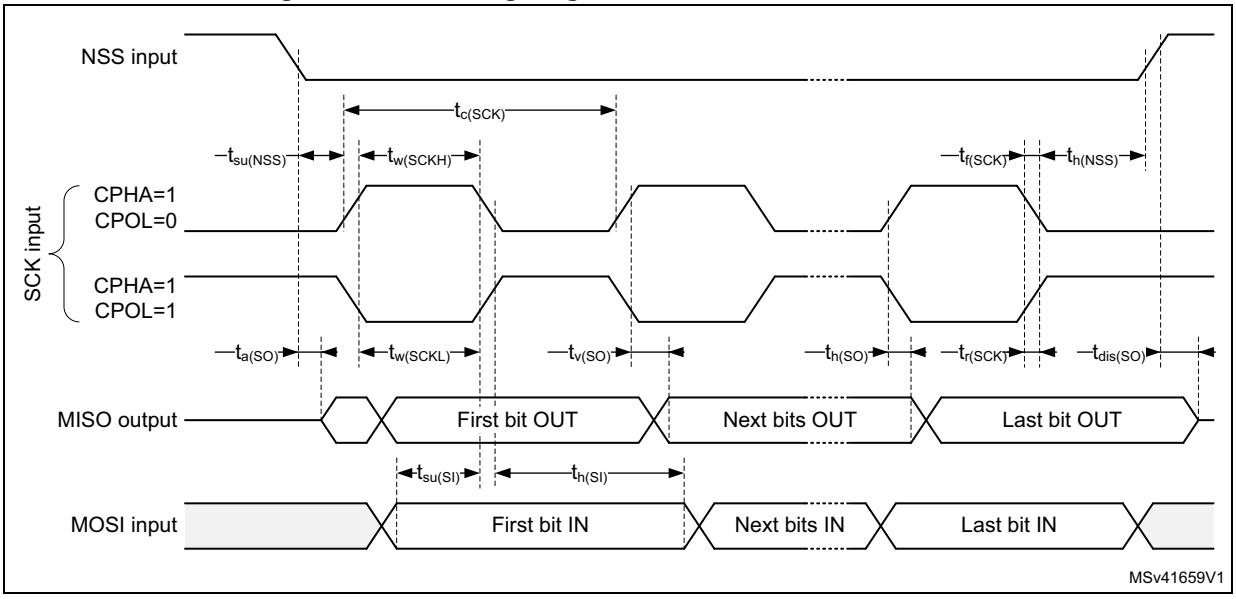
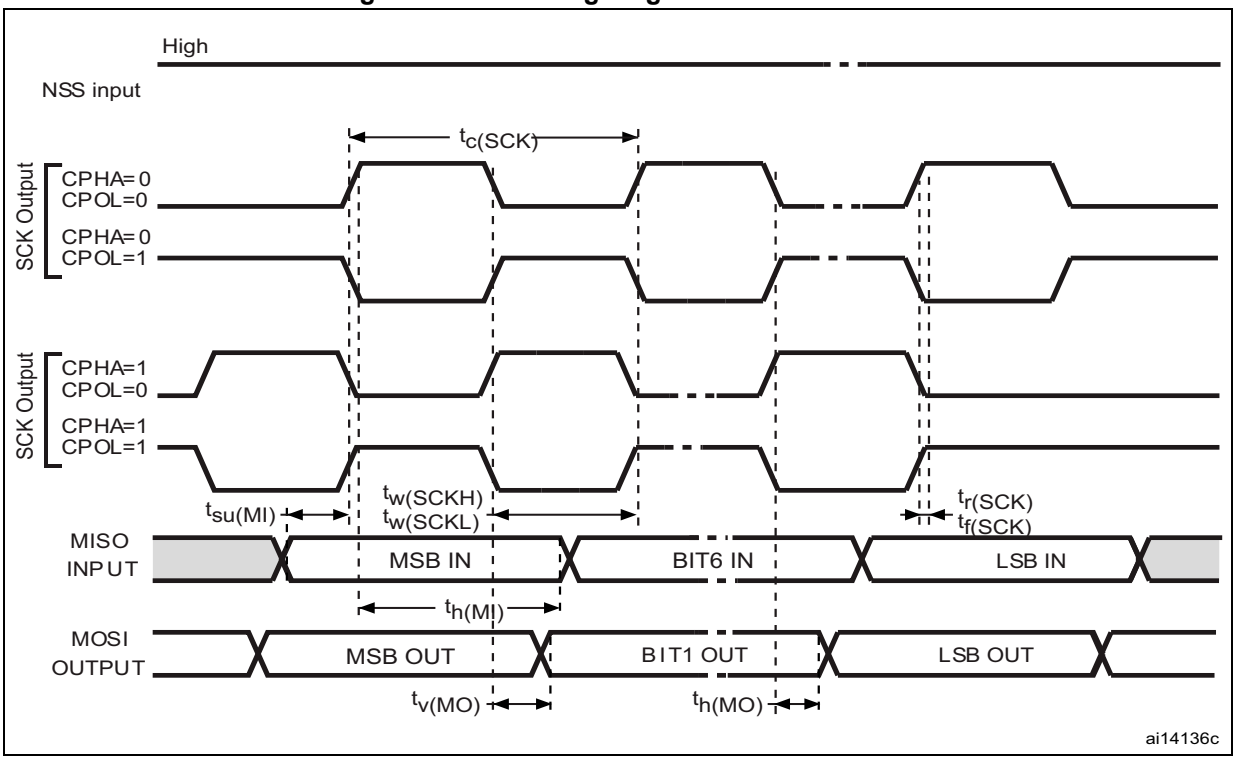


Figure 49. SPI timing diagram - slave mode and CPHA = 1



1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Figure 50. SPI timing diagram - master mode



1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

SAI characteristics

Unless otherwise specified, the parameters given in *Table 130* for SAI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 27: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to *Section 5.3.15: I/O port characteristics* for more details on the input/output alternate function characteristics (CK,SD,FS).

Table 130. SAI characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	SAI Main clock output	-	-	50	MHz
f_{CK}	SAI clock frequency(2)	Master Transmitter 2.7<=VDD<=3.6 Voltage ranges 0/1	-	23.5	
		Master Transmitter 1.71<=VDD<=3.6 Voltage ranges 0/1	-	16	
		Master Receiver Voltage ranges 0/1	-	16	
		Slave Transmitter 2.7<=VDD<=3.6 Voltage ranges 0/1	-	26	
		Slave Transmitter 1.71<=VDD<=3.6 Voltage ranges 0/1	-	20	
		Slave Receiver Voltage ranges 0/1	-	50	
		Voltage range 2	-	13	

Table 130. SAI characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{v(FS)}$	FS valid time	Master mode 2.7<=VDD<=3.6	-	21	ns
		Master mode 1.71<=VDD<=3.6	-	25	
$t_{h(FS)}$	FS hold time	Master mode	10	-	
$t_{su(FS)}$	FS setup time	Slave mode	1.5	-	
$t_{h(FS)}$	FS hold time	Slave mode	2.5	-	
$t_{su(SD\_A\_MR)}$	Data input setup time	Master receiver	1	-	
$t_{su(SD\_B\_SR)}$		Slave receiver	1.5	-	
$t_{h(SD\_A\_MR)}$	Data input hold time	Master receiver	5	-	
$t_{h(SD\_B\_SR)}$		Slave receiver	0	-	
$t_{v(SD\_B\_ST)}$	Data output valid time	Slave transmitter (after enable edge) 2.7<=VDD<=3.6	-	19	
		Slave transmitter (after enable edge) 1.71<=VDD<=3.6	-	25	
$t_{h(SD\_B\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	10	-	
$t_{v(SD\_A\_MT)}$	Data output valid time	Master transmitter (after enable edge) 2.7<=VDD<=3.6	-	17	
		Master transmitter (after enable edge) 1.71<=VDD<=3.6	-	25	
$t_{h(SD\_A\_MT)}$	Data output hold time	Master transmitter (after enable edge)	9	-	

1. Guaranteed by characterization results.
2. 2.APB clock frequency must be at least twice SAI clock frequency.

Figure 51. SAI master timing waveforms

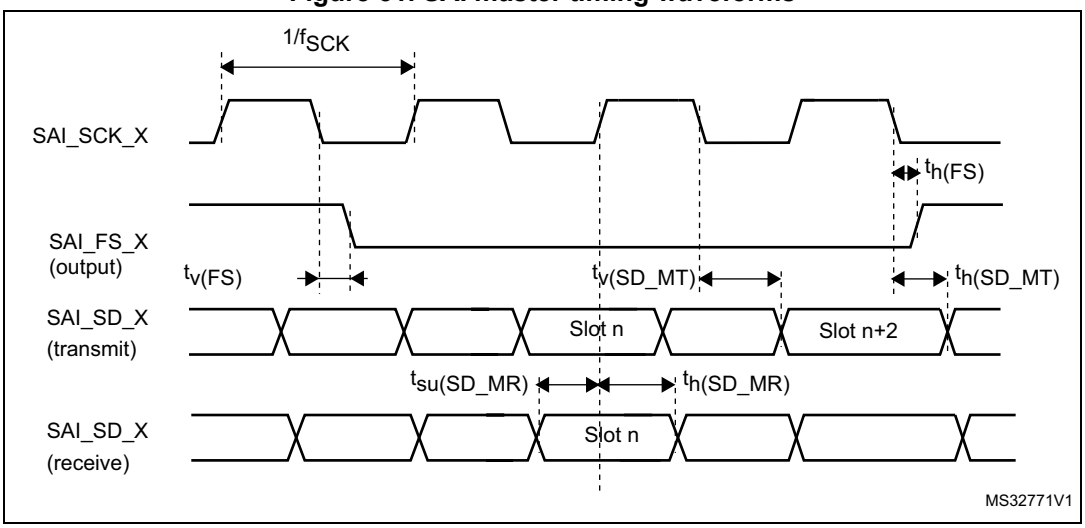
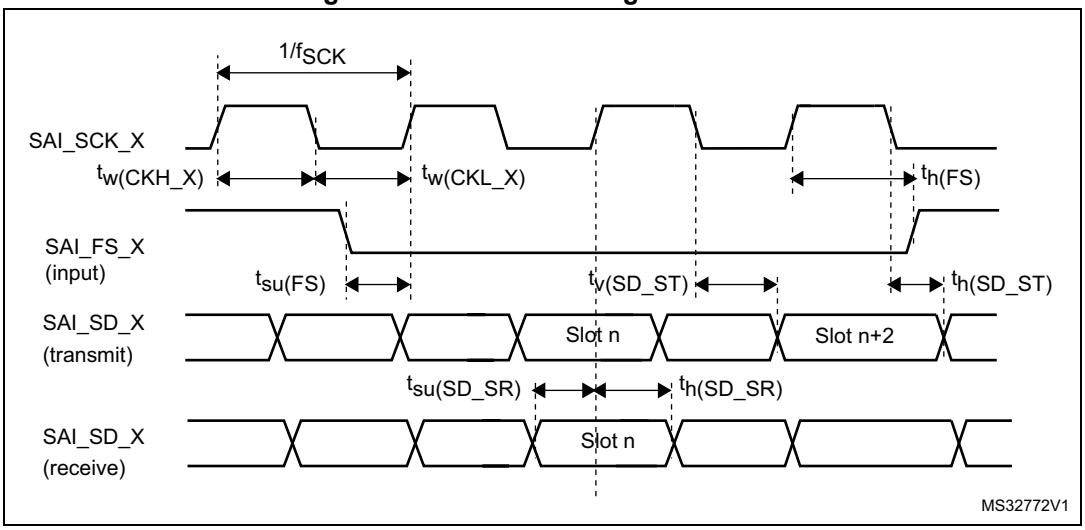


Figure 52. SAI slave timing waveforms



CAN (controller area network) interface

Refer to *Section 5.3.15: I/O port characteristics* for more details on the input/output alternate function characteristics (FDCAN_TX and FDCAN_RX).

USART characteristics

Unless otherwise specified, the parameters given in *Table 131* for USART are derived from tests performed under the ambient temperature, fPCLKx frequency and VDD supply voltage conditions summarized in *Table 27: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C=30pF
- Measurement points are done at CMOS levels: 0.5VDD

Refer to *Section 5.3.15: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, CK, TX, RX for USART).

Table 131. USART characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SPI clock frequency	Master mode 1.71<VDD<3.6	-	-	13	MHz
		Slave receiver mode 1.71<VDD<3.6	-	-	36	
		Slave mode transmitter 2.7<VDD<3.6	-	-	19	
		Slave mode transmitter 1.71<VDD<3.6	-	-	26	

Table 131. USART characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
tsu(NSS)	NSS setup time	Slave mode	Tker +4	-	-	-
th(NSS)	NSS hold time	Slave mode	1	-	-	
tw(SCKH) tw(SCKL)	SCK high and low time	Master mode	1/fsck/2-1	1/fsck/2	1/fsck/2+1	
tsu(MI)	Data input setup time	Master mode	22.5	-	-	ns
tsu(SI)		Slave mode	1	-	-	
th(MI)	Data input hold time	Master mode	0	-	-	
th(SI)		Slave mode	3	-	-	
tv(SO)	Data output valid time	Slave mode 2.7<VDD<3.6V	-	14.5	19	
		Slave mode 1.71<VDD<3.6V	-	14.5	26	
tv(MO)		Master mode	-	1.5	3	
th(SO)	Data output hold time	Slave mode 1.71<VDD<3.6V	12	-	-	
th(MO)		Master mode	1	-	-	

1. Guaranteed by characterization results, not tested in production.

Figure 53. USART master mode timing diagram

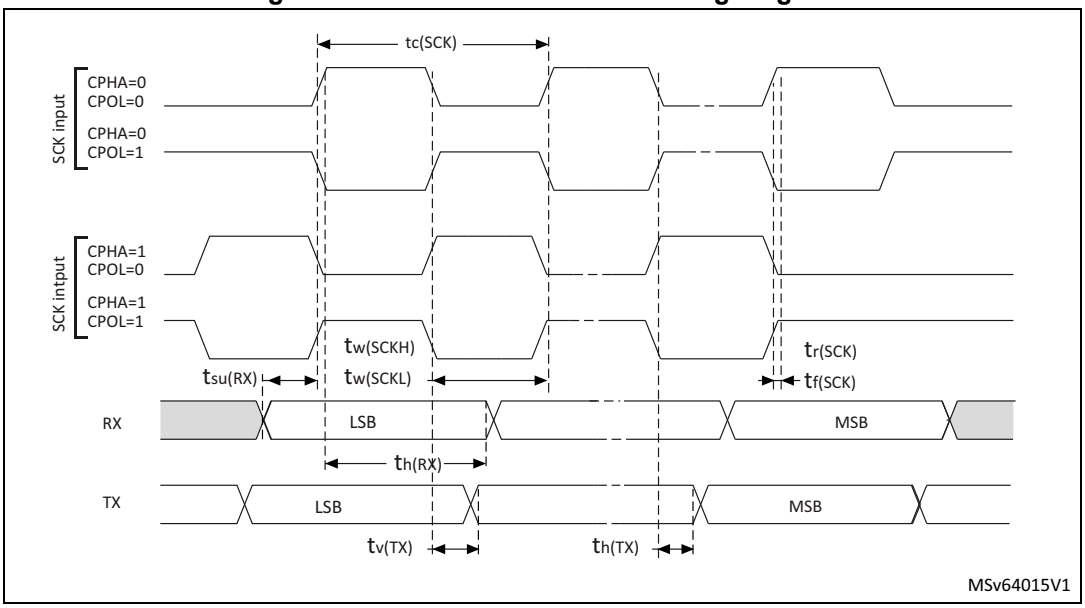
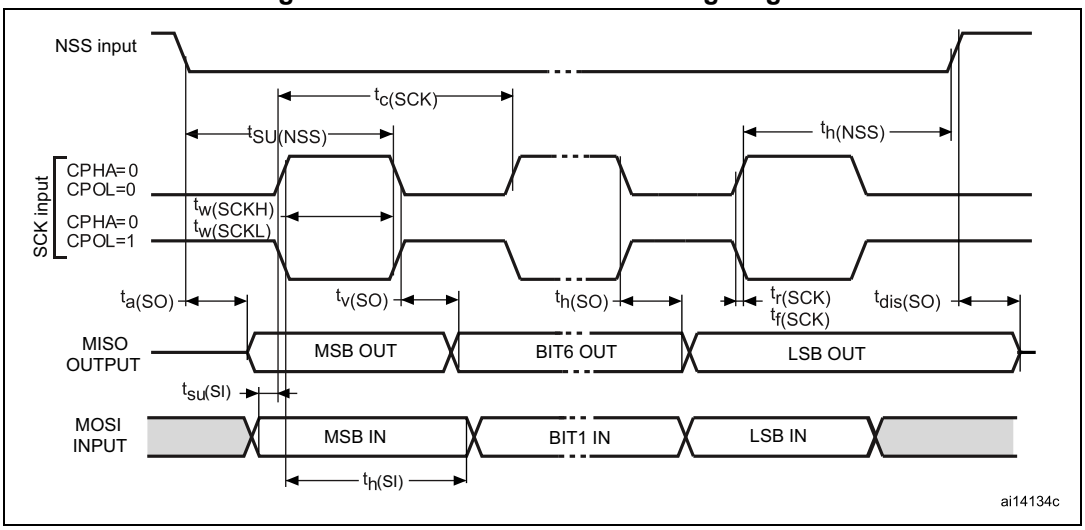


Figure 54. USART slave mode timing diagram



5.3.30 FSMC characteristics

Unless otherwise specified, the parameters given in *Table 132* to *Table 145* for the FMC interface are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage conditions summarized in *Table 27: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 x V_{DD}

Refer to *Section 5.3.15: I/O port characteristics* for more details on the input/output characteristics.

Asynchronous waveforms and timings

Figure 55 through *Figure 58* represent asynchronous waveforms and *Table 132* through *Table 139* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- AddressSetupTime (ADDSET) = 0x1
- AddressHoldTime (ADDHLD) = 0x1
- DataHoldTime = 0x1
- ByteLaneSetup (NBLSET) = 0x1
- DataSetupTime (DATAST) = 0x1 (except for asynchronous NWAIT mode, DataSetupTime = 0x5)
- DataHoldTime (DATAHLD) = 0x1 (1THCLK for read operations and 2THCLK for write operations)
- BusTurnAroundDuration = 0x0
- Capacitive load CL = 30 pF

In all timing tables, the THCLK is the HCLK clock period.

Figure 55. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms

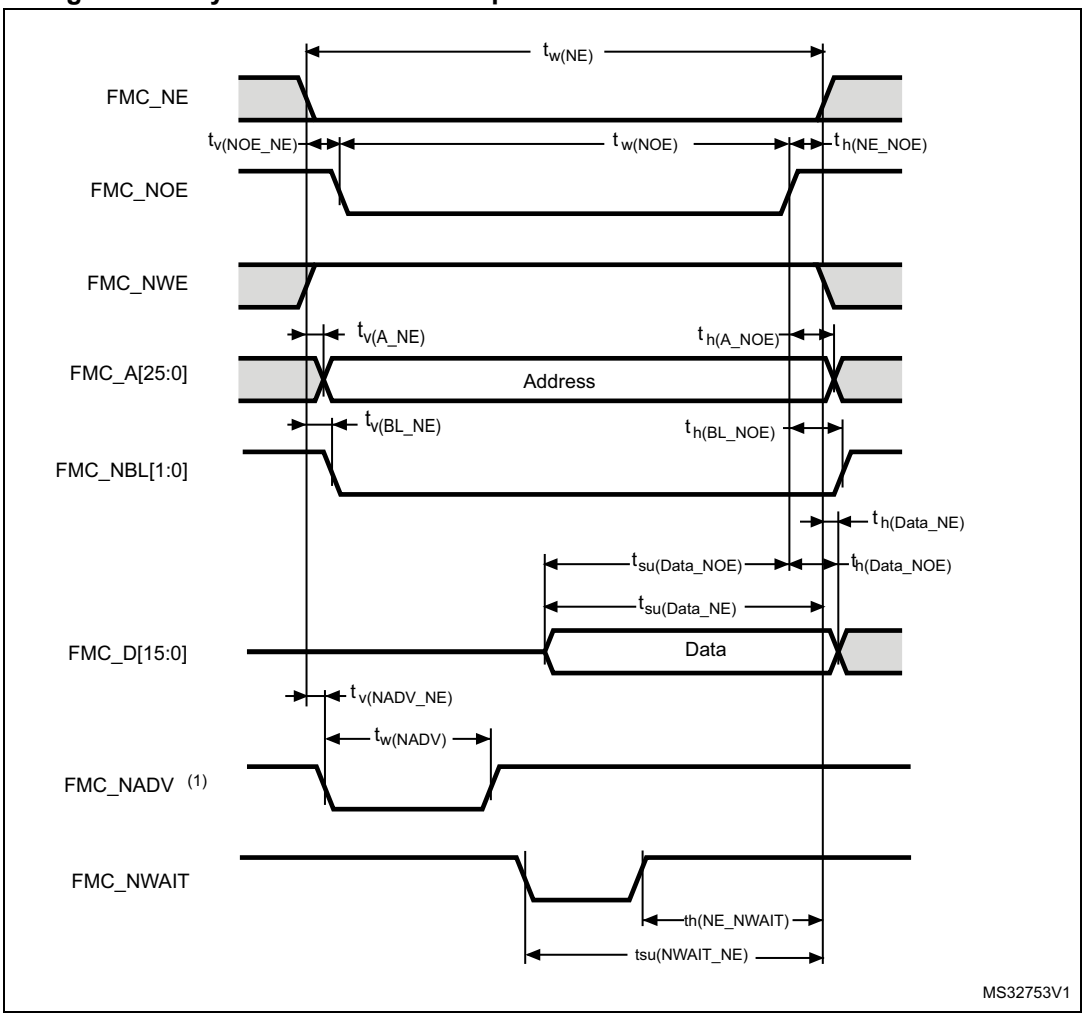


Table 132. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings(1)

Symbol	Parameter	Min	Max	Unit
tw(NE)	FMC_NE low time	3THCLK– 0.5	3 THCLK+1	ns
tv(NOE_NE)	FMC_NEx low to FMC_NOE low	0	1	
tw(NOE)	FMC_NOE low time	2THCLK -0.5	2THCLK + 1	
th(NE_NOE)	FMC_NOE high to FMC_NE high hold time	THCLK	-	
tv(A_NE)	FMC_NEx low to FMC_A valid	-	1	
th(A_NOE)	Address hold time after FMC_NOE high	2THCLK-1	-	
tsu(Data_NE)	Data to FMC_NEx high setup time	THCLK +14	-	
tsu(Data_NOE)	Data to FMC_NOEx high setup time	14	-	
th(Data_NOE)	Data hold time after FMC_NOE high	0	-	
th(Data_NE)	Data hold time after FMC_NEx high	0	-	
tv(NADV_NE)	FMC_NEx low to FMC_NADV low	-	0	
tw(NADV)	FMC_NADV low time	-	THCLK+1.5	

1. Guaranteed by characterization results, not tested in production.

Table 133. Asynchronous non-multiplexed SRAM/PSRAM/NOR read-NWAIT timings(1)

Symbol	Parameter	Min	Max	Unit
tw(NE)	FMC_NE low time	8THCLK-0.5	8THCLK+1	ns
tw(NOE)	FMC_NWE low time	7THCLK -0.5	7THCLK +0.5	
tw(NWAIT)	FMC_NWAIT low time	THCLK	-	
tsu(NWAIT_NE)	FMC_NWAIT valid before FMC_NEx high	5THCLK +12.5	-	
th(NE_NWAIT)	FMC_NEx hold time after FMC_NWAIT invalid	4THCLK+12	-	

1. Guaranteed by characterization results, not tested in production.

Figure 56. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms

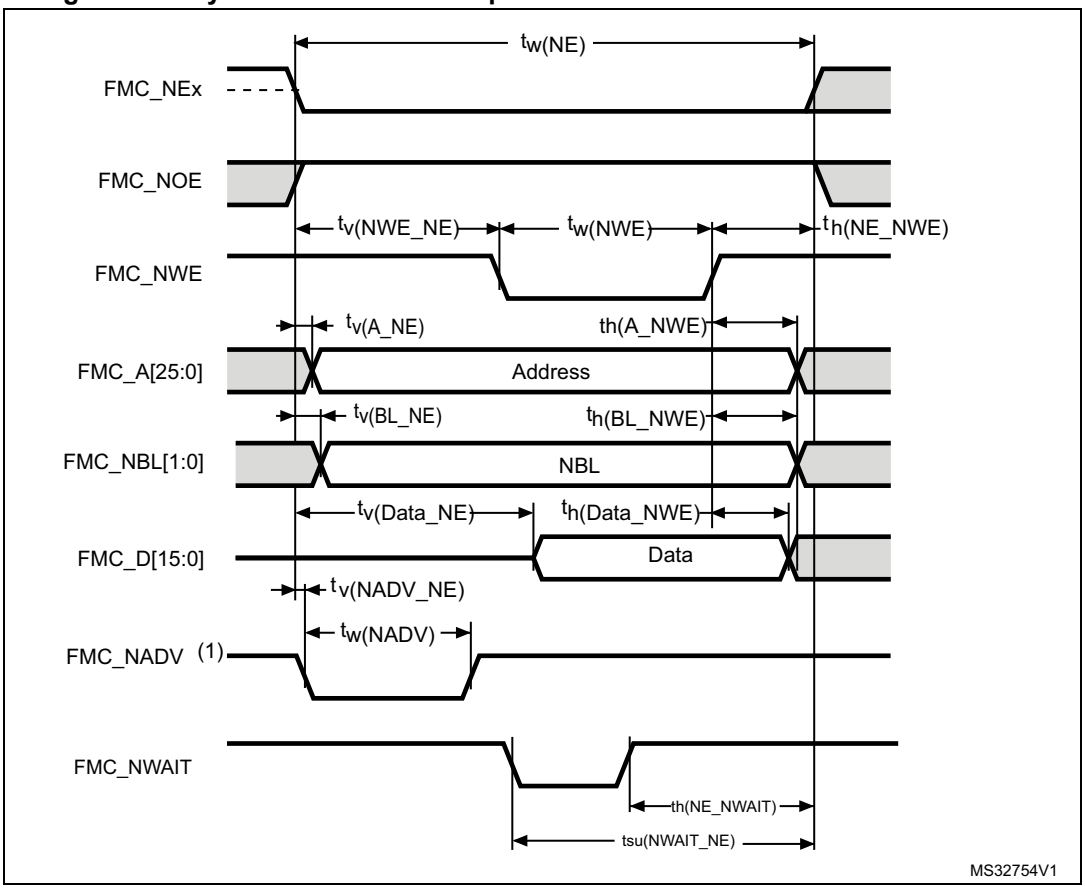


Table 134. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings(1)

Symbol	Parameter	Min	Max	Unit
tw(NE)	FMC_NE low time	4THCLK-0.5	4THCLK+1	Ns
tv(NWE_NE)	FMC_NEx low to FMC_NWE low	THCLK-0.5	THCLK +1	-
tw(NWE)	FMC_NWE low time	THCLK-0.5	THCLK+1	
th(NE_NWE)	FMC_NWE high to FMC_NE high hold time	2THCLK-0.5	-	
tv(A_NE)	FMC_NEx low to FMC_A valid	-	0	
th(A_NWE)	Address hold time after FMC_NWE high	2THCLK-1	-	
tv(BL_NE)	FMC_NEx low to FMC_BL valid	-	THCLK	
th(BL_NWE)	FMC_BL hold time after FMC_NWE high	2THCLK-0.5	-	
tv(Data_NE)	FMC_NEx low to Data valid	-	THCLK+3	
th(Data_NWE)	Data hold time after FMC_NWE high	2THCLK+1	-	
tv(NADV_NE)	FMC_NEx low to FMC_NADV low	-	1	
tw(NADV)	FMC_NADV low time	-	THCLK+ 1.5	

1. Guaranteed by characterization results, not tested in production.

Table 135. Asynchronous non-multiplexed SRAM/PSRAM/NOR write-NWAIT timings(1)

Symbol	Parameter	Min	Max	Unit
tw(NE)	FMC_NE low time	9THCLK-0.5	9THCLK+1.5	ns
tw(NWE)	FMC_NWE low time	6THCLK-0.5	6THCLK+1	
tsu(NWAIT_NE)	FMC_NWAIT valid before FMC_NEx high	7THCLK+13	-	
th(NE_NWAIT)	FMC_NEx hold time after FMC_NWAIT invalid	5THCLK+13	-	

1. Guaranteed by characterization results, not tested in production.

Figure 57. Asynchronous multiplexed PSRAM/NOR read waveforms

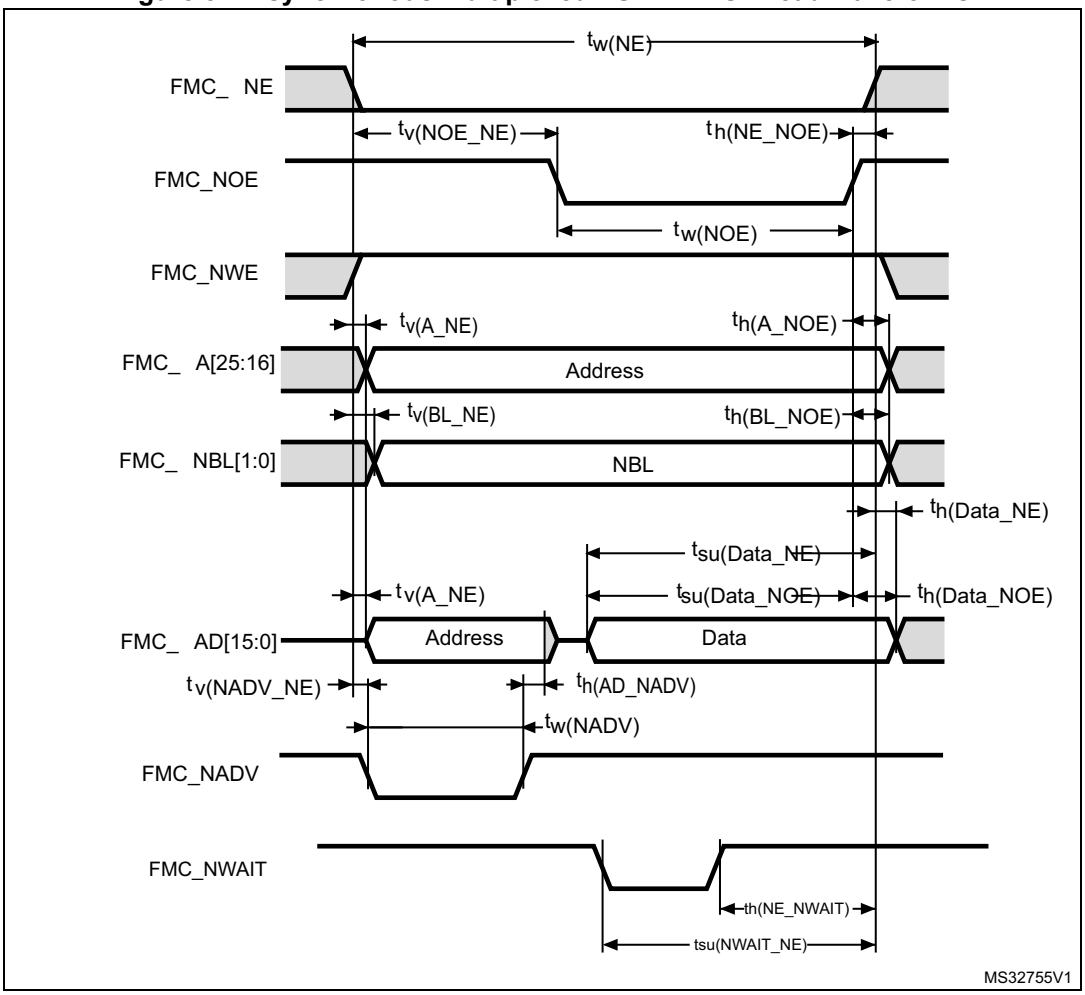


Table 136. Asynchronous multiplexed PSRAM/NOR read timings(1)

Symbol	Parameter	Min	Max	Unit
tw(NE)	FMC_NE low time	4THCLK-0.5	4THCLK +1	Ns
tv(NOE_NE)	FMC_NEx low to FMC_NOE low	2THCLK -0.5	2THCLK +1	
tw(NOE)	FMC_NOE low time	THCLK-0.5	THCLK+ 0.5	
th(NE_NOE)	FMC_NOE high to FMC_NE high hold time	THCLK-1	-	
tv(A_NE)	FMC_NEx low to FMC_A valid	-	3	
tv(NADV_NE)	FMC_NEx low to FMC_NADV low	0.5	1.5	
tw(NADV)	FMC_NADV low time	THCLK	THCLK+ 1.5	
th(AD_NADV)	FMC_AD(address) valid hold time after FMC_NADV high)	THCLK-3	-	
th(A_NOE)	Address hold time after FMC_NOE high	Address holded until next read operation	-	
tsu(Data_NE)	Data to FMC_NEx high setup time	THCLK+14	-	
tsu(Data_NOE)	Data to FMC_NOE high setup time	14	-	
th(Data_NE)	Data hold time after FMC_NEx high	0	-	
th(Data_NOE)	Data hold time after FMC_NOE high	0	-	

1. Guaranteed by characterization results, not tested in production.

Table 137. Asynchronous multiplexed PSRAM/NOR read-NWAIT timings(1)

Symbol	Parameter	Min	Max	Unit
tw(NE)	FMC_NE low time	8THCLK-0.5	9THCLK+1	Ns
tw(NOE)	FMC_NOE low time	5THCLK -0.5	6THCLK +1	
tsu(NWAIT_NE)	FMC_NWAIT valid before FMC_NEx high	5THCLK+12	-	
th(NE_NWAIT)	FMC_NEx hold time after FMC_NWAIT invalid	4THCLK+11	-	

1. Guaranteed by characterization results, not tested in production.

Figure 58. Asynchronous multiplexed PSRAM/NOR write waveforms

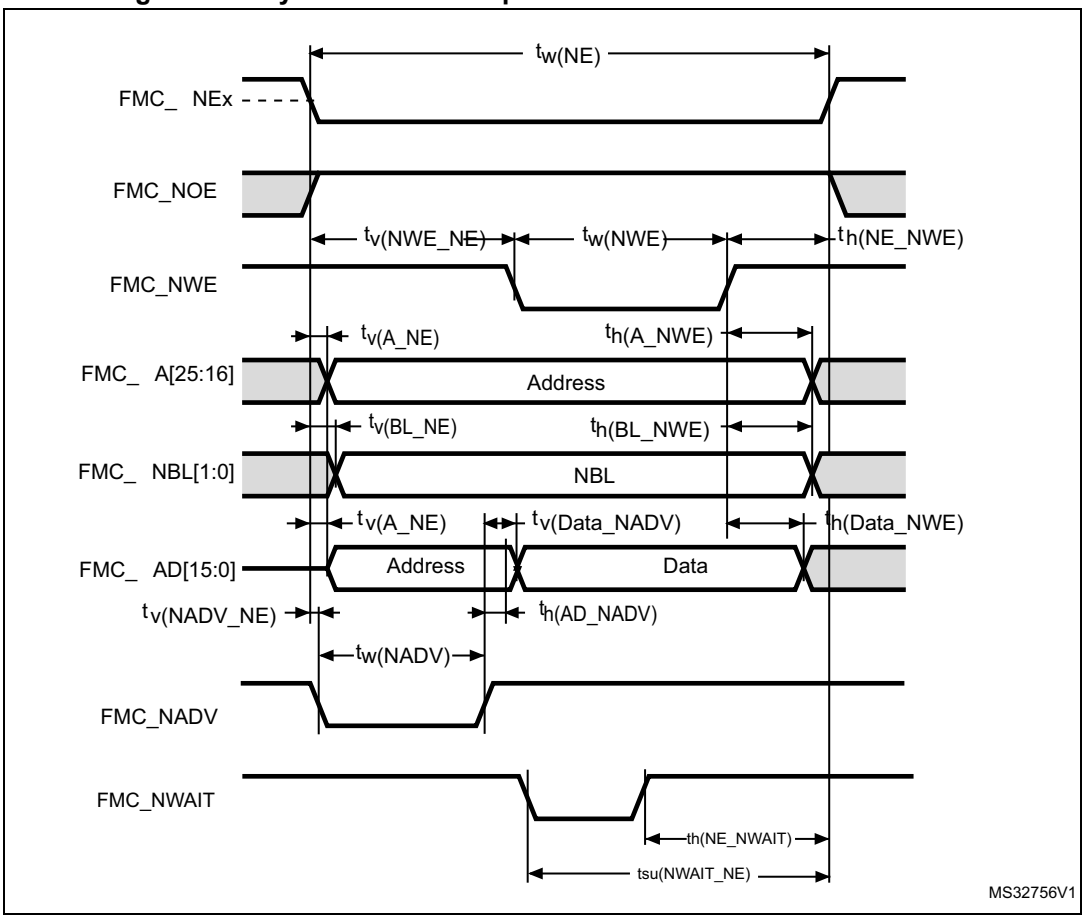


Table 138. Asynchronous multiplexed PSRAM/NOR write timings(1)

Symbol	Parameter	Min	Max	Unit
tw(NE)	FMC_NE low time	5THCLK-0.5	5THCLK+1	ns
tv(NWE_NE)	FMC_NEx low to FMC_NWE low	THCLK– 0.5	THCLK+ 1	
tw(NWE)	FMC_NWE low time	2THCLK-0.5	2THCLK+0.5	
th(NE_NWE)	FMC_NWE high to FMC_NE high hold time	2THCLK-0.5	-	
tv(A_NE)	FMC_NEx low to FMC_A valid	-	3	
tv(NADV_NE)	FMC_NEx low to FMC_NADV low	0	1	
tw(NADV)	FMC_NADV low time	THCLK+0.5	THCLK+1.5	
th(AD_NADV)	FMC_AD(adress) valid hold time after FMC_NADV high)	THCLK-3	-	
th(A_NWE)	Address hold time after FMC_NWE high	Address holded until next write operation	-	
th(BL_NWE)	FMC_BL hold time after FMC_NWE high	2THCLK-0.5	-	
tv(BL_NE)	FMC_NEx low to FMC_BL valid	-	THCLK	
tv(Data_NADV)	FMC_NADV high to Data valid	-	THCLK+2	
th(Data_NWE)	Data hold time after FMC_NWE high	2THCLK+0.5	-	

1. Guaranteed by characterization results, not tested in production.

Table 139. Asynchronous multiplexed PSRAM/NOR write-NWAIT timings(1)

Symbol	Parameter	Min	Max	Unit
tw(NE)	FMC_NE low time	10THCLK-0.5	10THCLK+1	ns
tw(NWE)	FMC_NWE low time	7THCLK-0.5	7THCLK+0.5	
tsu(NWAIT_NE)	FMC_NWAIT valid before FMC_NEx high	7THCLK+11.5	-	
th(NE_NWAIT)	FMC_NEx hold time after FMC_NWAIT invalid	5THCLK+12.5	-	

1. Guaranteed by characterization results, not tested in production.

Synchronous waveforms and timings

Figure 59 through *Figure 62* represent synchronous waveforms and *Table 140* through *Table 143* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- BurstAccessMode = FMC_BurstAccessMode_Enable
- MemoryType = FMC_MemoryType_CRAM
- WriteBurst = FMC_WriteBurst_Enable
- CLKDivision = 1
- DataLatency = 1 for NOR Flash; DataLatency = 0 for PSRAM

In all timing tables, the T_{HCLK} is the HCLK clock period.

- Maximum FMC_CLK =55MHz for CLKDIV=0x1 and 42MHz CLKDIV=0x0 for 2.7V<VDD<3.6V
- Maximum FMC_CLK =55MHz for CLKDIV=0x1 and 26MHz CLKDIV=0x0 for 1.71V<VDD<1.9V with CL=20pF

Figure 59. Synchronous multiplexed NOR/PSRAM read timings

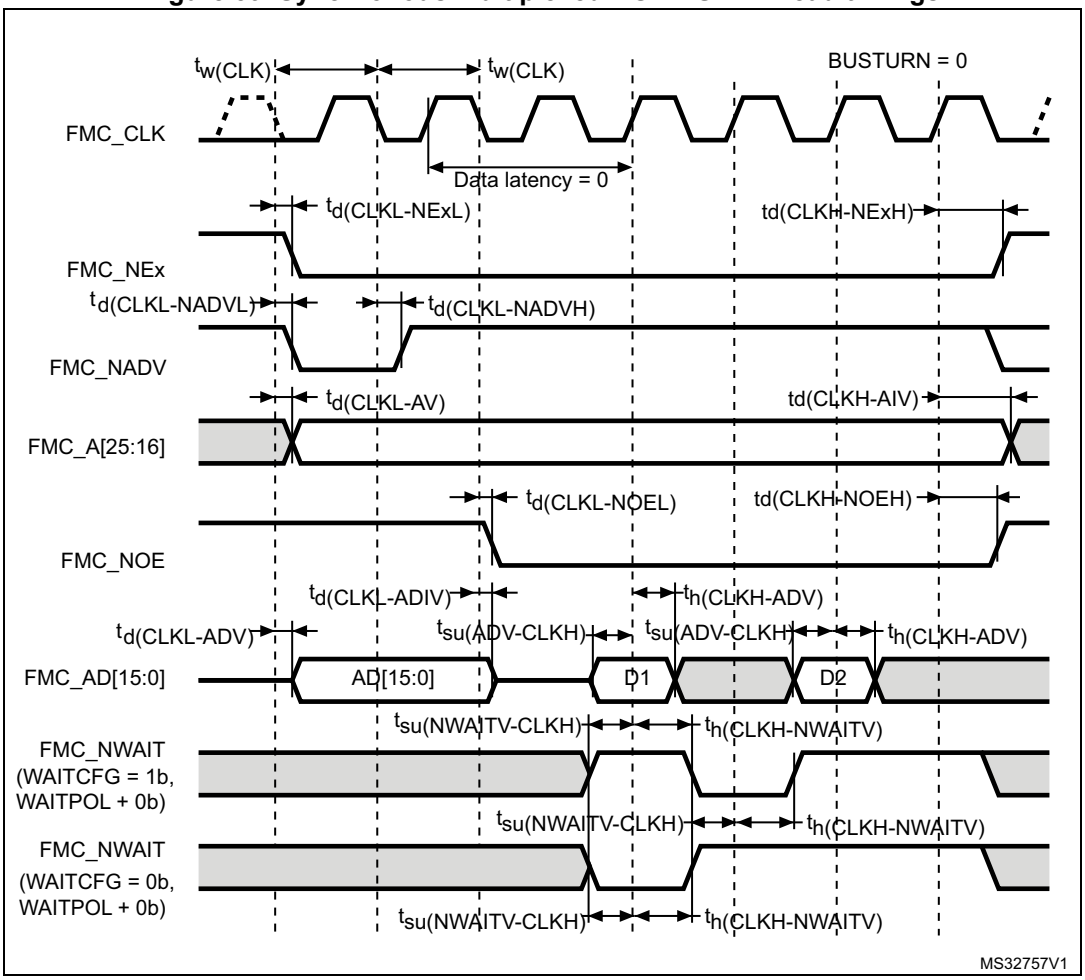


Table 140. Synchronous multiplexed NOR/PSRAM read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
tw(CLK)	FMC_CLK period	R*THCLK-0.5(2))	-	ns
td(CLKL-NExL)	FMC_CLK low to FMC_NEx low (x=0..2)	-	2.5	
td(CLKH_NExH)	FMC_CLK high to FMC_NEx high (x= 0…2)	R*THCLK/2+1(2)	-	
td(CLKL-NADVL)	FMC_CLK low to FMC_NADV low	-	2.5	
td(CLKL-NADVH)	FMC_CLK low to FMC_NADV high	2	-	
td(CLKL-AV)	FMC_CLK low to FMC_Ax valid (x=16…25)	-	5.5	
td(CLKH-AIV)	FMC_CLK high to FMC_Ax invalid (x=16…25)	R*THCLK/2 + 1(2)	-	
td(CLKL-NOEL)	FMC_CLK low to FMC_NOE low	-	2	
td(CLKH-NOEH)	FMC_CLK high to FMC_NOE high	R*THCLK/2+1(2)	-	
td(CLKL-ADV)	FMC_CLK low to FMC_AD[15:0] valid	-	3	
td(CLKL-ADIV)	FMC_CLK low to FMC_AD[15:0] invalid	0	-	
tsu(ADV-CLKH)	FMC_A/D[15:0] valid data before FMC_CLK high	2	-	
th(CLKH-ADV)	FMC_A/D[15:0] valid data after FMC_CLK high	4	-	
tsu(NWAIT-CLKH)	FMC_NWAIT valid before FMC_CLK high	1.5	-	
th(CLKH-NWAIT)	FMC_NWAIT valid after FMC_CLK high	4	-	

1. Guaranteed by characterization results, not tested in production.
2. Clock ratio R = (HCLK period /FMC_CLK period).

Figure 60. Synchronous multiplexed PSRAM write timings

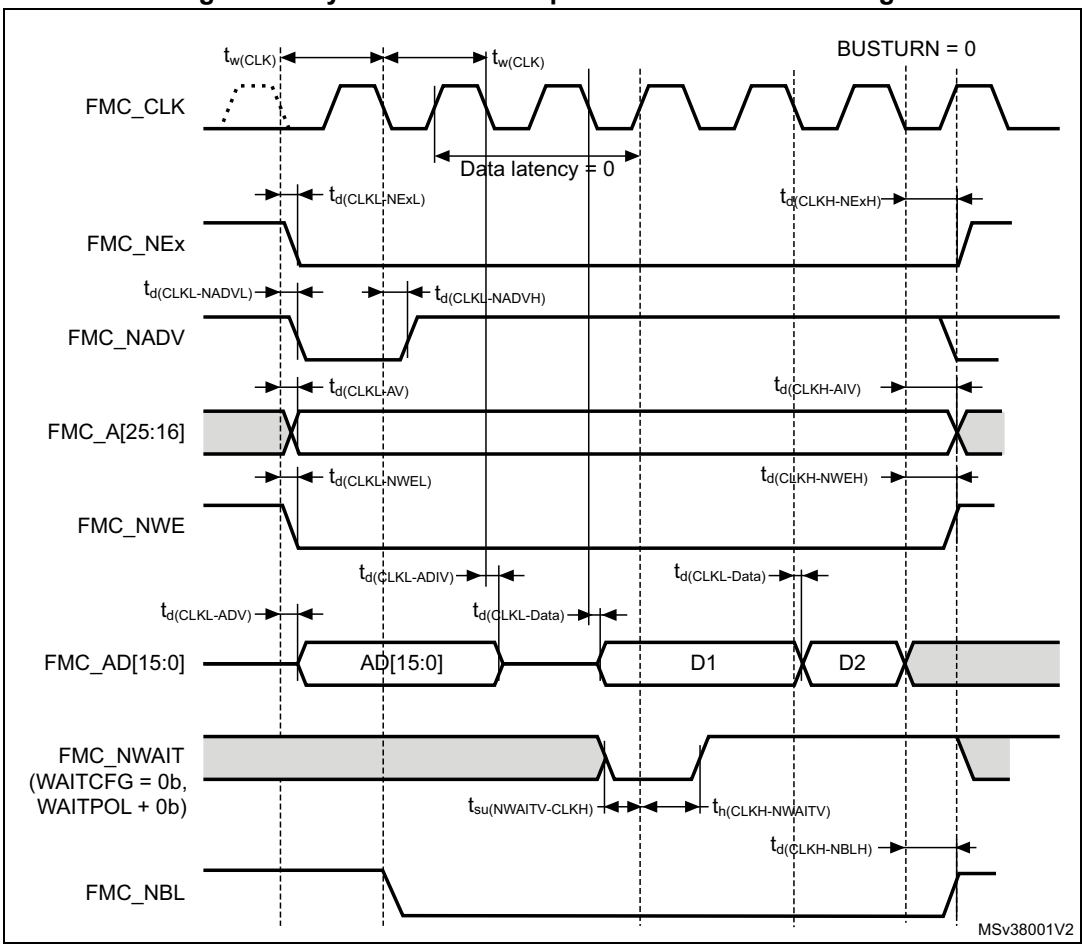


Table 141. Synchronous multiplexed PSRAM write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
tw(CLK)	FMC_CLK period, VDD range= 2.7 to 3.6 V	R*THCLK-0.5(2)	-	ns
td(CLKL-NExL)	FMC_CLK low to FMC_NEx low (x=0..2)	-	2.5	
td(CLKH-NExH)	FMC_CLK high to FMC_NEx high (x= 0…2)	R*THCLK/2+1(2)	-	
td(CLKL-NADVL)	FMC_CLK low to FMC_NADV low	-	2.5	
td(CLKL-NADVH)	FMC_CLK low to FMC_NADV high	2	-	
td(CLKL-AV)	FMC_CLK low to FMC_Ax valid (x=16…25)	-	5.75	
td(CLKH-AIV)	FMC_CLK high to FMC_Ax invalid (x=16…25)	R*THCLK/2+1(2)	-	
td(CLKL-NWEL)	FMC_CLK low to FMC_NWE low	-	2	
td(CLKH-NWEH)	FMC_CLK high to FMC_NWE high	R*THCLK/2+1(2)	-	
td(CLKL-ADV)	FMC_CLK low to to FMC_AD[15:0] valid	-	3	
td(CLKL-ADIV)	FMC_CLK low to FMC_AD[15:0] invalid	0	-	
td(CLKL-DATA)	FMC_A/D[15:0] valid data after FMC_CLK low	-	3.5	
td(CLKL-NBLL)	FMC_CLK low to FMC_NBL low	1	-	
td(CLKH-NBLH)	FMC_CLK high to FMC_NBL high	R*THCLK/2+1.5(2)	-	
tsu(NWAIT-CLKH)	FMC_NWAIT valid before FMC_CLK high	1.5	-	
th(CLKH-NWAIT)	FMC_NWAIT valid after FMC_CLK high	4	-	

1. Guaranteed by characterization results, not tested in production.
2. Clock ratio R = (HCLK period /FMC_CLK period).

Figure 61. Synchronous non-multiplexed NOR/PSRAM read timings

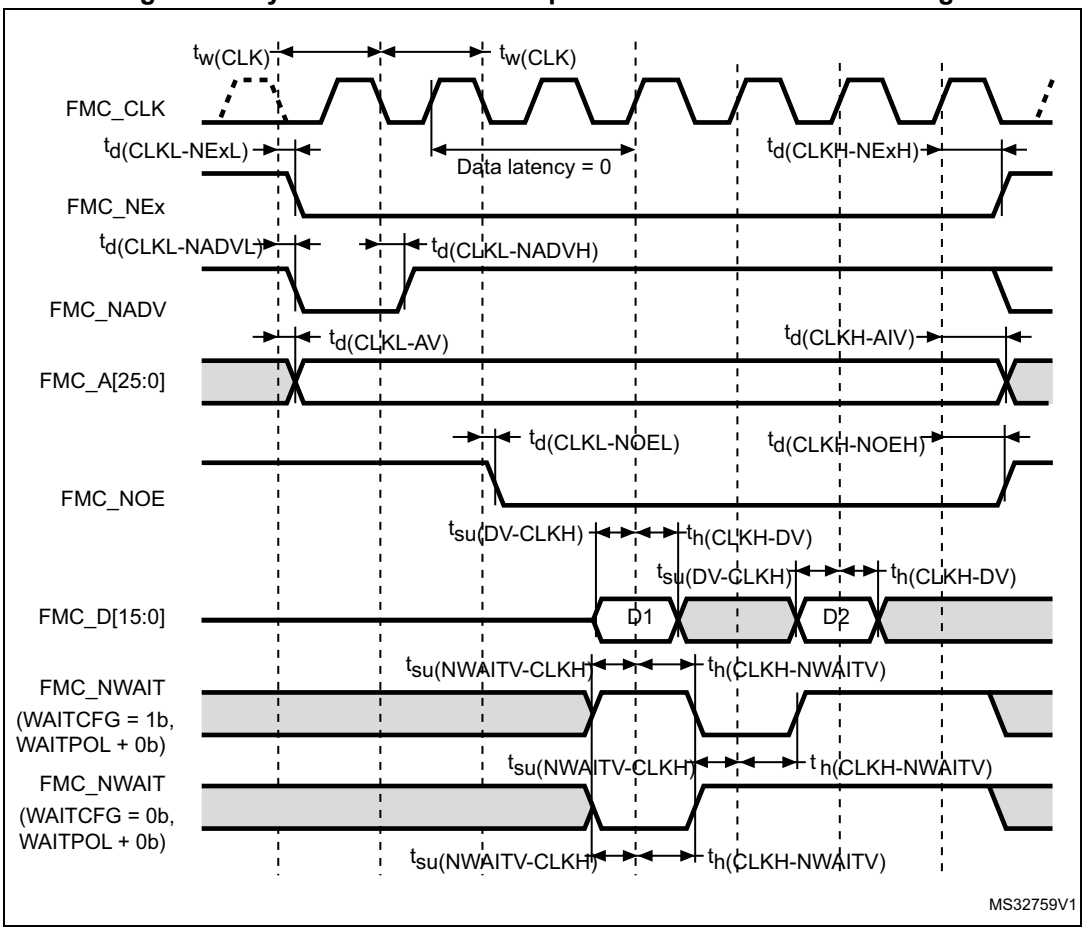


Table 142. Synchronous non-multiplexed NOR/PSRAM read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
tw(CLK)	FMC_CLK period	R*THCLK-0.5(2)	-	ns
td(CLKL-NExL)	FMC_CLK low to FMC_NEx low (x=0..2)	-	2.5	
td(CLKH-NExH)	FMC_CLK high to FMC_NEx high (x= 0…2)	R*THCLK/2+1(2)	-	
td(CLKL-NADVL)	FMC_CLK low to FMC_NADV low	-	2.5	
td(CLKL-NADVH)	FMC_CLK low to FMC_NADV high	2	-	
td(CLKL-AV)	FMC_CLK low to FMC_Ax valid (x=0…25)	-	5.5	
td(CLKH-AIV)	FMC_CLK high to FMC_Ax invalid (x=0…25)	R*THCLK/2+0.5(2)	-	
td(CLKL-NOEL)	FMC_CLK low to FMC_NOE low	-	2	
td(CLKH-NOEH)	FMC_CLK high to FMC_NOE high	R*THCLK/2+1(2)	-	
tsu(DV-CLKH)	FMC_D[15:0] valid data before FMC_CLK high	2	-	
th(CLKH-DV)	FMC_D[15:0] valid data after FMC_CLK high	4	-	
tsu(NWAIT-CLKH)	FMC_NWAIT valid before FMC_CLK high	1.5	-	
th(CLKH-NWAIT)	FMC_NWAIT valid after FMC_CLK high	4	-	

1. Guaranteed by characterization results, not tested in production.
2. Clock ratio R = (HCLK period /FMC_CLK period).

Figure 62. Synchronous non-multiplexed PSRAM write timings

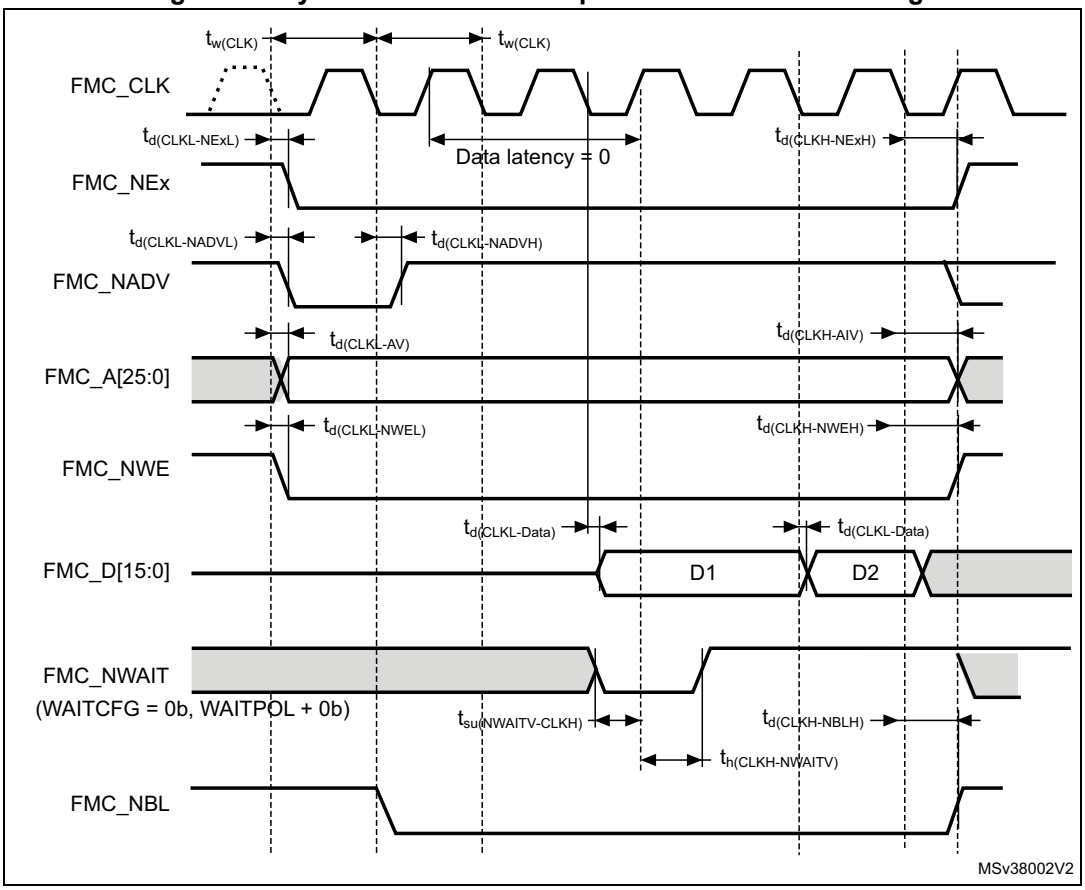


Table 143. Synchronous non-multiplexed PSRAM write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
tw(CLK)	FMC_CLK period	R*THCLK-0.5(2)	-	ns
td(CLKL-NExL)	FMC_CLK low to FMC_NEx low (x=0..2)	-	2.5	
td(CLKH-NExH)	FMC_CLK high to FMC_NEx high (x= 0…2)	R*THCLK/2 +1(2)	-	
td(CLKL-NADVL)	FMC_CLK low to FMC_NADV low	-	2.5	
td(CLKL-NADVH)	FMC_CLK low to FMC_NADV high	2	-	
td(CLKL-AV)	FMC_CLK low to FMC_Ax valid (x=0…25)	-	5.5	
td(CLKH-AIV)	FMC_CLK high to FMC_Ax invalid (x=0…25)	R*THCLK/2+0.5(2)	-	
td(CLKL-NWEL)	FMC_CLK low to FMC_NWE low	-	2	
td(CLKH-NWEH)	FMC_CLK high to FMC_NWE high	R*THCLK/2+1(2)	-	
td(CLKL-Data)	FMC_D[15:0] valid data after FMC_CLK low	-	3.5	
td(CLKL-NBLL)	FMC_CLK low to FMC_NBL low	1	-	
td(CLKH-NBLH)	FMC_CLK high to FMC_NBL high	R*THCLK/2+1.5(2)	-	
tsu(NWAIT-CLKH)	FMC_NWAIT valid before FMC_CLK high	1.5	-	
th(CLKH-NWAIT)	FMC_NWAIT valid after FMC_CLK high	4	-	

1. Guaranteed by characterization results, not tested in production.
2. Clock ratio R = (HCLK period /FMC_CLK period).

NAND controller waveforms and timings

Figure 63 through *Figure 66* represent synchronous waveforms, and *Table 144* and *Table 145* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- COM.FMC_SetupTime = 0x01
- COM.FMC_WaitSetupTime = 0x03
- COM.FMC_HoldSetupTime = 0x02
- COM.FMC_HiZSetupTime = 0x01
- ATT.FMC_SetupTime = 0x01
- ATT.FMC_WaitSetupTime = 0x03
- ATT.FMC_HoldSetupTime = 0x02
- ATT.FMC_HiZSetupTime = 0x01
- Bank = FMC_Bank_NAND
- MemoryDataWidth = FMC_MemoryDataWidth_16b
- ECC = FMC_ECC_Enable
- ECCPageSize = FMC_ECCPageSize_512Bytes
- TCLRSetupTime = 0
- TARSetupTime = 0

In all timing tables, the T_{HCLK} is the HCLK clock period.

Figure 63. NAND controller waveforms for read access

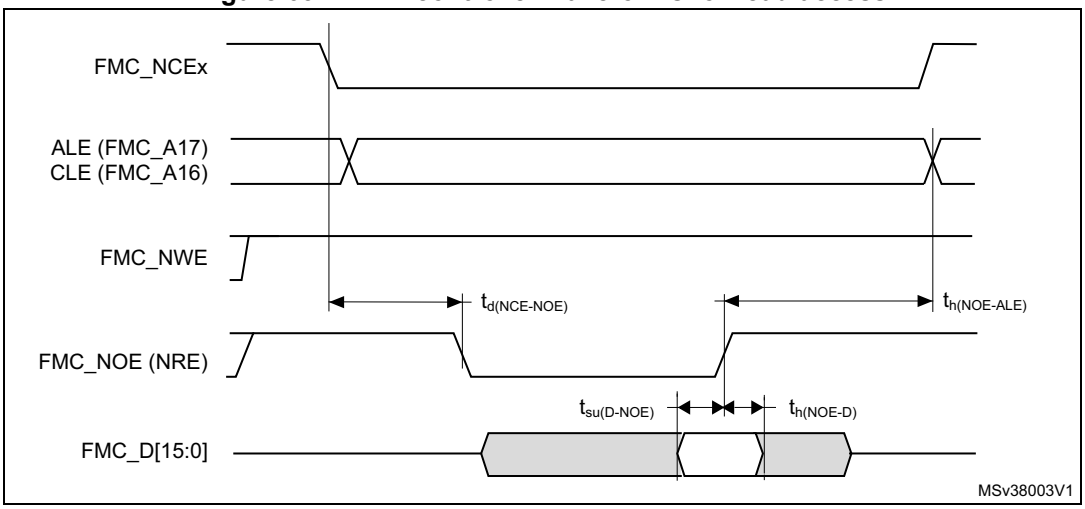


Figure 64. NAND controller waveforms for write access

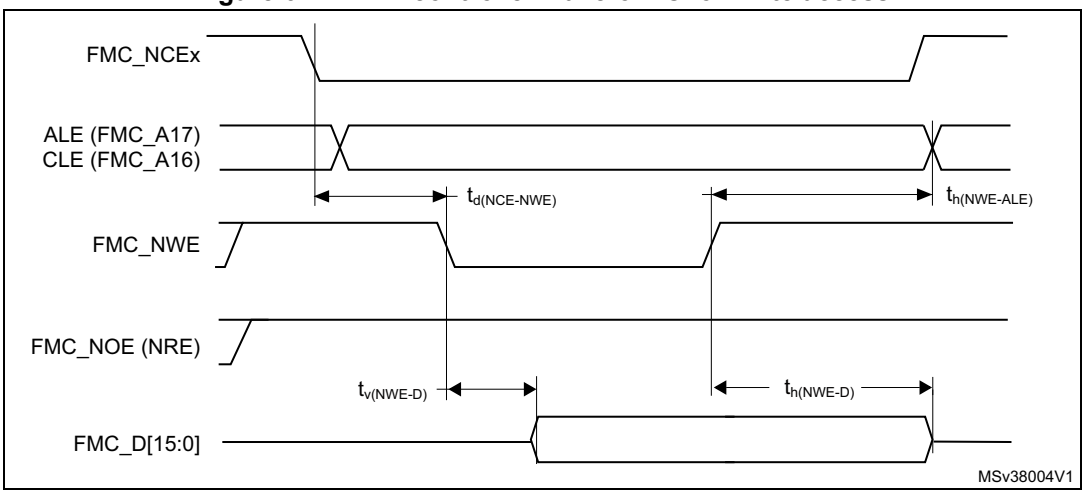


Figure 65. NAND controller waveforms for common memory read access

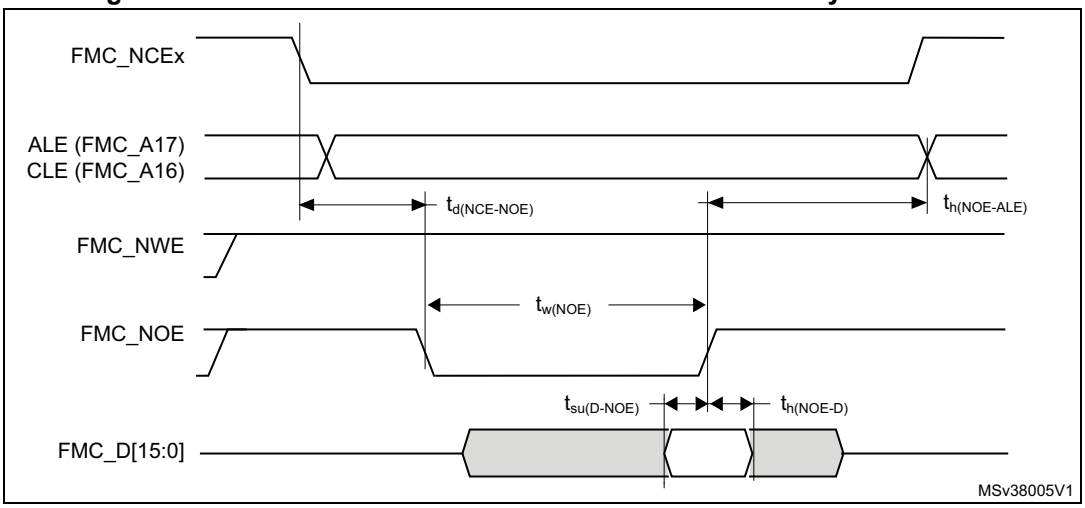


Figure 66. NAND controller waveforms for common memory write access

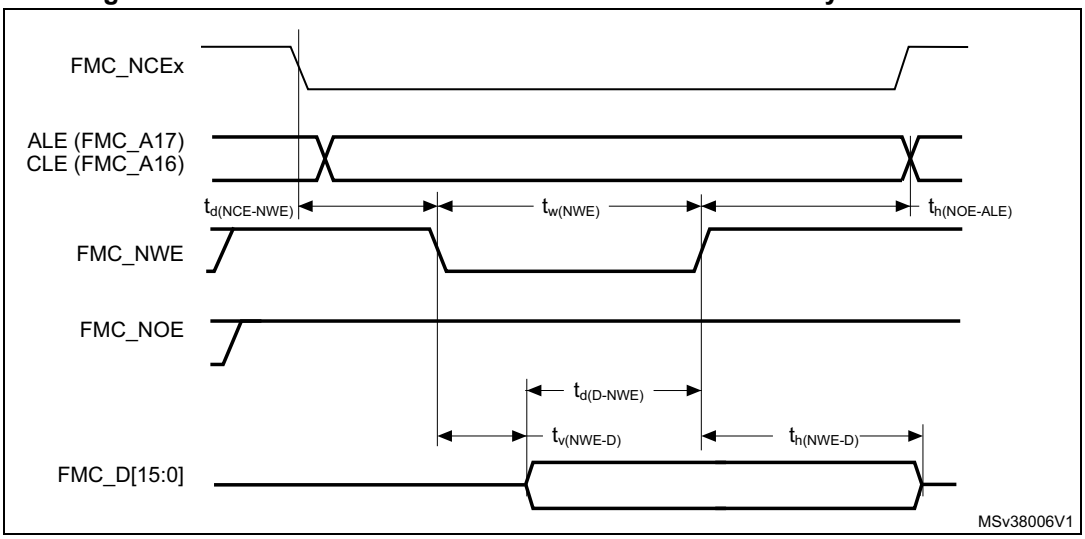


Table 144. Switching characteristics for NAND Flash read cycles(1)

Symbol	Parameter	Min	Max	Unit
Tw(N0E)	FMC_NOE low width	4THCLK - 0.5	4THCLK+0.5	ns
Tsu(D-NOE)	FMC_D[15-0] valid data before FMC_NOE high	14	-	
Th(NOE-D)	FMC_D[15-0] valid data after FMC_NOE high	0	-	
Td(ALE-NOE)	FMC_ALE valid before FMC_NOE low	-	3THCLK-1	
Th(NOE-ALE)	FMC_NWE high to FMC_ALE invalid	3THCLK-0.5	-	

1. Guaranteed by characterization results, not tested in production.

Table 145. Switching characteristics for NAND Flash write cycles(1)

Symbol	Parameter	Min	Max	Unit
Tw(NWE)	FMC_NWE low width	4THCLK - 0.5	4THCLK+0.5	ns
Tv(NWE-D)	FMC_NWE low to FMC_D[15-0] valid	0	-	
Th(NWE-D)	FMC_NWE high to FMC_D[15-0] invalid	2THCLK	-	
Td(D-NWE)	FMC_D[15-0] valid before FMC_NWE high	5THCLK - 1	-	
Td(ALE_NWE)	FMC_ALE valid before FMC_NWE low	-	3THCLK-1	
Th(NWE-ALE)	FMC_NWE high to FMC_ALE invalid	3THCLK-0.5	-	

1. Guaranteed by characterization results, not tested in production.

5.3.31 OCTOSPI characteristics

Unless otherwise specified, the parameters given in *Table 146*, *Table 147* and *Table 148* for OCTOSPI are derived from tests performed under the ambient temperature, f_{AHB} frequency and V_{DD} supply voltage conditions summarized in *Table 27: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- For DTR(with DQS)/HyperBus the delay resister is set to DLYCFGR[3:0]=4

Refer to *Section 5.3.15: I/O port characteristics* for more details on the input/output alternate function characteristics.

The following table summarizes the parameters measured in SDR mode.

Table 146. OCTOSPI(1) characteristics in SDR mode(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F(CLK)	OCTOSPI clock frequency	1.71<V_{DD}<3.6 Voltage ranges 0/1 20 pF	-	-	54	MHz
		2.7<V_{DD}<3.6 Voltage ranges 0/1 20pF	-	-	90	
		1.71<V_{DD}<3.6 Voltage ranges 0/1 15pF	-	-	56	
		1.71<V_{DD}<3.6 Voltage range 2 CL=20pF	-	-	26	
tw(CKH)	OCTOSPI clock high and low time	PRESCALER[7:0] = n = 0,1,3,5	t(CK)/2 - 0.5	-	t(CK)/2	ns
tw(CKL)			t(CK)/2 -0.5	-	t(CK)/2	
tw(CKH)	OCTOSPI clock high and low time Odd division	PRESCALER[7:0] = n = 2,4,6,8	(n/2)×t(CK)/ (n+1)- 0.5	-	(n/2)×t(CK) /(n+1)	
tw(CKL)			(n/2+1)×t(CK)/ (n+1) -0.5	-	(n/2+1)× t(CK)/(n+1)	
ts(IN)	Data input setup time	Voltage ranges 0/1	1.5	-	-	
		Voltage range 2	2	-	-	
th(IN)	Data input hold time	Voltage ranges 0/1	4	-	-	
		Voltage range 2	5.25	-	-	
tv(OUT)	Data output valid time	Voltage ranges 0/1	-	0.5	2	
		Voltage range 2	-	0.5	1.5	
th(OUT)	Data output hold time	Voltage ranges 0/1	-0.5	-	-	
		Voltage range 2	-0.75	-	-	

1. Values in the table applies to octal and quad SPI mode.
2. Guaranteed by characterization results.

The following table summarizes the parameters measured in DTR mode (no DQS).

Table 147. OCTOSPI(1) characteristics in DTR mode (no DQS)(2)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
F(CLK)	OCTOSPI clock frequency	1.71<V_{DD}<3.6 Voltage ranges 0/1 20 pF		-	-	56	MHz
		2.7<V_{DD}<3.6 Voltage ranges 0/1 20 pF		-	-	60	
		1.71<V_{DD}<3.6 Voltage ranges 0/1 15 pF		-	-	60	
		1.71<V_{DD}<3.6 Voltage range 2		-	-	26	
tw(CKH)	OCTOSPI clock high and low time	PRESCALER[7:0] = n = 0,1,3,5		t(CK)/2 -0.5	-	t(CK)/2+0.5	ns
tw(CKL)				t(CK)/2 -0.5	-	t(CK)/2+0.5	
tw(CKH)	OCTOSPI clock high and low time Odd division	PRESCALER[7:0] = n = 2,4,6,8		(n/2)×t(CK)/(n+1)-0.5	-	(n/2)×t(CK)/(n+1)+0.5	
tw(CKL)				(n/2+1)×t(CK)/(n+1) -0.5	-	(n/2+1)×t(CK)/(n+1)+0.5	
tsr(IN), tsf(IN)	Data input setup time	Voltage ranges 0/1		2.5	-	-	
		Voltage range 2		1.5	-	-	
thr(IN),thf(IN)	Data input hold time	Voltage ranges 0/1		3	-	-	
		Voltage range 2		4	-	-	
tvr(OUT), tvf(OUT)	Data output valid time	Voltage ranges 0/1	DHQC=0	-	5.5	7.25	
			DHQC=1 Pres=1,2 …	-	Tpclk /4 +0.5	Tpclk/4 +2	
		Voltage range 2 DHQC=0		-	8	10	
thr(OUT), thf(OUT)	Data output hold time	Voltage ranges 0/1	DHQC=0	5	-	-	
			DHQC=1 Pres=1,2 …	Tpclk/4 -0.25	-	-	
		Voltage range 2 DHQC=0		8	-	-	

1. Values in the table applies to octal and quad SPI mode.
2. Guaranteed by characterization results.

The following table summarizes the parameters measured in DTR mode (with DQS) / HyperBus.

Table 148. OCTOSPI characteristics in DTR mode (with DQS)(1)/Octal and HyperBus

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F(CLK)	OCTOSPI clock frequency	1.71<V_{DD}<3.6 Voltage ranges 0/1 20 pF	-	-	58(2)	MHz
		2.7<V_{DD}<3.6 Voltage ranges 0/1 20 pF	-	-	76(2)	
		1.71<V_{DD}<3.6 Voltage range 2 20 pF	-	-	26(2)	
tw(CKH)	OCTOSPI clock high and low time Even division	-	t(CK)/2 -1	-	t(CK)/2 +0.5	ns
tw(CKL)			t(CK)/2 -0.5	-	t(CK)/2+0.5	
tw(CKH)	OCTOSPI clock high and low time Odd division	-	(n/2)×t(CK)/(n+1) -0.5	-	(n/2)×t(CK)/(n+1) +0.5	
tw(CKL)			(n/2+1)×t(CK)/ (n+1) - 0.5	-	(n/2+1)*×(CK)/ (n+1)+0.5	
tv(CK)	Clock valid time	-	-	-	t(CK) + 2	
th(CK)	Clock hold time	-	t(CK)/2 -0.5	-	-	
VODr(CK)(3)	CK,CK# crossing level on CK rising edge	V_{DD}=1v8	832	-	1050	mV
VODf(CK)(3)	CK,CK# crossing level on CK falling edge	V_{DD}=1v8	840	-	1071	

Table 148. OCTOSPI characteristics in DTR mode (with DQS)(1)/Octal and HyperBus (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
tw(CS)	Chip select high time	-		3×t(CK)	-	-	ns
tv(DQ)	Data input valid time	-		0	-	-	
tv(DS)	Data strobe input valid time						
th(DS)	Data strobe input hold time	-		0	-	-	
tv(RWDS)	Data strobe output valid time	-		-	-	3×t(CK)	
tsr(DQ),tsf(DQ)	Data input setup time	Voltage ranges 0/1		-0.75	-	t(CK)/2 -5.75(4)	
		Voltage range 2		-2.25	-	t(CK)/2 -8(4)	
thr(DQ),thf(DQ)	Data input hold time	Voltage ranges 0/1		3.75	-	-	
		Voltage range 2		4.75	-	-	
tvr(OUT), tvf(OUT)	Data output valid time	Voltage ranges 0/1	DHQC= 0	-	5.75	7.75	
			DHQC= 1 Pres=1, 2…	-	Tpclk/4 +0.75	Tpclk/4 +2.5	
		Voltage range 2 DHQC=0		-	8	11	
thr(OUT), thf(OUT)	Data output hold time	Voltage ranges 0/1	DHQC= 0	3.25	-	-	
			DHQC= 1 Pres=1, 2…	Tpclk/4 -0.25	-	-	
		Voltage range 2 DHQC=0		6.5	-	-	

1. Guaranteed by characterization results.
2. Maximum frequency values are given for a RWDS to DQ skew of maximum +/-1.0 ns.
3. (PA3/PF11), (PF10/PB12), (PF10/PB5), (PE10/PF11), (PA3/PE9) and (PE10/PB5) clk/clk# pair usage is recommended in order to respect HyperMemory AC differential crossing voltage margins.
4. Data input setup time maximum does not take into account the data level switching duration.

Figure 67. OCTOSPI timing diagram - SDR mode

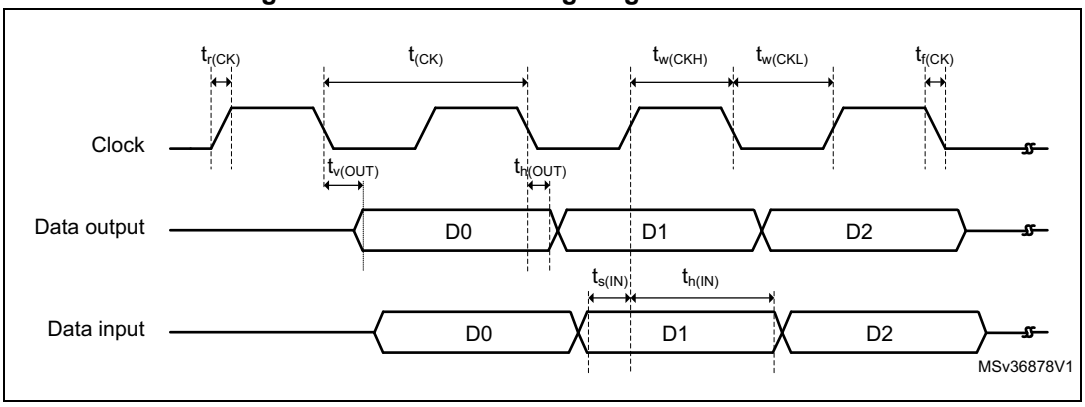


Figure 68. OCTOSPI timing diagram - DDR mode

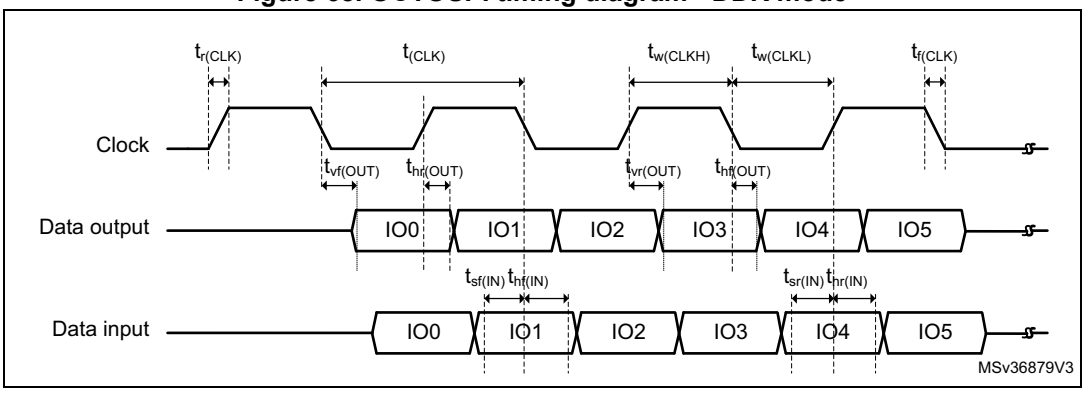


Figure 69. OCTOSPI HyperBus clock

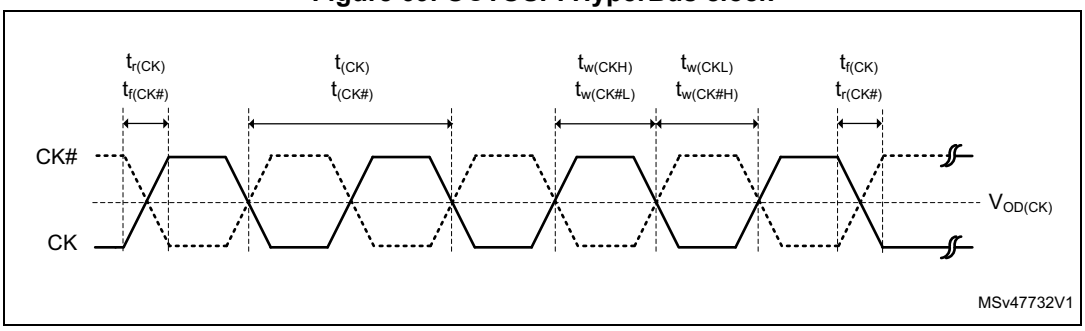


Figure 70. OCTOSPI HyperBus read

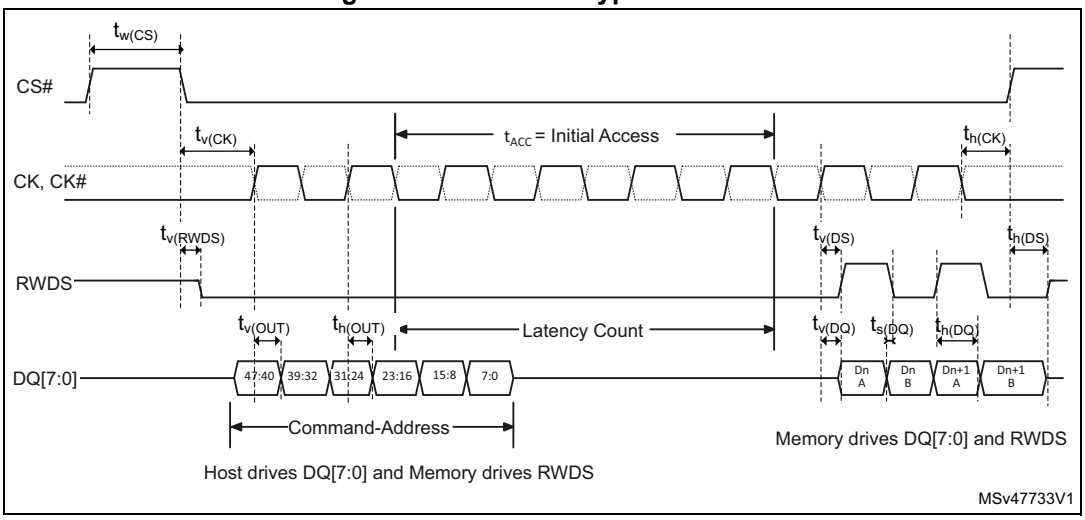


Figure 71. OCTOSPI HyperBus read with double latency

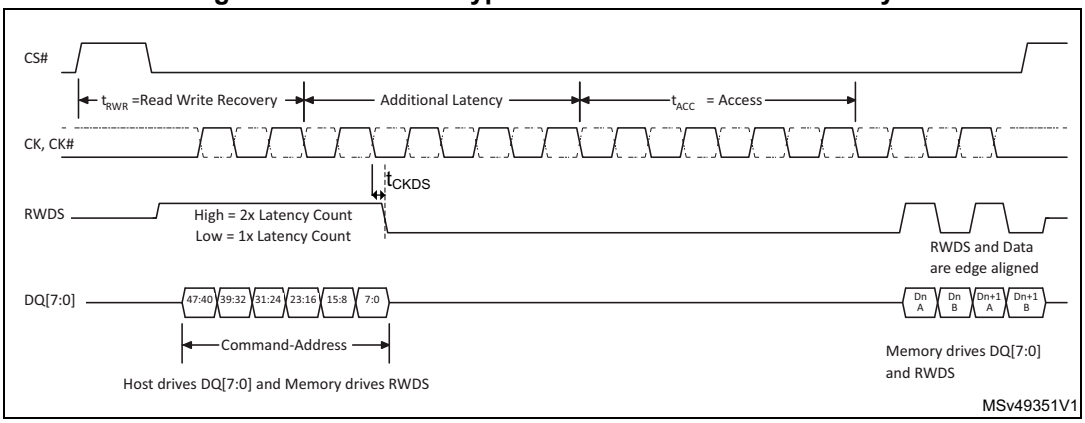
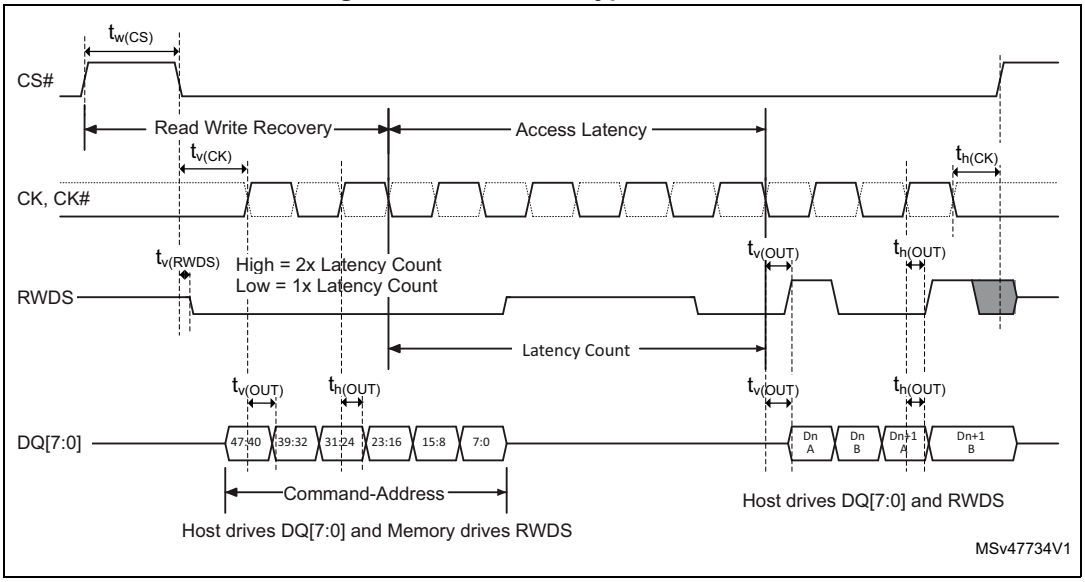


Figure 72. OCTOSPI HyperBus write



Delay block

Unless otherwise specified, the parameters given in *Table 149* for delay block are derived from tests performed under the ambient temperature, fPCLKx frequency and VDD supply voltage conditions summarized in *Table 27: General operating conditions* with the configuration shown in the figure below.

Table 149. Dynamics characteristics: delay block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{init}	Initial delay	-	1175	1375	1450	ps
t_{Δ}	Unit delay	-	250	500	750	

5.3.32 SD/SDIO/MMC card host interfaces (SDMMC)

Unless otherwise specified, the parameters given in *Table 150* and *Table 151* for SDIO are derived from tests performed under the ambient temperature, fPCLKx frequency and VDD supply voltage conditions summarized in *Table 27: General operating conditions* with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to *Section 5.3.15: I/O port characteristics* for more details on the input/output characteristics.

Table 150. Dynamics characteristics: SD / eMMC characteristics, VDD=2.7V to 3.6 V(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
fPP	Clock frequency in data transfer mode	-	0	-	70	MHz
-	SDIO_CK/fPCLK2 frequency ratio	-	-	-	8/3	-
tW(CKL)	Clock low time	fpp =52MHz	8.5	9.5	-	ns
tW(CKH)	Clock high time	fpp =52MHz	8.5	9.5	-	
CMD, D inputs (referenced to CK) in eMMC legacy/SDR/DDR and SD HS/SDR(2)/DDR(2) mode						
tISU	Input setup time HS	-	2.5	-	-	ns
tIHD	Input hold time HS	-	1	-	-	
CMD, D outputs (referenced to CK) in eMMC legacy/SDR/DDR and SD HS/SDR(2)/DDR(2) mode						
tOV	Output valid time HS	-	-	5	6	ns
tOH	Output hold time HS	-	4.5	-	-	
CMD, D inputs (referenced to CK) in SD default mode						
tISUD	Input setup time SD	-	2.5	-	-	ns
tIHD	Input hold time SD	-	1	-	-	

Table 150. Dynamics characteristics: SD / eMMC characteristics, VDD=2.7V to 3.6 V(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CMD, D outputs (referenced to CK) in SD default mode						
tOVD	Output valid default time SD	-	-	1	2.5	ns
tOHD	Output hold default time SD	-	0.5	-	-	

1. Guaranteed by characterization results.
2. For SD 1.8 V support, an external voltage converter is needed.

Table 151. Dynamics characteristics: eMMC characteristics VDD=1.71 V to 1.9 V(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
fPP	Clock frequency in data transfer mode	-	0	-	52	MHz
-	SDIO_CK/fPCLK2 frequency ratio	-	-	-	8/3	-
tW(CKL)	Clock low time	fpp =52 MHz	8.5	9.5	-	ns
tW(CKH)	Clock high time	fpp =52 MHz	8.5	9.5	-	
CMD, D inputs (referenced to CK) in eMMC mode						
tISU	Input setup time HS	-	2.5	-	-	ns
tIH	Input hold time HS	-	2	-	-	
CMD, D outputs (referenced to CK) in eMMC mode						
tOV	Output valid time HS	-	-	5.5	6.5	ns
tOH	Output hold time HS	-	4	-	-	

1. Guaranteed by characterization results.
2. Cload=20 pF.

See the different SDMMC diagrams in *Figure 73*, *Figure 74* and *Figure 75* below.

Figure 73. SDIO high-speed mode

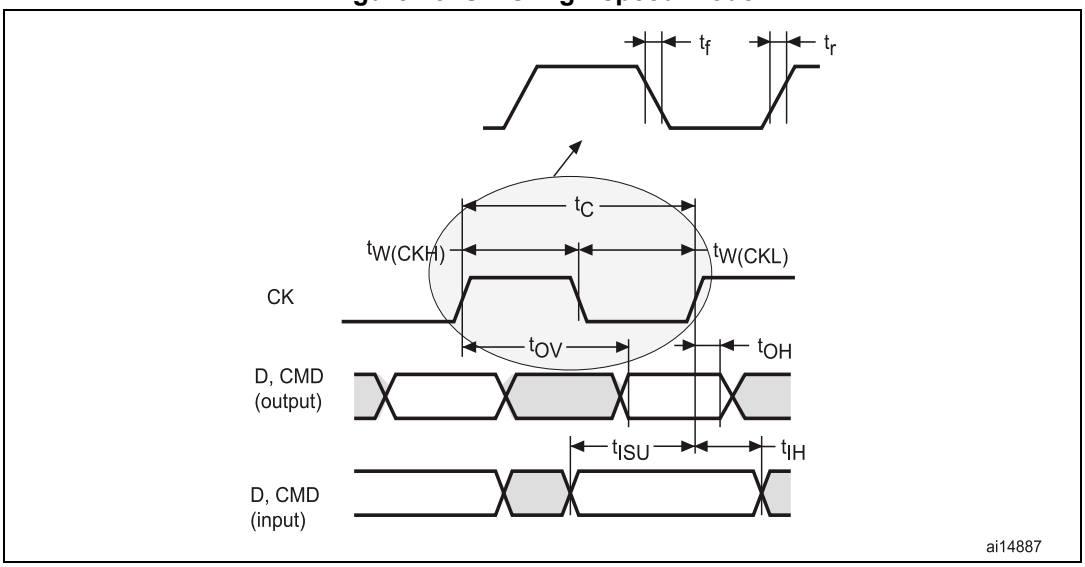


Figure 74. SD default mode

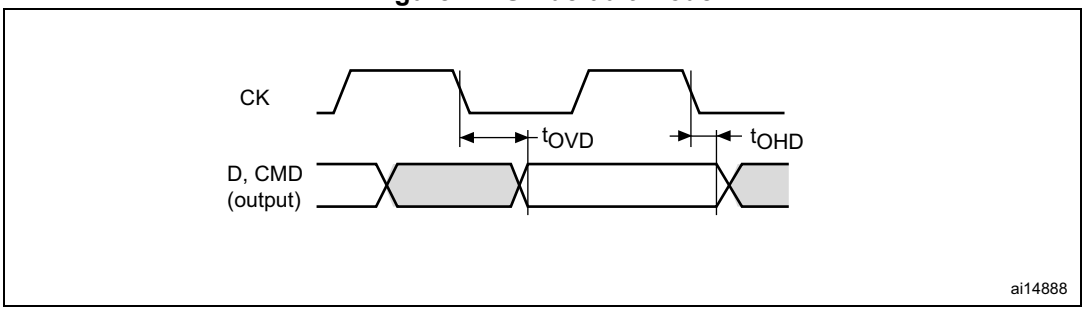
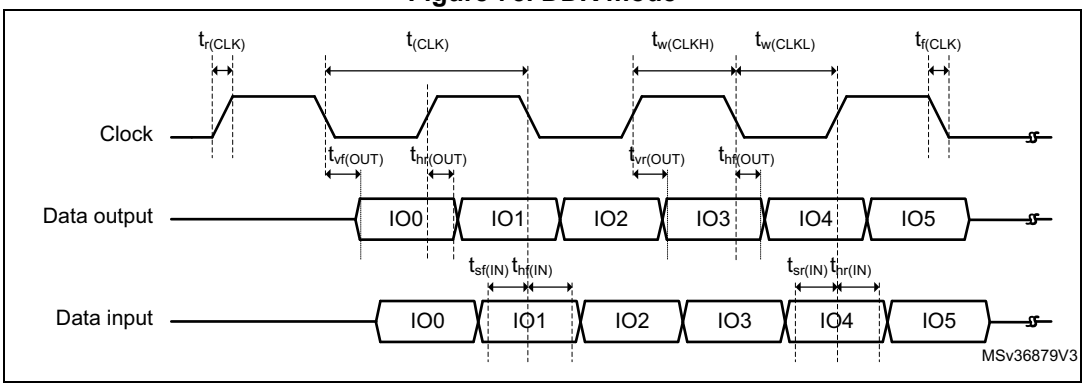


Figure 75. DDR mode



5.3.33 UCPD characteristics

UCPD controller complies with USB Type-C Rev 1.2 and USB Power Delivery Rev 3.0 specifications.

Table 152. UCPD characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	UCPD operating supply voltage	Sink mode only	3.0	3.3	3.6	V
		Sink and source mode	3.135	3.3	3.465	

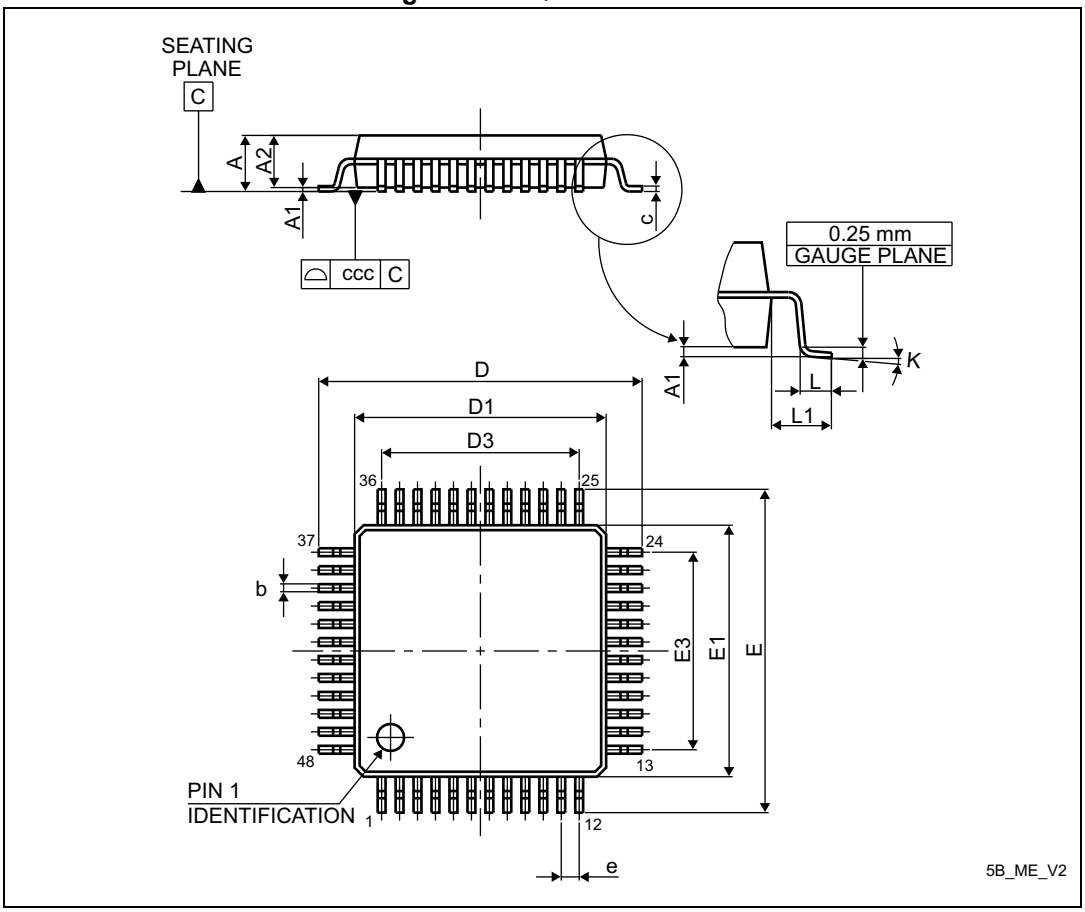
6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

6.1 LQFP48 package information

LQFP48 is a 48-pin, 7 x 7 mm, low-profile quad flat package.

Figure 76. LQFP48 outline



1. Drawing is not to scale.

Table 153. LQFP48 mechanical data

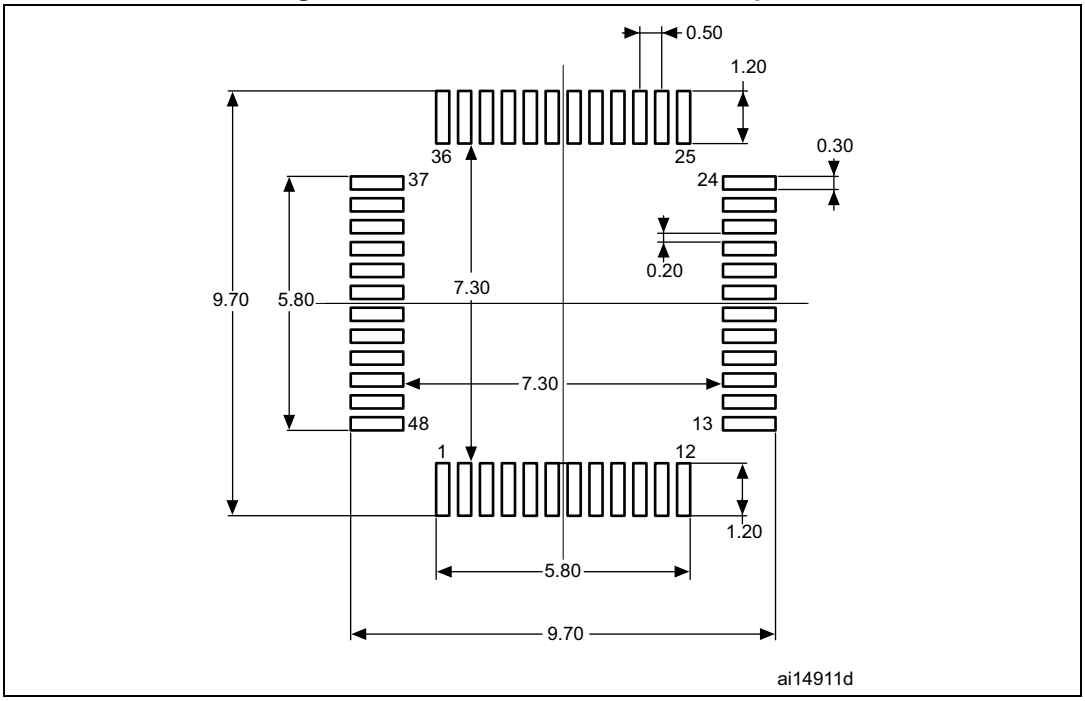
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571

Table 153. LQFP48 mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 77. LQFP48 recommended footprint



1. Dimensions are expressed in millimeters.

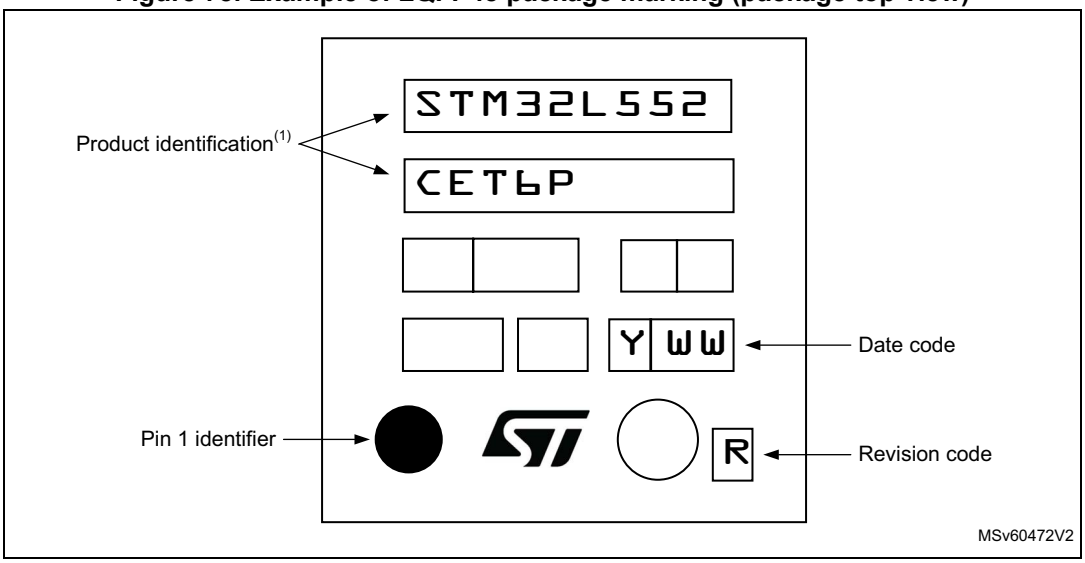
Device marking for LQFP48

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which also depend on supply chain operations, are not indicated below.

Figure 78. Example of LQFP48 package marking (package top view)

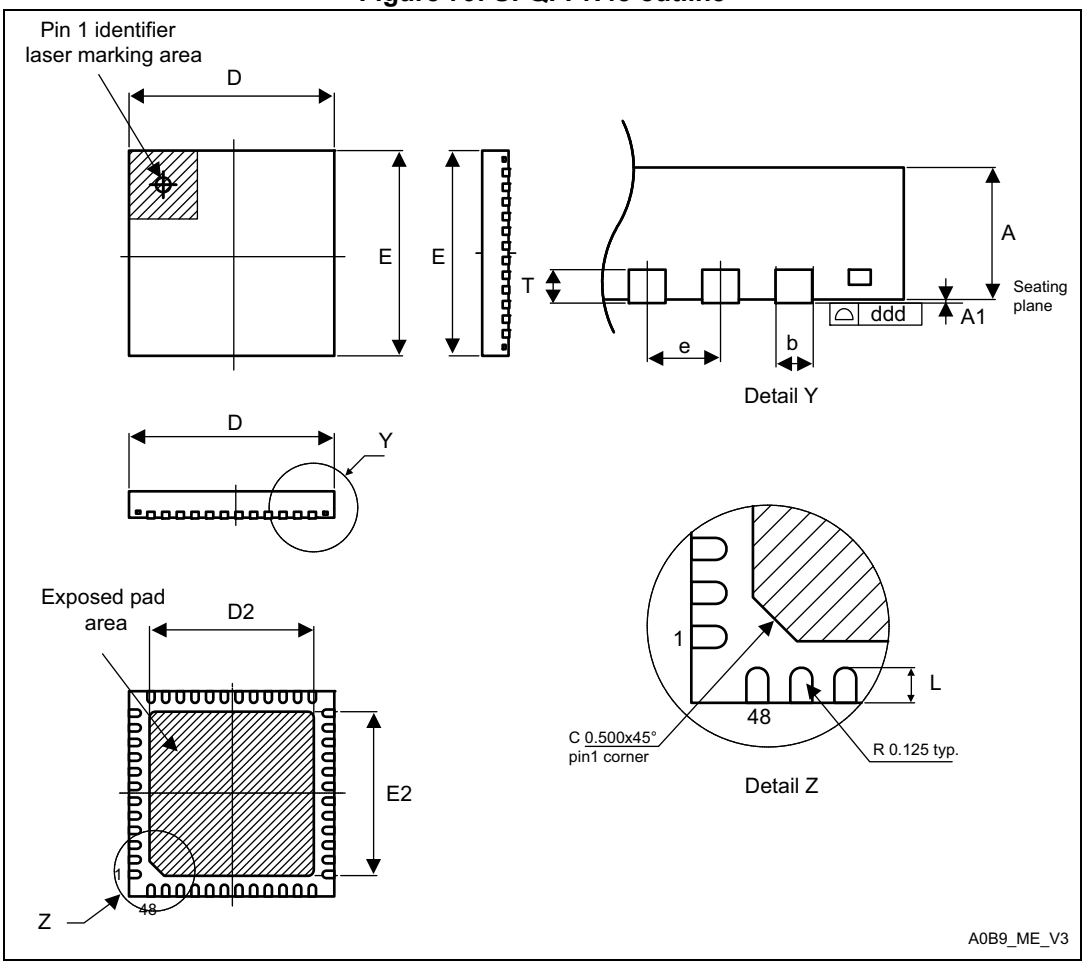


1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

6.2 UFQFPN48 package information

UFQFPN48 is a 48-lead, 7 x 7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package.

Figure 79. UFQFPN48 outline



1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this back-side pad to PCB ground.

Table 154. UFQFPN48 mechanical data

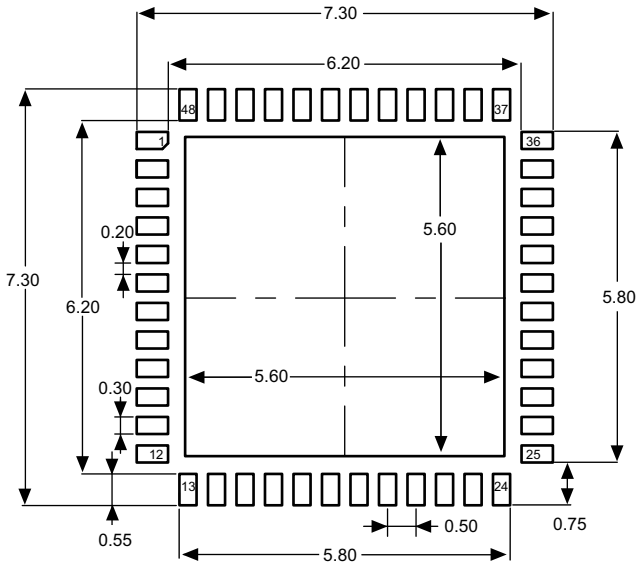
Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
D	6.900	7.000	7.100	0.2717	0.2756	0.2795
E	6.900	7.000	7.100	0.2717	0.2756	0.2795
D2	5.500	5.600	5.700	0.2165	0.2205	0.2244
E2	5.500	5.600	5.700	0.2165	0.2205	0.2244

Table 154. UFQFPN48 mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
T	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
e	-	0.500	-	-	0.0197	-
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 80. UFQFPN48 recommended footprint



1. Dimensions are expressed in millimeters.

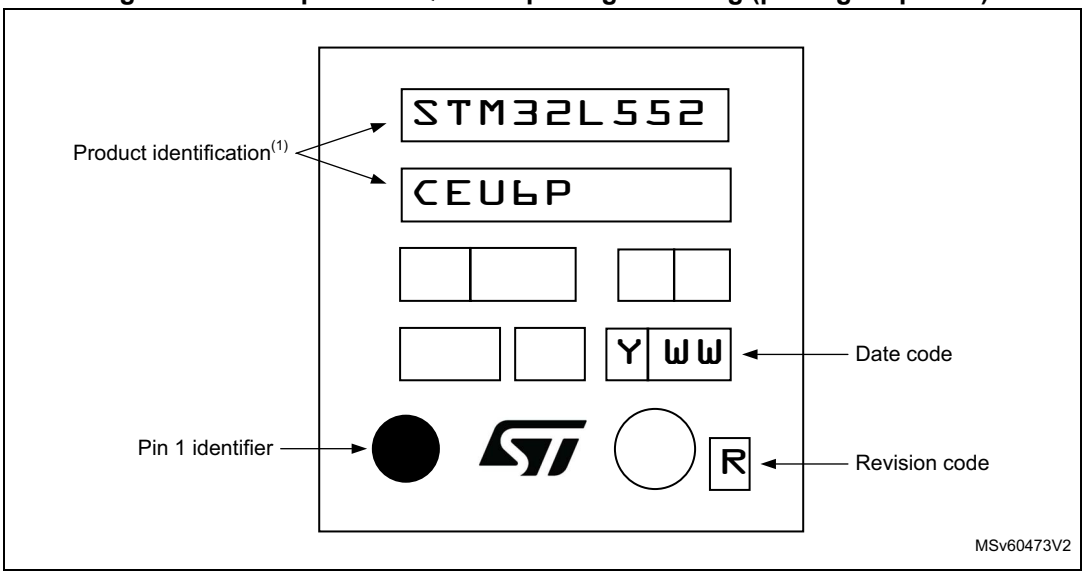
Device marking for UFQFPN48 (7 x 7)

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which also depend on supply chain operations, are not indicated below.

Figure 81. Example of UFQFPN48 package marking (package top view)

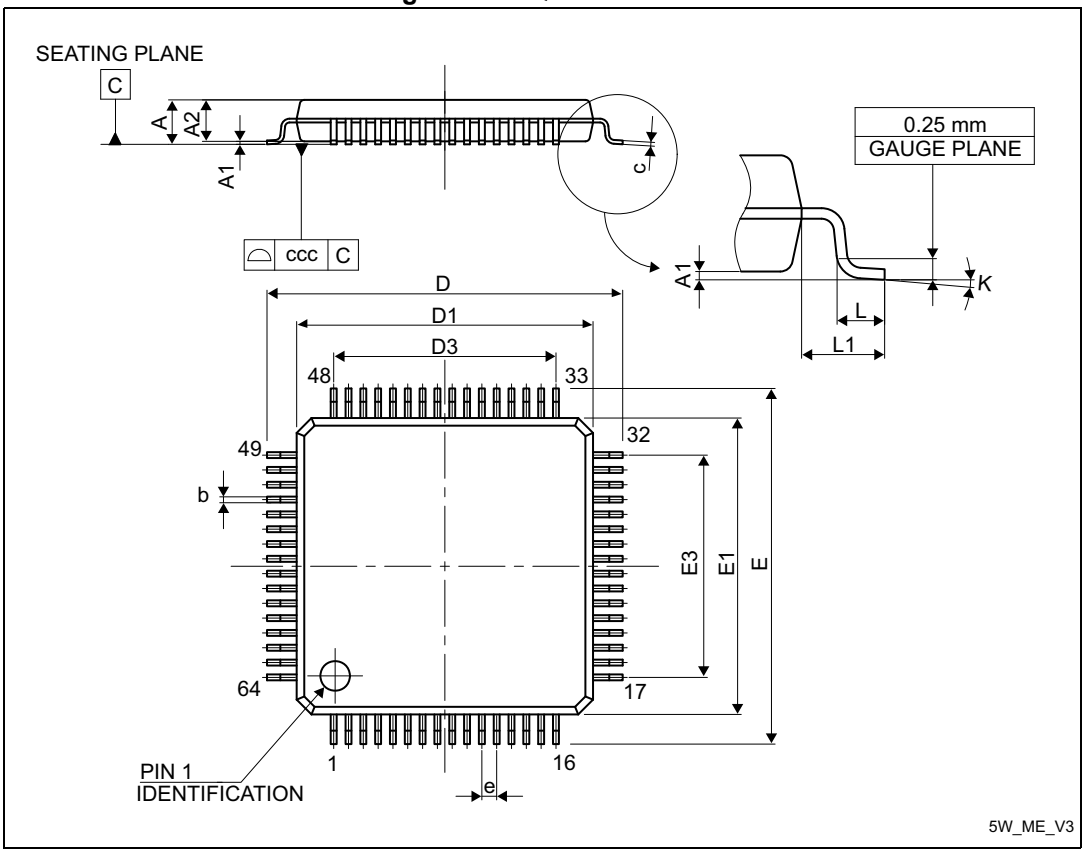


1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

6.3 LQFP64 package information

LQFP64 is a 64-pin, 10 x 10 mm, low-profile quad flat package.

Figure 82. LQFP64 outline



1. Drawing is not to scale.

Table 155. LQFP64 mechanical data

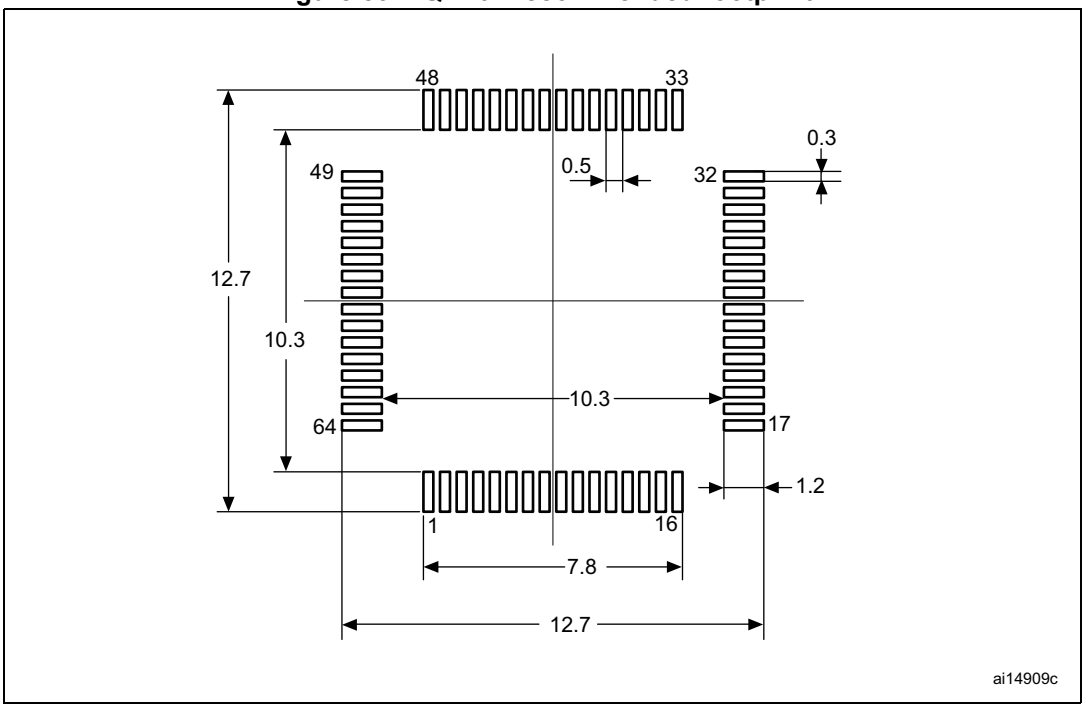
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-

Table 155. LQFP64 mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E3	-	7.500	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 83. LQFP64 recommended footprint



1. Dimensions are expressed in millimeters.

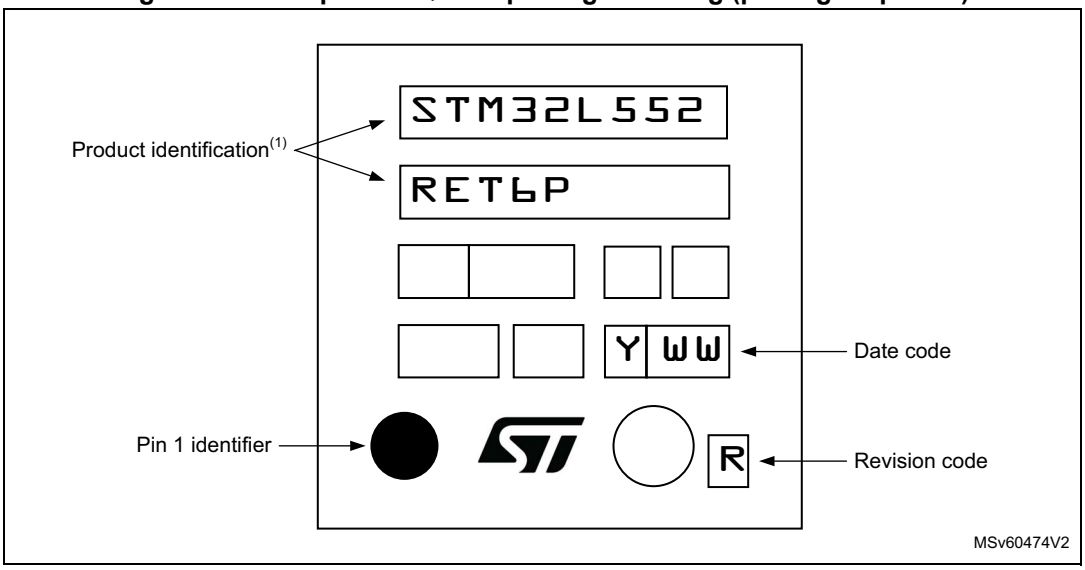
Device marking for LQFP64 (10 x 10)

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which also depend on supply chain operations, are not indicated below.

Figure 84. Example of LQFP64 package marking (package top view)

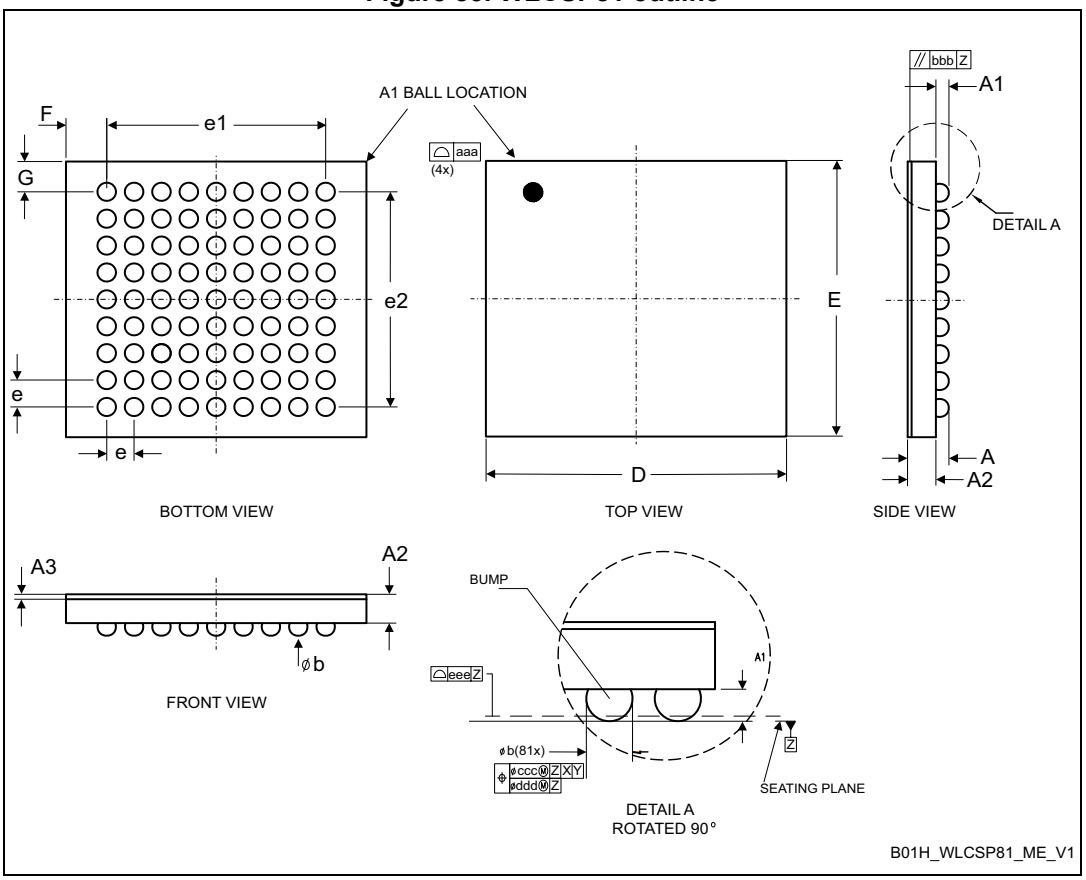


1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

6.4 WLCSP81 package information

WLCSP81 is a 81-ball, 4.36 x 4.07 mm, 0.4 mm pitch, wafer level chip scale package.

Figure 85. WLCSP81 outline



1. Drawing is not to scale.
2. Dimension is measured at the maximum bump diameter parallel to primary datum Z.
3. Primary datum Z and seating plane are defined by the spherical crowns of the bump.
4. Bump position designation per JESD 95-1, SPP-010.

Table 156. WLCSP81 mechanical data

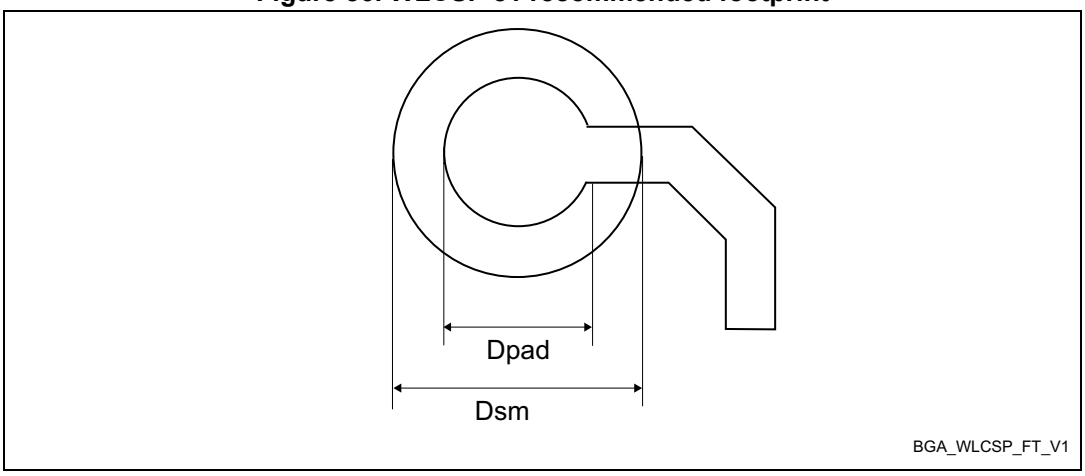
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A[2]	-	-	0.59	-	-	0.023
A1	-	0.18	-	-	0.007	-
A2	-	0.38	-	-	0.015	-
A3[3]	-	0.025	-	-	0.001	-
b	0.22	0.25	0.28	0.009	0.010	0.011
D	4.33	4.36	4.39	0.170	0.172	0.173
E	4.05	4.07	4.09	0.159	0.160	0.161

Table 156. WLCSP81 mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
e	-	0.40	-	-	0.016	-
e1	-	3.20	-	-	0.126	-
e2	-	3.20	-	-	0.126	-
F[4]	-	0.580	-	-	0.023	-
G[4]	-	0.435	-	-	0.017	-
aaa	-	0.10	-	-	0.004	-
bbb	-	0.10	-	-	0.004	-
ccc	-	0.10	-	-	0.004	-
ddd	-	0.05	-	-	0.002	-
eee	-	0.05	-	-	0.002	-

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. The maximum total package height is calculated by the RSS method (Root Sum Square) using nominal and tolerances values of A1 and A2.
3. Back side coating. Nominal dimension is rounded to the 3rd decimal place resulting from process capability.
4. Calculated dimensions are rounded to the 3rd decimal place.

Figure 86. WLCSP 81 recommended footprint



1. Dimensions are expressed in millimeters.

Table 157. WLCSP81 recommended PCB design rules

Dimension	Recommended values
Pitch	0.4 mm
Dpad	0,225 mm
Dsm	0.290 mm typ. (depends on soldermask registration tolerance)
Stencil opening	0.250 mm
Stencil thickness	0.100 mm

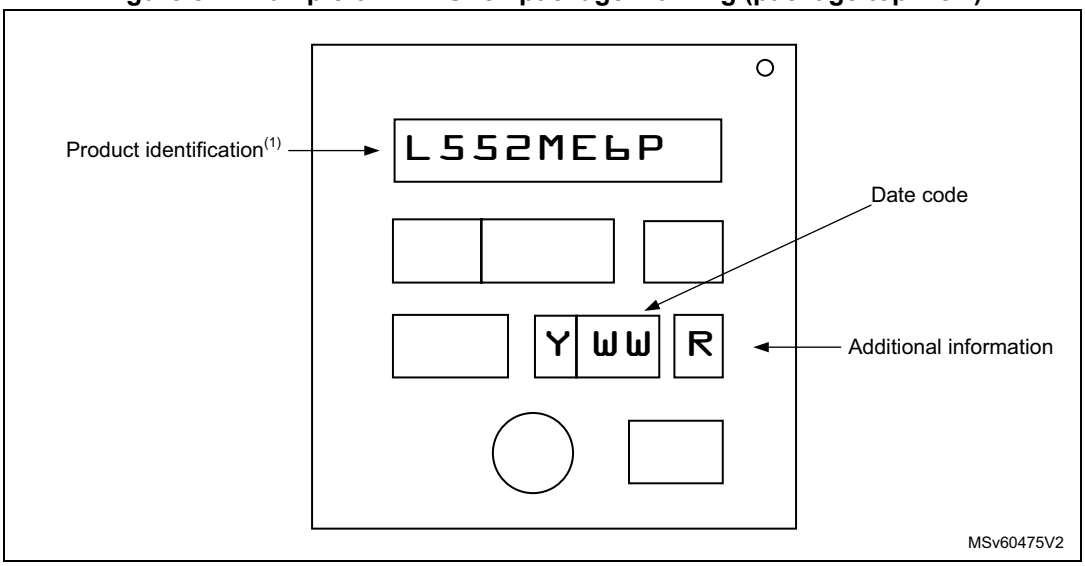
Device marking for WLCSP81

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which also depend on supply chain operations, are not indicated below.

Figure 87. Example of WLCSP81 package marking (package top view)

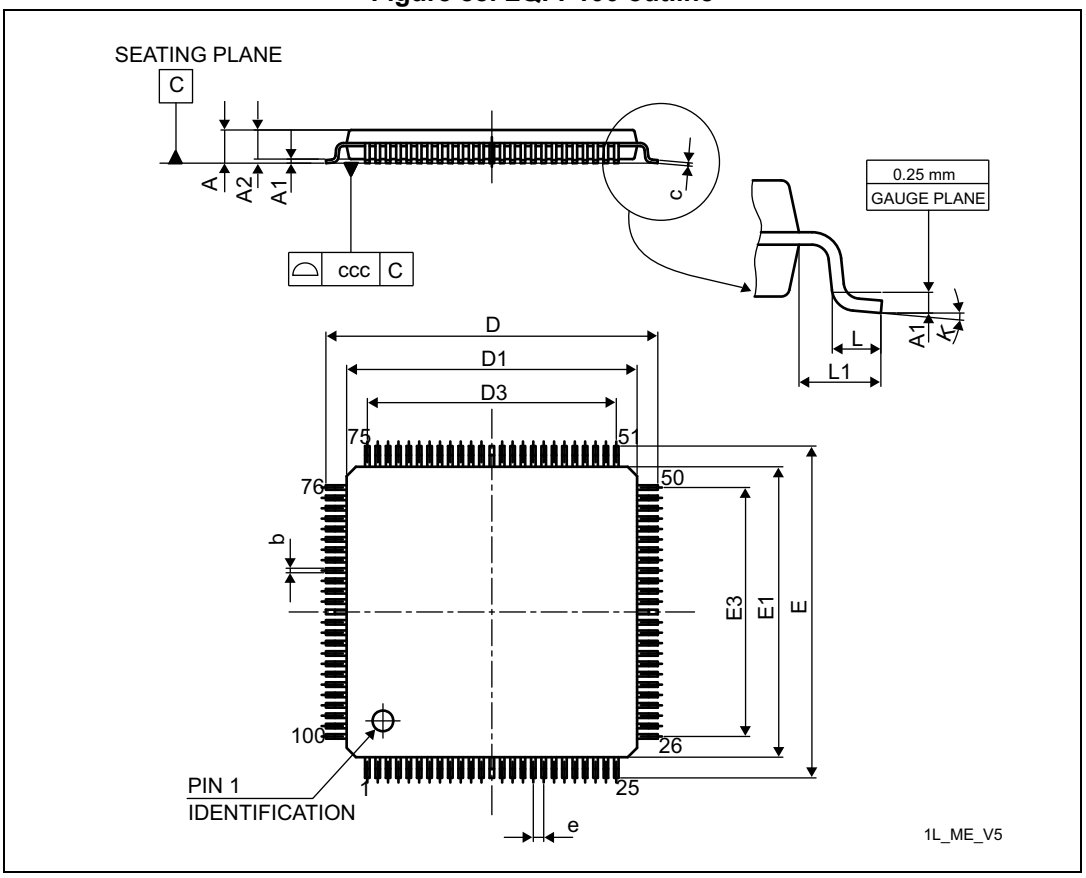


1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

6.5 LQFP100 package information

LQFP100 is a 100-pin, 14 x 14 mm low-profile quad flat package.

Figure 88. LQFP100 outline



1. Drawing is not to scale.

Table 158. LQPF100 mechanical data

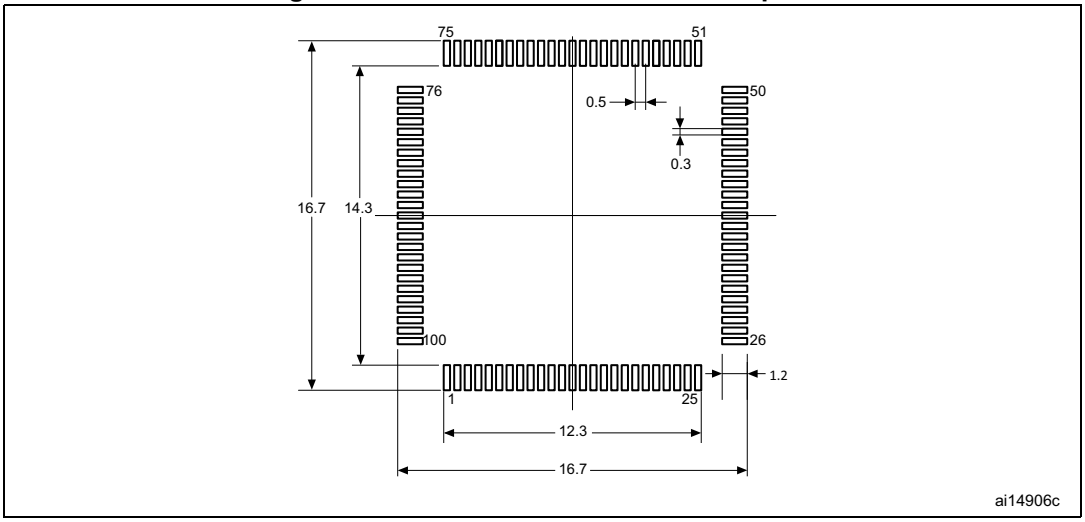
Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378

Table 158. LQPF100 mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 89. LQFP100 recommended footprint



1. Dimensions are expressed in millimeters.

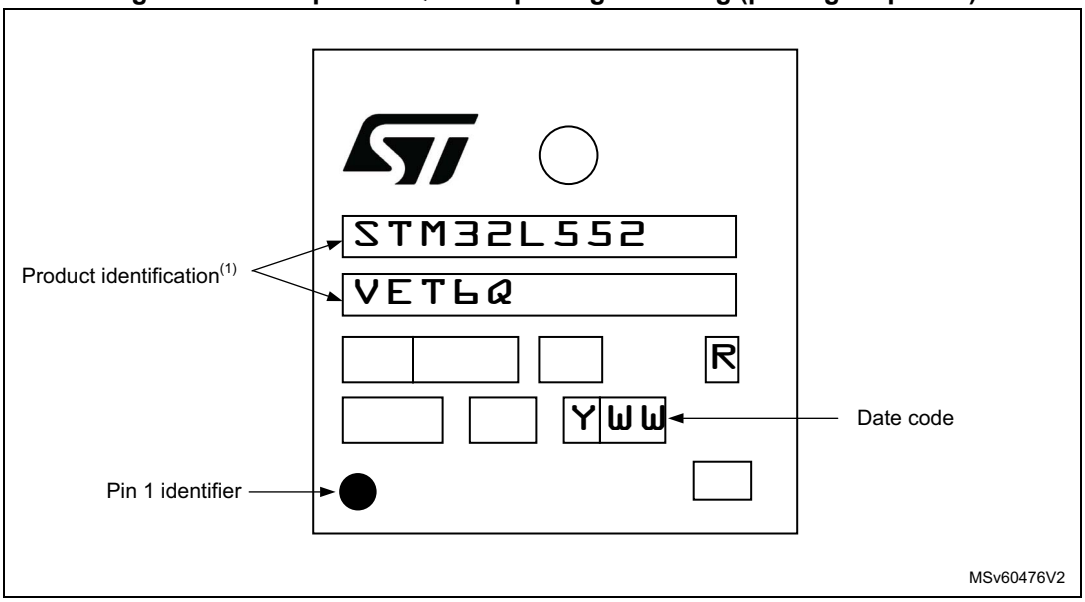
Device marking for LQFP100

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which also depend on supply chain operations, are not indicated below.

Figure 90. Example of LQFP100 package marking (package top view)

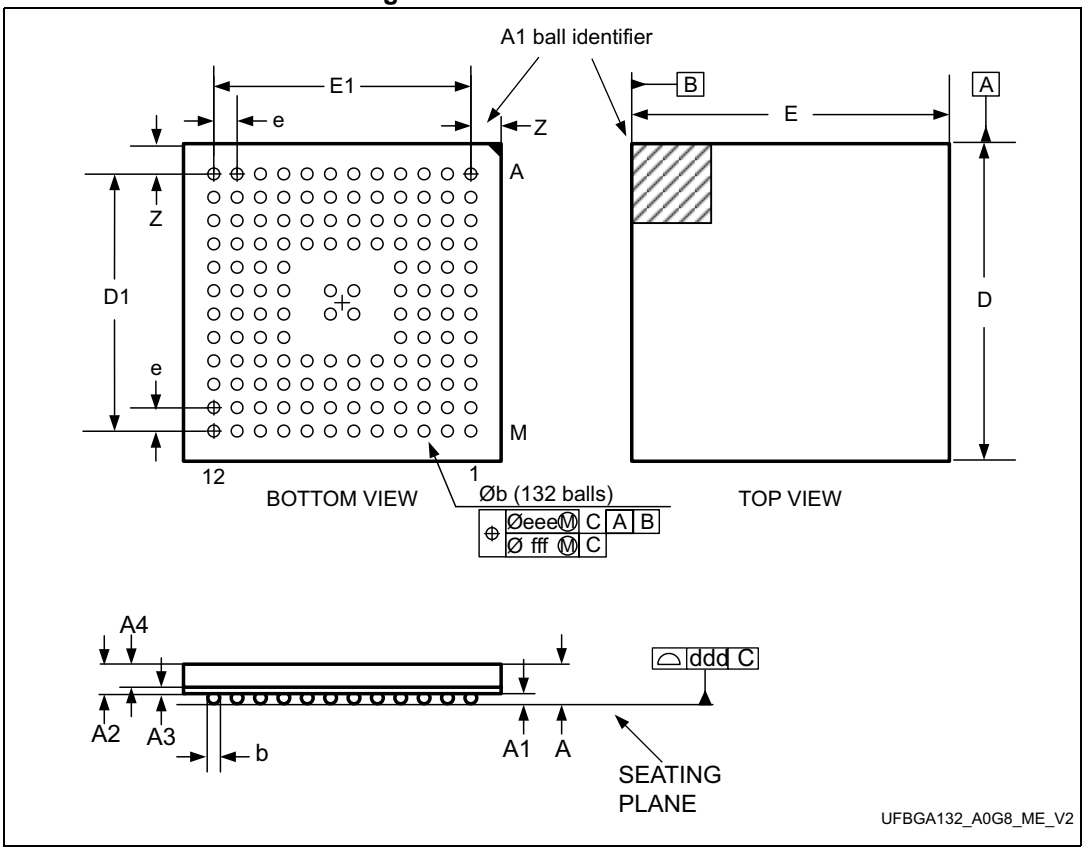


1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

6.6 UFBGA132 package information

UFBGA132 is a 132-pin, 7 x 7 mm, ultra thin fine pitch ball grid array package.

Figure 91. UFBGA132 outline



1. Drawing is not to scale.

Table 159. UFBGA132 mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	0.600	-	-	0.0236
A1	-	-	0.110	-	-	0.0043
A2	-	0.450	-	-	0.0177	-
A3	-	0.130	-	-	0.0051	-
A4	-	0.320	-	-	0.0126	-
b	0.240	0.290	0.340	0.0094	0.0114	0.0134
D	6.850	7.000	7.150	0.2697	0.2756	0.2815
D1	-	5.500	-	-	0.2165	-
E	6.850	7.000	7.150	0.2697	0.2756	0.2815
E1	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-

Table 159. UFBGA132 mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
Z	-	0.750	-	-	0.0295	-
ddd	-	0.080	-	-	0.0031	-
eee	-	0.150	-	-	0.0059	-
fff	-	0.050	-	-	0.0020	-

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 92. UFBGA132 recommended footprint

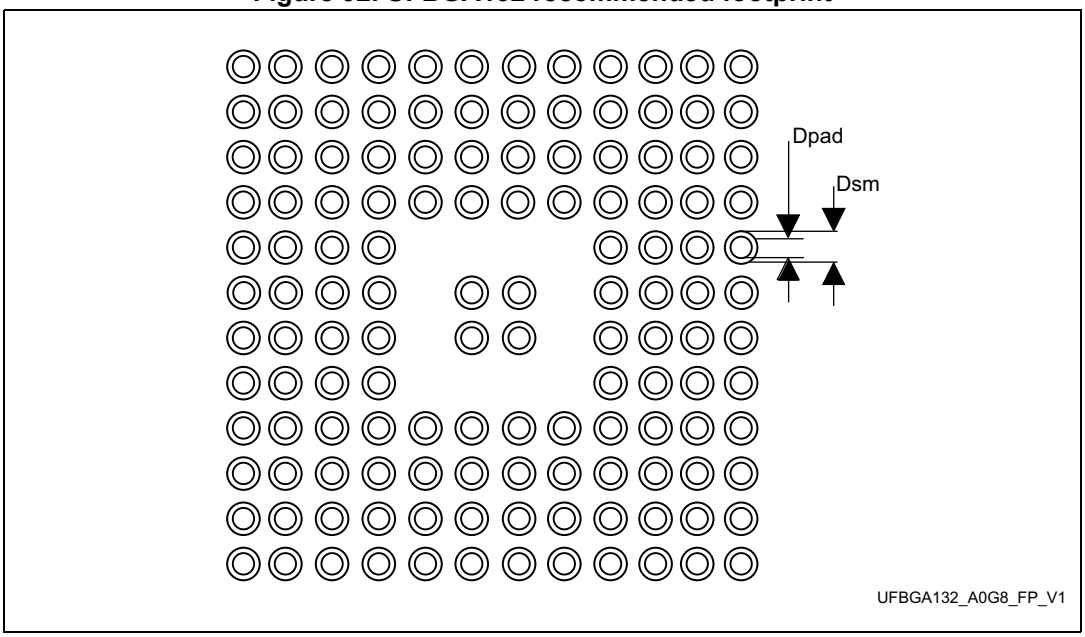


Table 160. UFBGA132 recommended PCB design rules (0.5 mm pitch BGA)

Dimension	Recommended values
Pitch	0.5 mm
Dpad	0.280 mm
Dsm	0.370 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.280 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.100 mm
Ball diameter	0.280 mm

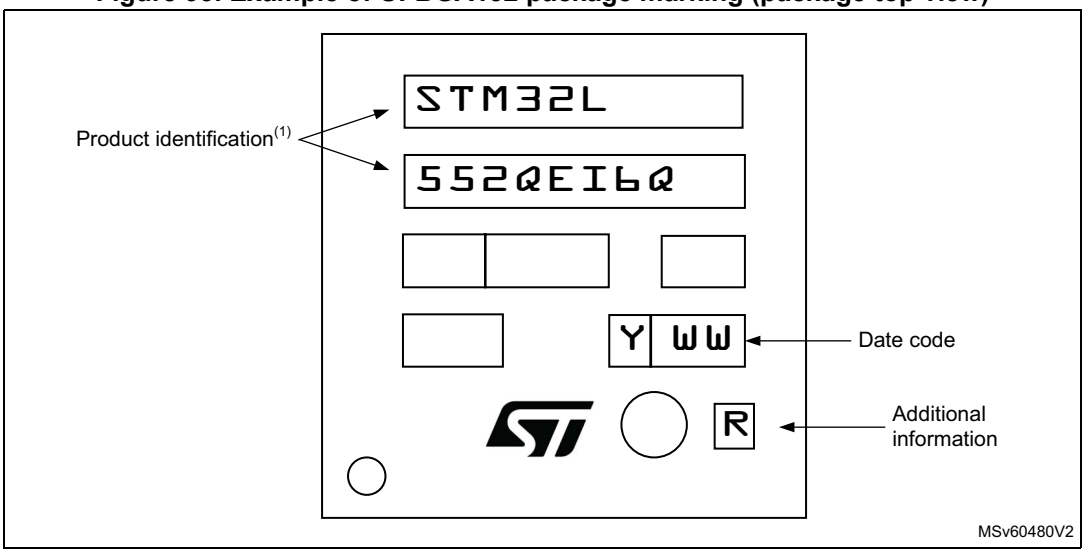
Device marking for UFBGA132 (7 x 7)

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which also depend on supply chain operations, are not indicated below.

Figure 93. Example of UFBGA132 package marking (package top view)

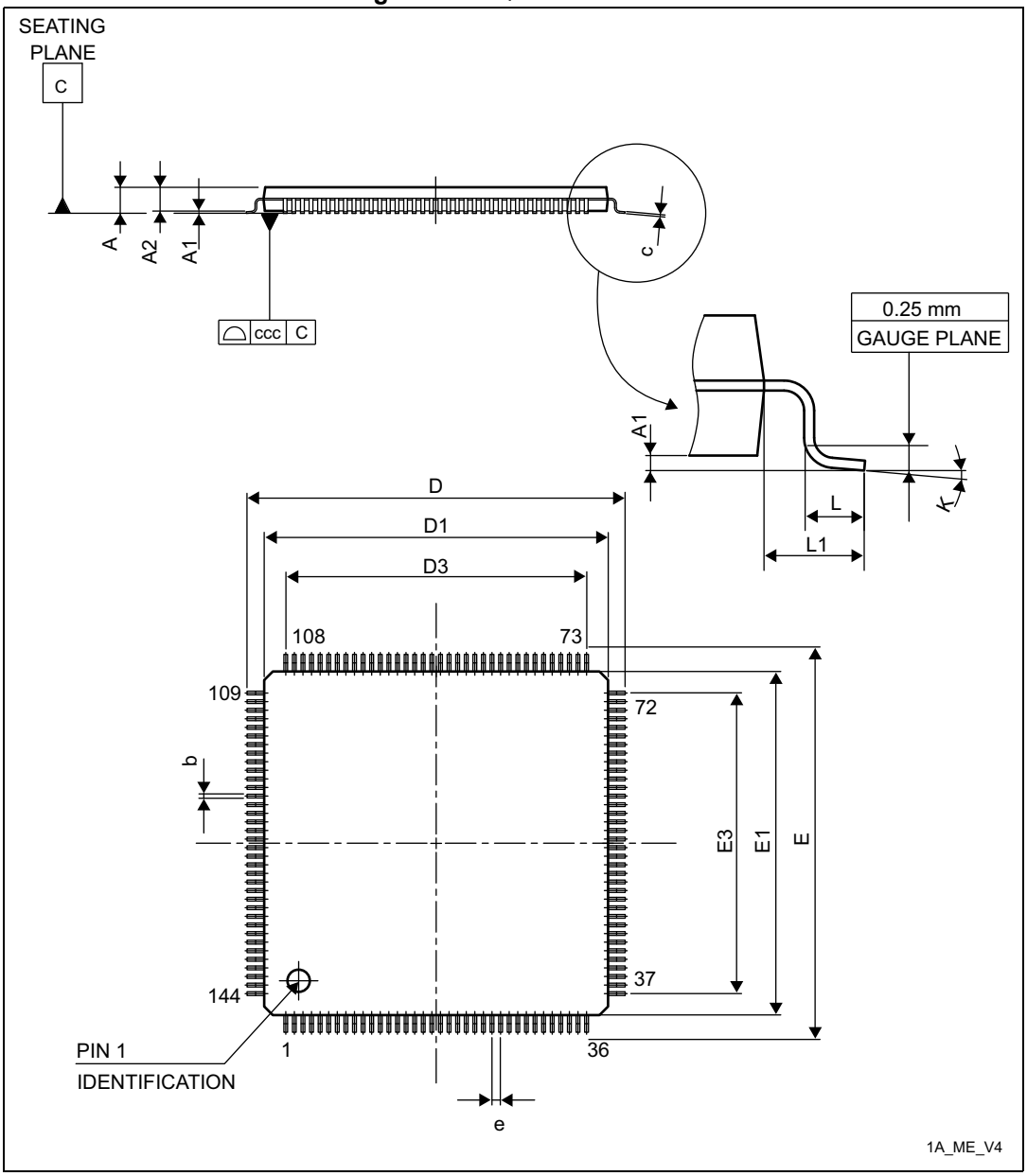


1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

6.7 LQFP144 package information

LQFP144 is a 144-pin, 20 x 20 mm low-profile quad flat package.

Figure 94. LQFP144 outline



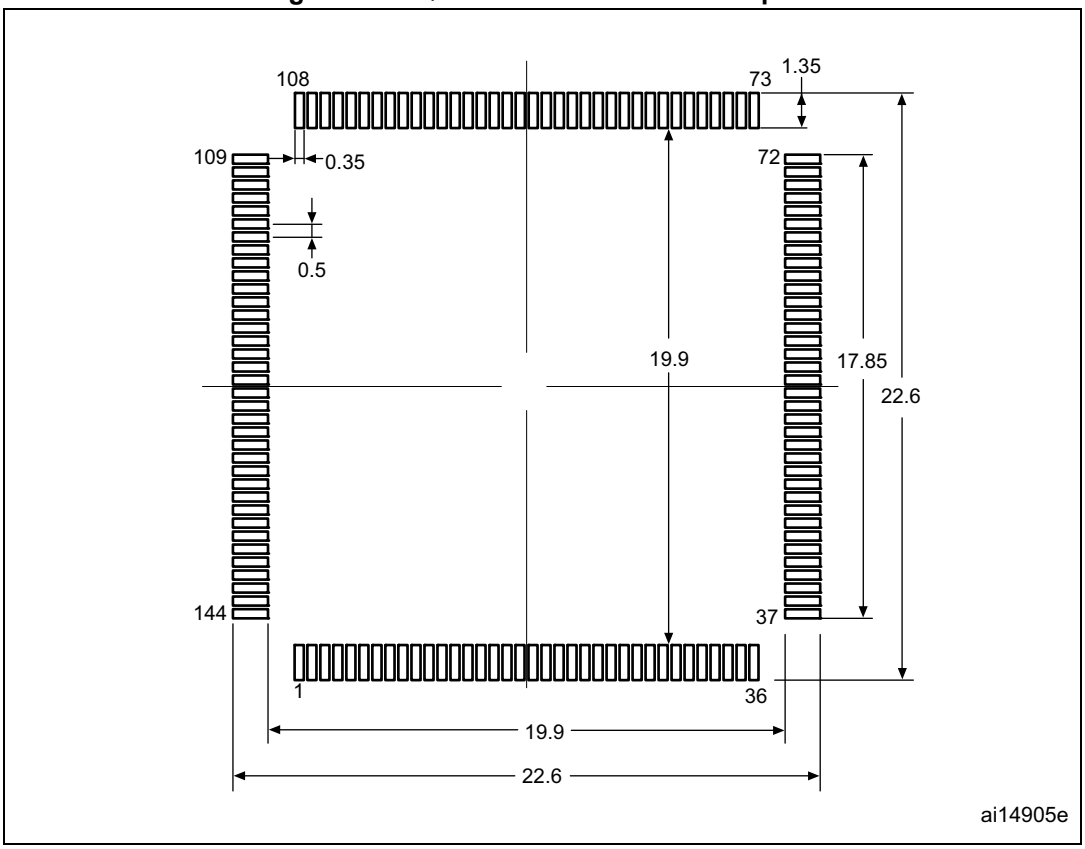
1. Drawing is not to scale.

Table 161. LQFP144 mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	21.800	22.000	22.200	0.8583	0.8661	0.8740
D1	19.800	20.000	20.200	0.7795	0.7874	0.7953
D3	-	17.500	-	-	0.6890	-
E	21.800	22.000	22.200	0.8583	0.8661	0.8740
E1	19.800	20.000	20.200	0.7795	0.7874	0.7953
E3	-	17.500	-	-	0.6890	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 95. LQFP144 recommended footprint



1. Dimensions are expressed in millimeters.

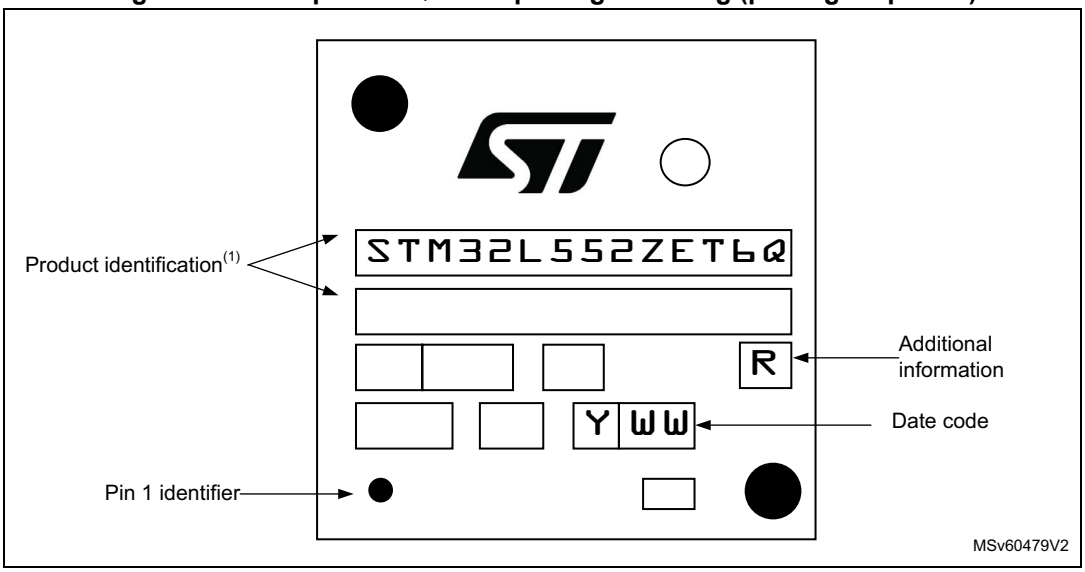
Device marking for LQFP144

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which also depend on supply chain operations, are not indicated below.

Figure 96. Example of LQFP144 package marking (package top view)



1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

6.8 Thermal characteristics

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

T_J max = T_A max + (P_D max x Θ_{JA})

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$P_{I/O}$ max = Σ (V_{OL} × I_{OL}) + Σ ((V_{DDIOx} – V_{OH}) × I_{OH}),

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 162. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** LQFP144 20 x 20 mm	47.4	°C/W
	Thermal resistance junction-ambient LQFP100 - 14 × 14 mm	49.3	
	Thermal resistance junction-ambient LQFP64 10 x 10 mm	50.7	
	Thermal resistance junction-ambient LQFP48 7 x 7 mm	52.3	
	Thermal resistance junction-ambient UFQFPN48 7 x 7 mm	25.6	
	Thermal resistance junction-ambient UFBGA132 7 x 7 mm	39.6	
	Thermal resistance junction-ambient WLCSP81 4.36 x 4.07 mm	45	

Table 162. Package thermal characteristics (continued)

Symbol	Parameter	Value	Unit
Θ_{JC}	**Thermal resistance junction-case** LQFP144 20 x 20 mm	13.5	°C/W
	Thermal resistance junction-case LQFP100 - 14 × 14 mm	14	
	Thermal resistance junction-case LQFP64 10 x 10 mm	14.2	
	Thermal resistance junction-case LQFP48 7 x 7 mm	14.4	
	Thermal resistance junction-case UFQFPN48 7 x 7 mm	1.5	
	Thermal resistance junction-case UFBGA132 7 x 7 mm	38.1	
	Thermal resistance junction-case WLCSP81 4.36 x 4.07 mm	1.5	
Θ_{JB}	**Thermal resistance junction-board** LQFP144 20 x 20 mm	43.3	°C/W
	Thermal resistance junction-board LQFP100 - 14 × 14 mm	41.5	
	Thermal resistance junction-board LQFP64 10 x 10 mm	39.5	
	Thermal resistance junction-board LQFP48 7 x 7 mm	37.4	
	Thermal resistance junction-board UFQFPN48 7 x 7 mm	13.5	
	Thermal resistance junction-board UFBGA132 7 x 7 mm	13.2	
	Thermal resistance junction-board WLCSP81 4.36 x 4.07 mm	27	

6.8.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

6.8.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Section 7: Ordering information*.

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the STM32L552xx at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range is best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

Example 1: High-performance application

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 82 °C (measured according to JESD51-2), I_{DDmax} = 50 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V and maximum 8 I/Os used at the same time in output at low level with I_{OL} = 20 mA, V_{OL}= 1.3 V

P_{INTmax} = 50 mA × 3.5 V= 175 mW

P_{IOmax} = 20 × 8 mA × 0.4 V + 8 × 20 mA × 1.3 V = 272 mW

This gives: P_{INTmax} = 175 mW and P_{IOmax} = 272 mW:

P_{Dmax} = 175 + 272 = 447 mW

Using the values obtained in T_{Jmax} is calculated as follows:

– For LQFP100, 49.3°C/W

T_{Jmax} = 82 °C + (49.3°C/W × 447 mW) = 82 °C + 22.04 °C = 104.04 °C

This is within the range of the suffix 6 version parts (–40 < T_J < 105 °C) see *Section 7: Ordering information*.

In this case, parts must be ordered at least with the temperature range suffix 6 (see *Section 7: Ordering information*).

Note: With this given P_{Dmax} we can find the TAmax allowed for a given device temperature range (order code suffix 6 or 7).

Suffix 6: T_{Amax} = T_{Jmax} - (49.3°C/W × 447 mW) = 105 - 22.03= 82.97 °C

Suffix 3: T_{Amax} = T_{Jmax} - (49.3°C/W × 447 mW) = 130 - 22.03 = 107.97 °C

Example 2: High-temperature application

Using the same rules, it is possible to address applications that run at high ambient temperatures with a low dissipation, as long as junction temperature T_J remains within the specified range.

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 100 °C (measured according to JESD51-2), I_{DDmax} = 20 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V

P_{INTmax} = 20 mA × 3.5 V= 70 mW

P_{IOmax} = 20 × 8 mA × 0.4 V = 64 mW

This gives: P_{INTmax} = 70 mW and P_{IOmax} = 64 mW:

P_{Dmax} = 70 + 64 = 134 mW

Thus: P_{Dmax} = 134 mW

Using the values obtained in T_{Jmax} is calculated as follows:

– For LQFP100, 49.3 °C/W

T_{Jmax} = 100 °C + (49.3 °C/W × 134 mW) = 100 °C + 6.6 °C = 106.6 °C

This is above the range of the suffix 6 version parts (–40 < T_J < 105 °C).

In this case, parts must be ordered at least with the temperature range suffix 3 (see *Section 7: Ordering information*) unless we reduce the power dissipation in order to be able to use suffix 6 parts.

7 Ordering information

Table 163. STM32L552xx ordering information scheme

Example: STM32 L 552 V E T 6 Q TR

Device family

STM32 = Arm® based 32-bit microcontroller

Product type

L = ultra-low-power

Device subfamily

552 = STM32L552xx

Pin count

C = 48 pins
R = 64 pins
M = 81 pins
V = 100 pins
Q = 132 balls
Z = 144 pins

Flash memory size

E = 512 Kbytes of Flash memory
C= 256 Kbytes of Flash memory

Package

T = LQFP
I = UFBGA
U = UFQFPN
Y = WLCSP

Temperature range

6 = Industrial temperature range, -40 to 85 °C (105 °C junction)
3 = Industrial temperature range, -40 to 125 °C (130°C junction)

Dedicated pinout

Q = Dedicated pinout supporting SMPS step down converter
P = Dedicated pinout supporting external SMPS

Packing

TR = tape and reel
xxx = programmed parts

1. All packages are ECOPACK2 (RoHS compliant and free of brominated, chlorinated and antimony-oxide flame retardants).
2. For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

8 Revision history

Table 164. Document revision history

Date	Revision	Changes
04-Oct-2019	1	Internal release
18-Dec-2019	2	Updated *Section : Features*. Updated *Section 3.3: Memory protection unit*. Updated *Section 3.4: Embedded Flash memory*. Updated *Table 5: Boot space versus RDP protection*. Updated *Section 3.9.4: SMPS step down converter*. Updated *Table 11: Functionalities depending on the working mode*. Updated *Figure 7: STM32L552xx clock tree*. Updated *Table 27: General operating conditions*. Updated *Table 36: Current consumption in Run mode, code with data processing running from Flash in single bank, ICACHE ON in 2-way and power supplied by internal SMPS step down converter*. Updated *Table 37: Current consumption in Run mode, code with data processing running from Flash in single bank, ICACHE ON in 1-way and power supplied by internal SMPS step down converter*. Updated *Table 38: Current consumption in Run mode, code with data processing running from Flash in single bank, ICACHE disabled and power supplied by internal SMPS step down converter*. Updated *Table 42: Current consumption in Run mode, code with data processing running from Flash in dual bank, ICACHE ON in 2-way and power supplied by internal SMPS step down converter*. Updated *Table 43: Current consumption in Run mode, code with data processing running from Flash in dual bank, ICACHE ON in 1-way and power supplied by internal SMPS step down converter*. Updated *Table 44: Current consumption in Run mode, code with data processing running from Flash in dual bank, ICACHE disabled and power supplied by internal SMPS step down converter*. Updated *Table 46: Current consumption in Run mode, code with data processing running from SRAM1 and power supplied by internal SMPS step down converter*. Updated *Table 47: Current consumption in Run and Low-power run modes, code with data processing running from SRAM2*.

Table 164. Document revision history

Date	Revision	Changes
18-Dec-2019	2 (continued)	Updated *Table 48: Current consumption in Run mode, code with data processing running from SRAM2 and power supplied by internal SMPS step down converter*. Updated *Table 61: Current consumption in Sleep mode, Flash ON and power supplied by internal SMPS step down converter*. Updated *Table 76: Current consumption in Stop 2 mode*. Updated *Table 77: Current consumption in Stop 1 mode*.. Updated *Table 79: Current consumption in Standby mode*. Updated *Table 80: Current consumption in Shutdown mode*. Updated *Table 81: Current consumption in VBAT mode*. Updated *Table 83: Low-power mode wakeup timings*. Updated *Table 102: I/O static characteristics*. Updated *Table 103: Output voltage characteristics*. Updated *Table 129: SPI characteristics*. Updated *Table 130: SAI characteristics*. Updated *Table 146: OCTOSPI characteristics in SDR mode*. Updated *Table 147: OCTOSPI characteristics in DTR mode (no DQS)*. Updated *Table 148: OCTOSPI characteristics in DTR mode (with DQS)/Octal and HyperBus*.
11-Feb-2020	3	Updated LQFP silhouette on cover page. Updated *Table 2: STM32L552xx features and peripheral counts*. Updated *Figure 1: STM32L552xx block diagram*. Updated *Section 3.1: Arm® Cortex®-M33 core with TrustZone® and FPU* Updated *Section 3.2: Art Accelerator – instruction cache (ICACHE)* Updated *Section 3.6: Boot modes* Updated *Table 5: Boot space versus RDP protection*. Updated *Table 6: Example of memory map security attribution vs SAU configuration regions*. Updated *Table 7: Securable peripherals by TZSC*. Updated *Section 3.9.4: SMPS step down converter*. Updated *Table 10: STM32L552xx modes overview*. Updated *Table 11: Functionalities depending on the working mode*. Updated *Table 12: STM32L552xx peripherals interconnect matrix*. Updated *Section 3.17.1: Nested vectored interrupt controller (NVIC)*.

Table 164. Document revision history

Date	Revision	Changes
11-Feb-2020	3 (continued)	Updated *Section 3.21: Analog-to-digital converter (ADC)*. Removed information related to UFBGA132_ExtSMPS in *Section 4: Pinouts and pin description*. Updated *Table 24: Voltage characteristics*. Updated *Table 33: Current consumption in Run and Low-power run modes, code with data processing running from Flash in single Bank, ICACHE ON in 2-way*. Updated *Table 55: Typical current consumption in Run and Low-power run modes, with different codes running from SRAM1*. Updated *Table 56: Typical current consumption in Run mode with internal SMPS, with different codes running from SRAM1*. Updated *Table 57: Typical current consumption in Run and Low-power run modes, with different codes running from SRAM2*. Updated *Table 58: Typical current consumption in Run mode with internal SMPS, with different codes running from SRAM2*. Updated *Table 79: Current consumption in Standby mode*. Updated *Table 99: ESD absolute maximum ratings*. Updated *Table 102: I/O static characteristics*. Updated *Table 117: VREFBUF characteristics*. Updated *Table 119: OPAMP characteristics*. Updated *Table 123: Temp and VDD monitoring characteristics*.
14-May-2020	4	Updated: – *Figure 1: STM32L552xx block diagram*. – *Figure 2: STM32L552xx power supply overview*. – *Figure 3: STM32L552xxxxP power supply overview*. – *Figure 12: STM32L552xx UFQFPN48 pinout*. – *Figure 13: STM32L552xxxxP UFQFPN48 external SMPS pinout*. – *Section 5.3.2: SMPS step-down converter*. – *Table 20: Legend/abbreviations used in the pinout table*. Updated title of *Table 36*, *Table 37*, *Table 38*, *Table 42*, *Table 43*, *Table 44*, *Table 46*, *Table 48*, *Table 50*, *Table 52*, *Table 54*, *Table 56*, *Table 58*, *Table 61*.

Table 164. Document revision history

Date	Revision	Changes
14-May-2020	4 (continued)	Added: – *Table 28: SMPS modes summary* – *Table 29: SMPS characteristics* – *Table 62: Current consumption in Run mode, code with data processing running from Flash in single bank, ICACHE ON in 2-way and power supplied by external SMPS*. – *Table 63: Current consumption in Run mode, code with data processing running from Flash in single bank, ICACHE ON in 1-way and power supplied by external SMPS*. – *Table 64: Current consumption in Run mode, code with data processing running from Flash in single bank, ICACHE disabled and power supplied by external SMPS*. – *Table 65: Current consumption in Run mode, code with data processing running from Flash in dual bank, ICACHE on in 2-way and power supplied by external SMPS*. – *Table 66: Current consumption in Run mode, code with data processing running from Flash in dual bank, ICACHE on in 1-way and power supplied by external SMPS*. – *Table 67: Current consumption in Run mode, code with data processing running from Flash in dual bank, ICACHE disabled and power supplied by external SMPS*. – *Table 68: Current consumption in Run mode, code with data processing running from SRAM1, and power supplied by external SMPS*. – *Table 69: Current consumption in Run mode, code with data processing running from SRAM2, and power supplied by external SMPS*. – *Table 70: Current consumption in Sleep mode, Flash ON and power supplied by external SMPS*. – *Table 71: Current consumption in Run mode, code with data processing running from Flash, ICACHE on (2-way) and power supplied by external SMPS*. – *Table 72: Current consumption in Run mode, code with data processing running from Flash, ICACHE on (1-way) and power supplied by external SMPS*. – *Table 73: Current consumption in Run mode, code with data processing running from Flash, ICACHE disabled and power supplied by external SMPS*. – *Table 74: Current consumption in Run mode, code with data processing running from SRAM1, and power supplied by external SMPS*. – *Table 75: Current consumption in Run mode, code with data processing running from SRAM2, and power supplied by external SMPS*.

Table 164. Document revision history

Date	Revision	Changes
14-May-2020	4 (continued)	Updated *Table 102: I/O static characteristics*. Updated *Table 146: OCTOSPI characteristics in SDR mode*. Updated *Table 147: OCTOSPI characteristics in DTR mode (no DQS)*. Updated *Table 148: OCTOSPI characteristics in DTR mode (with DQS)/Octal and HyperBus*. Updated *Table 150: Dynamics characteristics: SD / eMMC characteristics, VDD=2.7V to 3.6 V*. Updated *Table 151: Dynamics characteristics: eMMC characteristics VDD=1.71 V to 1.9 V*. Updated *Section 6: Package information*. Updated *Table 163: STM32L552xx ordering information scheme*.
09-Sep-2020	5	Updated: – *Table 10: STM32L552xx modes overview*. – *Section 3.28: True random number generator (RNG)*. – *Table 77: Current consumption in Stop 1 mode*. – *Table 80: Current consumption in Shutdown mode*. – *Table 82: Peripheral current consumption*. – *Table 83: Low-power mode wakeup timings*.
21-Oct-2020	6	Updated: – *Table 10: STM32L552xx modes overview*. – *Table 14: Temperature sensor calibration values* – *Table 21: STM32L552xx pin definitions* – *Table 77: Current consumption in Stop 1 mode* – *Table 80: Current consumption in Shutdown mode*. – *Table 83: Low-power mode wakeup timings* – *Table 117: VREFBUF characteristics* – *Table 121: V_{BAT} monitoring characteristics* – *Section 3.28: True random number generator (RNG)* Added – *Figure 46: VREFBUF in case VRS = 0* – *Figure 47: VREFBUF in case VRS = 1*

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