STMUX7000

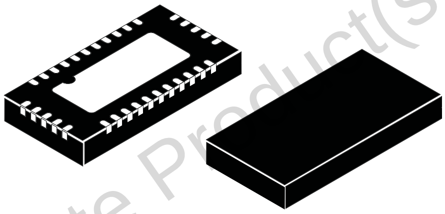
7-channel MUX/DEMUX for analog video signal

Features

- Low R_{ON}: 4.0 Ω typical
- V_{CC} operating range: 3.0 to 3.6 V
- Enhanced ESD protection: > 8 kV (contact) and 8 kV (HBM)
- Channel on capacitance: 7.8 pF typical
- Designed for VGA signal switching
- Integrated switches for RGB, HSYNC, VSYNC and DDC signals
- Very low crosstalk: -45 dB at 250 MHz
- > 1000 MHz -3 dB typical bandwidth (or data frequency)
- Low power mode for minimum power consumption
- Package: QFN32L

Applications

- Audio/video switching



QFN32
(3 x 6 mm)

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Description

The STMUX7000 is a 7-channel multiplexer/demultiplexer low R_{ON} bidirectional designed for analog video signal, such as VGA. It is designed for very low crosstalk, and high bandwidth to maintain high signal integrity.

The analog video signal multiplexed from one of two selected sources in the notebook and docking station while the unselected switch goes to Hi-Z status.

The device is also protected against high ESD that supports up to 8 kV contact on all I/O pins.

The device can be put into low power mode consuming minimum power.

Table 1. Device summary

Order code	Package	Packing
STMUX7000QTR	QFN32 (3 x 6 x 0.8 mm)	Tape and reel

Contents

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1 Pin description

Figure 1. Pin connection (top through view)

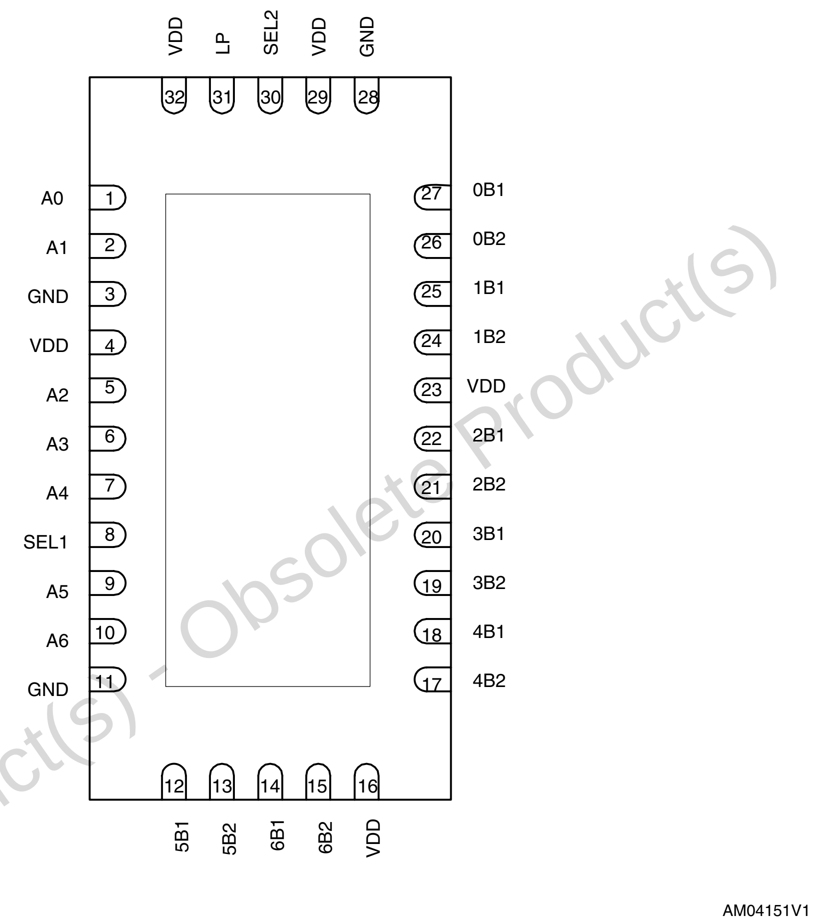

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Table 2. Pin description

Pin	Symbol	Name and function
8	SEL 1	Selecion for bit 0, 1, 2, 3, 4
30	SEL 2	Selection for bit 5, 6
1, 2, 5, 6, 7, 9, 10	A0, A1, A2, A3, A4, A5, A6	8-bit bus
4, 16, 23, 29, 32	VDD	Supply voltage
3, 11, 28	GND	Ground
27, 25, 22, 20, 18, 14, 12	0B1, 1B1, 2B1, 3B1, 4B1, 5B1, 6B1	8-bit multiplexed to bus 1
26, 24, 21, 19, 17, 15, 13	0B2, 1B2, 2B2, 3B2, 4B2, 5B2, 6B2	8-bit multiplexed to bus 2
31	LP	Low power mode enable

Figure 2. Input equivalent circuit

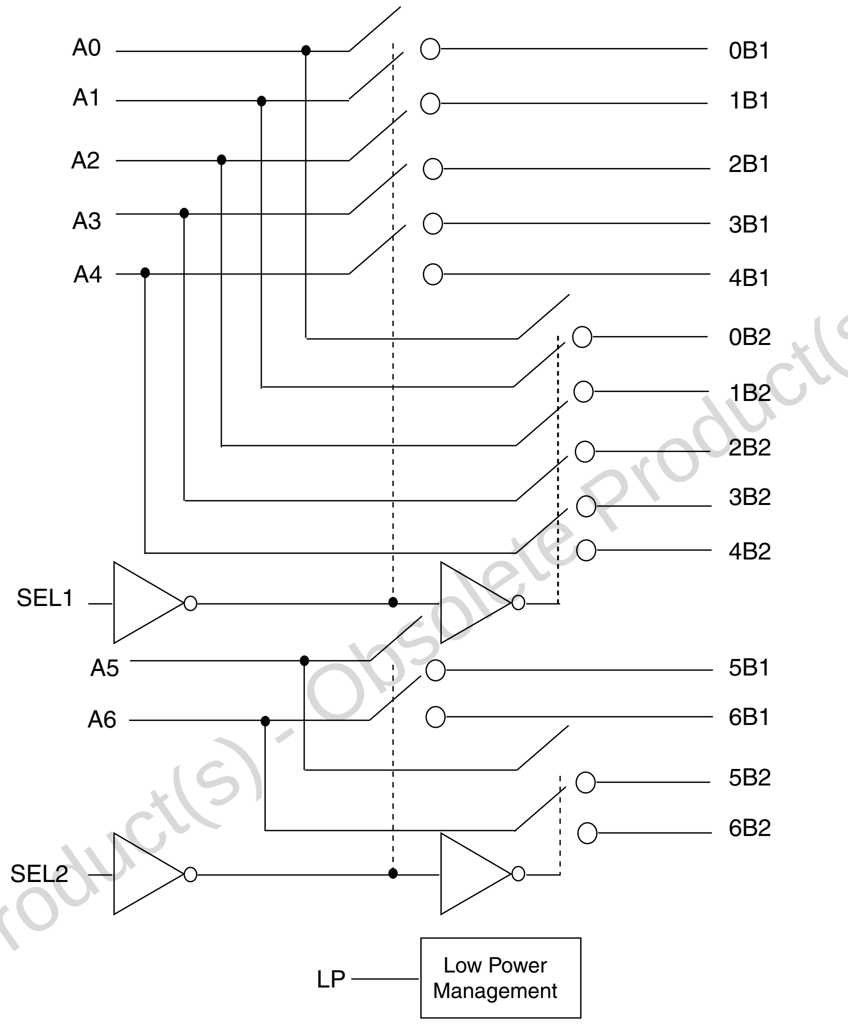

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Table 3. Bit 0, 1, 2, 3, 4 switch function table

LP	SEL 1	Function
L	L	Bit 0, 1, 2, 3, 4 multiplexed to bus 1, bus 2 in Hi-Z
L	H	Bit 0, 1, 2, 3, 4 multiplexed to bus 2, bus 1 in Hi-Z
H	X	Bus 1 and 2 in Hi-Z

Table 4. Bit 5, 6 switch function table

LP	SEL 2	Function
L	L	Bit 5,6 multiplexed to bus 1, bus 2 in Hi-Z

Table 4. Bit 5, 6 switch function table

LP	SEL 2	Function
L	H	Bit 5,6 multiplexed to bus 2, bus 1in Hi-Z
H	X	Bus 1 and 2 in Hi-Z

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2 Maximum rating

Stressing the device above the rating listed in the “absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 5. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage to ground	-0.5 to 4.6	V
V_{IO}	DC input output voltage	-0.5 to 4.6	V
V_{IC}	DC control input voltage	-0.5 to 4.6	V
I_O	DC output current(1)	120	mA
P_D	Power dissipation	0.5	W
T_{stg}	Storage temperature	-65 to 150	°C
T_L	Lead temperature (10 sec)	300	°C

1. If V_{IO} x I_O does not exceed the maximum limit of P_D.

2.1 Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage to ground	3	-	3.6	V
V_{IC}	DC control input voltage (SEL, LP)	0	-	5	V
V_{IO}	DC input/output voltage	0	-	V_{CC}	V
T_A	Operating temperature	-40	-	85	°C

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3 Electrical characteristics

Table 7. DC electrical characteristics (V_{CC} = 3.3 V ±10%)

Symbol	Parameter	Test condition	Value			Unit
			-40 to 85 °C			
			Min	Typ	Max	
V_{IH}	Voltage input high (SEL, LP)	High level guaranteed	2	-	-	V
V_{IL}	Voltage input low (SEL, LP)	Low level guaranteed	-0.5	-	0.8	V
V_{IK}	Clamp diode voltage (SEL, LP)	V_{CC} = 3.6 V I_{IN} = -18 mA	-	-0.8	-1.2	V
I_{IH}	Input high current (SEL, LP)	V_{CC} = 3.6 V V_{IN} = V_{CC}	-	-	±5	µA
I_{IL}	Input low current (SEL, LP)	V_{CC} = 3.6 V V_{IN} = GND	-	-	±5	µA
$IOFF_{(SW)}$(1)	Leakage current through the switch common terminals (A to H) (LED1 to LED3)	V_{CC} = 3.6 V A to H = V_{CC} LED1 to LED3 = V_{CC} A0 to H0 = 0 V A1 to H1 = floating LEDx_0 = 0 V LEDx1 = floating SEL = V_{CC}	-	-	±1	µA
$IOFF_{(SEL, LP)}$	SEL, LP pin leakage current	V_{CC} = 0 V SEL = 0 to 3.6 V	-	-	±1	µA
R_{ON}	Switch ON resistance(2)	V_{CC} = 3.0 V V_{IN} = 0 to 1.2 V I_{IN} = -40 mA	-	4.0	6.5	Ω
R_{FLAT}	ON resistance flatness (2)(3)	V_{CC} = 3.0 V V_{IN} at 0 and 1.2V I_{IN} = -40 mA	-	0.5	-	Ω
ΔR_{ON}	ON resistance match between channel $\Delta R_{ON} = R_{ONMAX} - R_{ONMIN}$ (2)(4)	V_{CC} = 3.0 V V_{IN} = 0 to 1.2 V I_{IN} = -40 mA	-	0.4	1	Ω

1. Refer to *Figure 4: Test circuit for leakage current (IOFF) on page 10*
2. Measured by voltage drop between channels at indicated current through the switch. ON resistance is determined by the lower of the voltages.
3. Flatness is defined as the difference between the R_{ONMAX} and R_{ONMIN} of ON resistance over the specified range.
4. ΔR_{ON} measured at same V_{CC}, temperature and voltage level.

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Table 8. Capacitance (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
C_{IN}	SEL, LP pin input capacitance(1)	DC = 0.25 V AC = 0.5 V_{PP} f = 1 MHz	-	2	3	pF
C_{OFF}	Switch off capacitance(2)	DC = 0.25 V AC = 0.5 V_{PP} f = 1 MHz	-	2.8	6.5	pF
C_{ON}	Switch on capacitance(3)	DC = 0.25 V AC = 0.5 V_{PP} f = 1 MHz	-	7.8	-	pF

1. Refer to *Figure 5 on page 11*.
2. Refer to *Figure 6 on page 11*.
3. Refer to *Figure 7 on page 12*.

Table 9. Power supply characteristics

Symbol	Parameter	Test condition	Value			Unit
			-40 to 85 °C			
			Min	Typ	Max	
I_{CC}	Active mode power supply current	V_{CC} = 3.6 V, V_{IN} = V_{CC} or GND, LP = GND	-	150	500	µA
I_{CC}	Low power mode power supply current	V_{CC} = 3.6 V, V_{IN} = V_{CC} or GND, LP = V_{CC}	-	10	15	µA

Table 10. Dynamic electrical characteristics (V_{CC} = 3.3 V ±10%)

Symbol	Parameter	Test condition	Value			Unit
			-40 to 85 °C			
			Min	Typ	Max	
X_{talk}	Crosstalk(1)	R_L = 50 Ω, R_S = 50 Ω f = 250 MHz	-	-45	-	dB
O_{IRR}	Off isolation(2)	R_L = 50 Ω, R_S = 50 Ω f = 250 MHz	-	-32	-	dB
BW	-3 dB bandwidth(3)	R_L = 50 Ω, R_S = 50 Ω $0 < V_{IN} \leq 1.2$ V	-	1000	-	MHz

1. Refer to *Figure 9 on page 13*.
2. Refer to *Figure 10 on page 14*.
3. Refer to *Figure 8 on page 12*.

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Table 11. Switching characteristics (T_A = 25 °C, V_{CC} = 3.3 V ±10%)

Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
t_{PD}	Propagation delay	V_{CC} = 3 to 3.6 V	-	0.25	-	ns
t_{PZH}, t_{PZL}	Line enable time, SE to x to x0 or x to x1	V_{CC} = 3 to 3.6 V 1 KΩ pull up/down resistor at xb1 or xB2	0.5	6.5	15	ns
t_{PHZ}, t_{PLZ}	Line disable time, SE to x to x0 or x to x1	V_{CC} = 3 to 3.6 V 1 KΩ pull up/down resistor at xb1 or xB2	0.5	16		ns
$t_{SK(O)}$	Output skew between center port to any other port	V_{CC} = 3 to 3.6 V	-	0.1	0.2	ns
$t_{SK(P)}$	Skew between opposite transition of the same output (t_{PHL}, t_{PLH})	V_{CC} = 3 to 3.6 V	-	0.1	0.2	ns

Table 12. ESD performance

Symbol	Test condition	Value			Unit
		Min	Typ	Max	
ESD	Contact discharge[(1)] IEC61000-4-2	-	±8	-	kV
	Human body model (JESD22-A114)	-	±8	-	kV

1. Refer to *Figure 3: Diagram for suggested VDD decoupling on page 10*.

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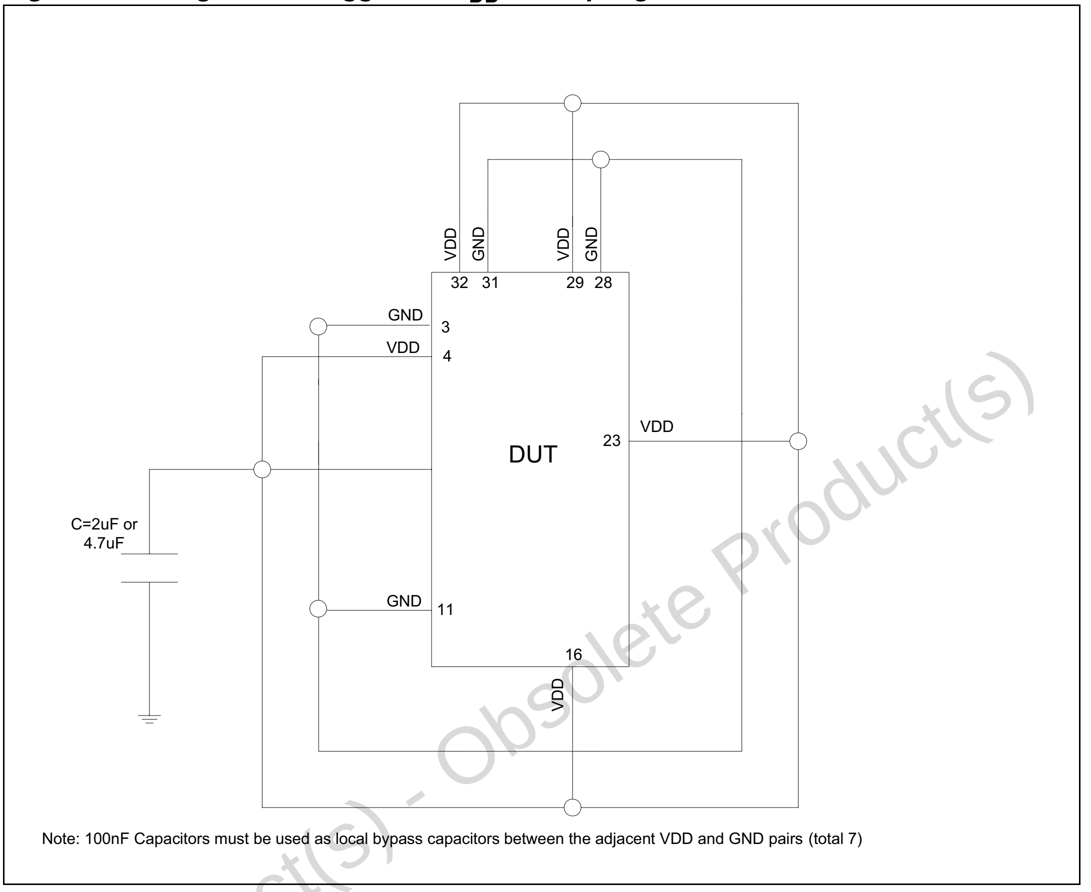
Figure 3. Diagram for suggested V_{DD} decoupling



1. Applicable for system level ESD test

Figure 4. Test circuit for leakage current (I_{OFF})

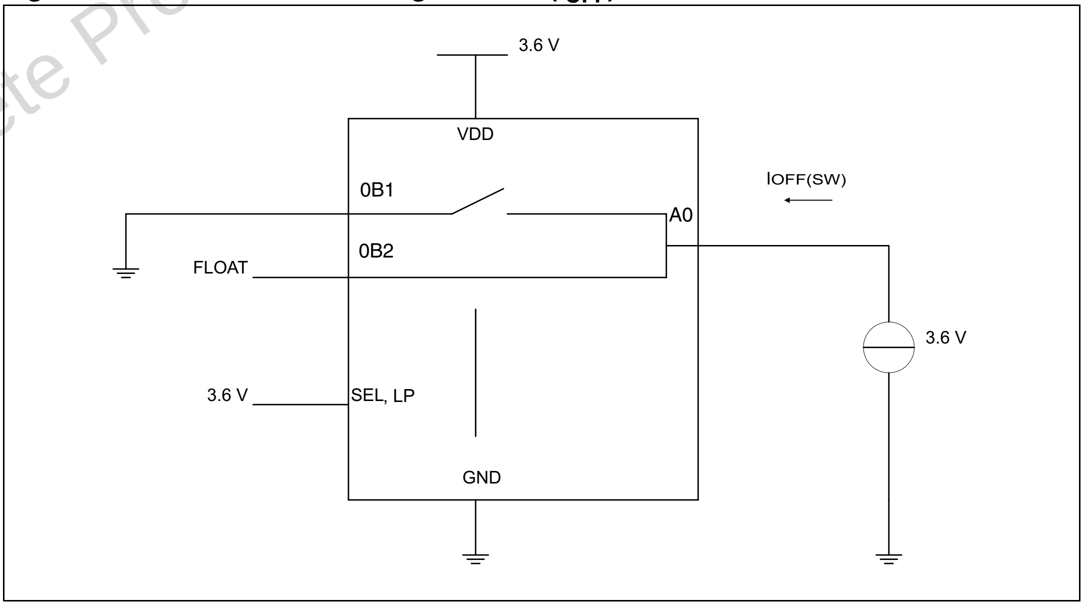


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Figure 5. Test circuit for SEL pin input capacitance (C_{IN})

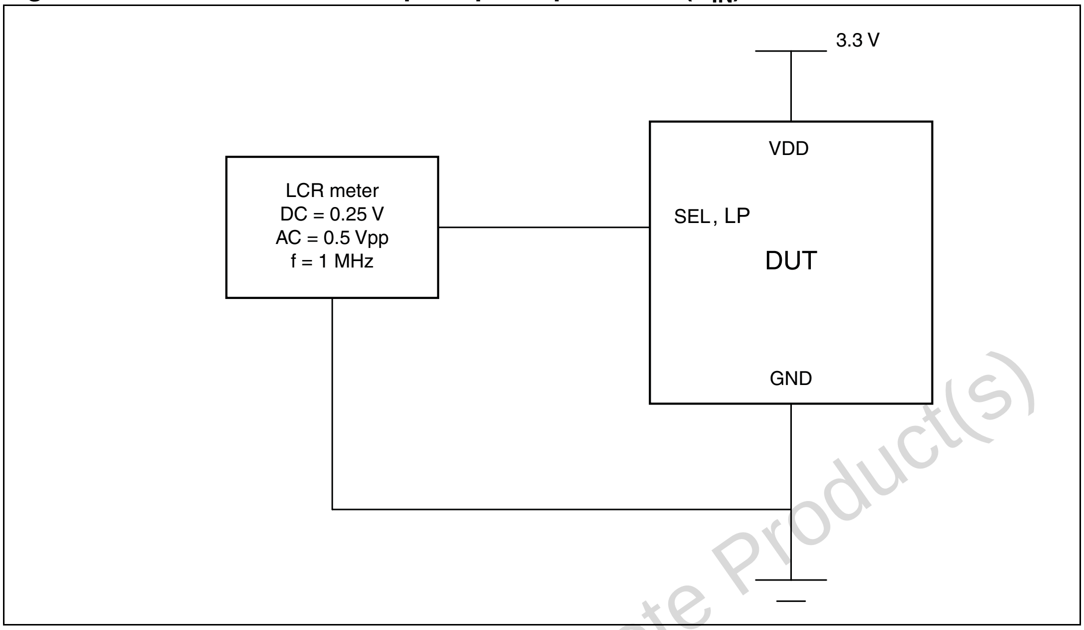

Figure 6. Test circuit for switch off capacitance (C_{OFF})

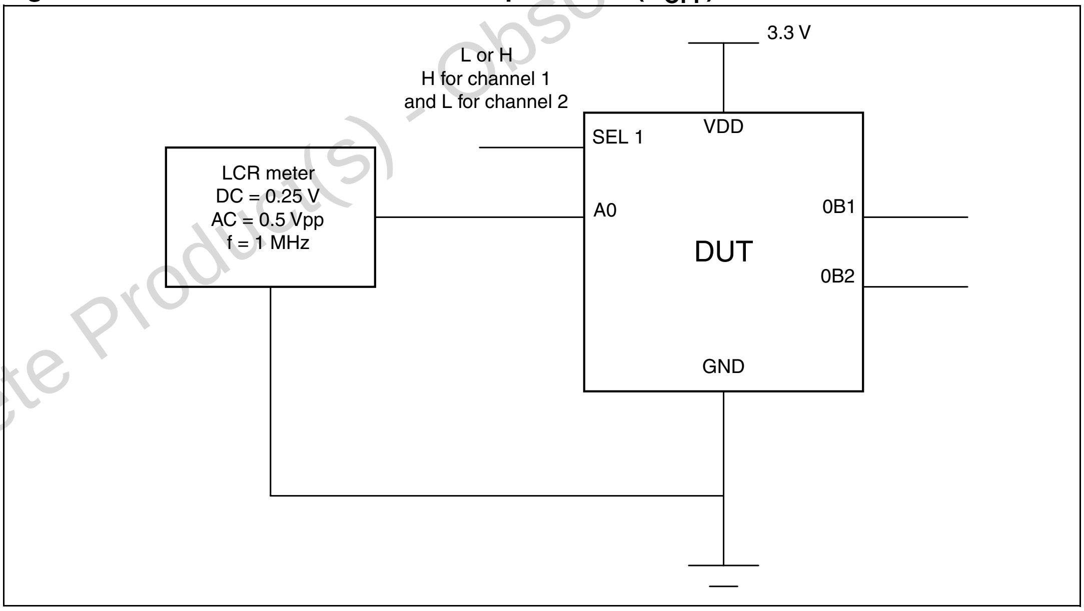

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Figure 7. Test circuit for switch on capacitance (C_{ON})

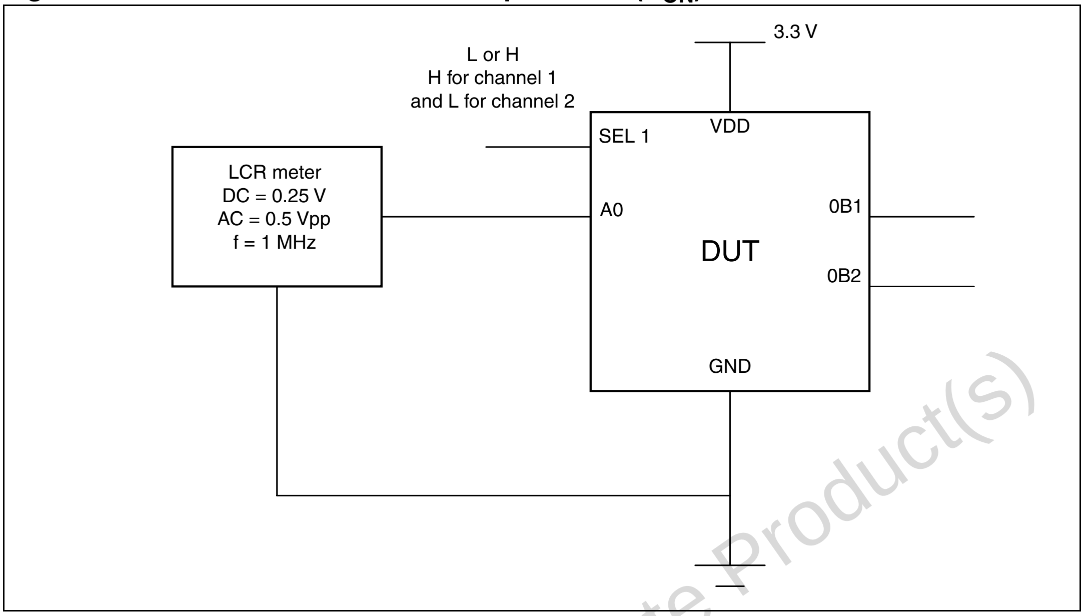
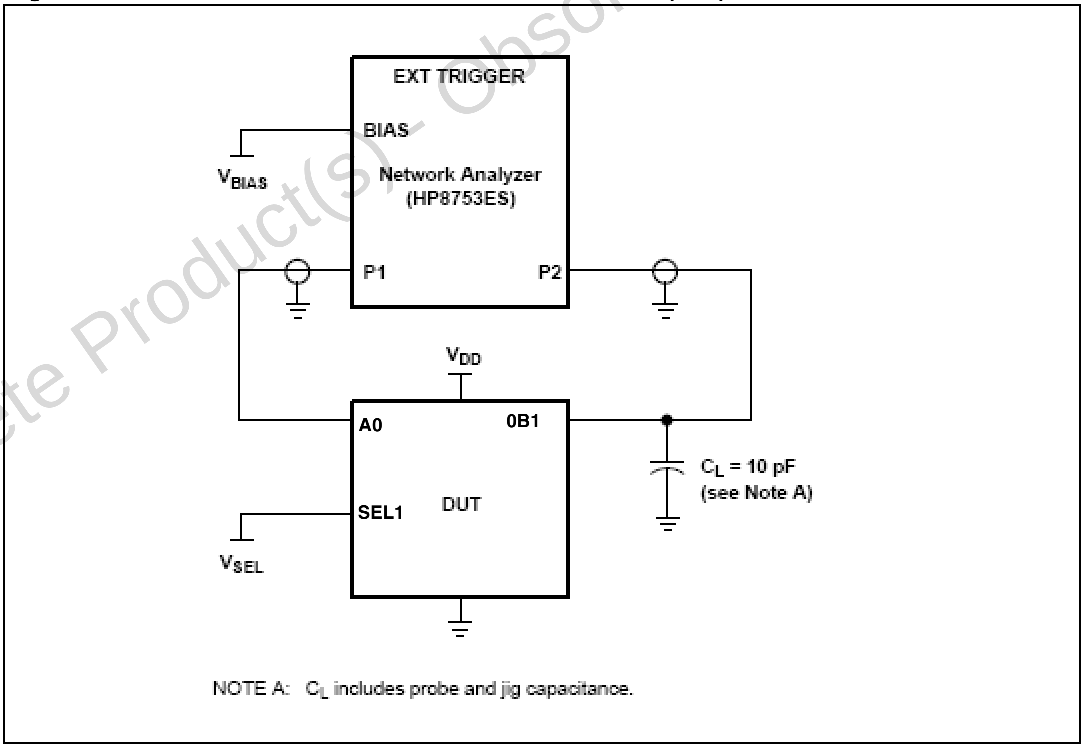


Figure 8. Test circuit for bandwidth measurement (BW)



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Frequency response is measured at the output of the ON channel. For example, when V_{SEL1} = 0 and A0 is the input, the output is measured at 0B1. All unused analog I/O ports are left open.

HP8753ES setup:

Average = 4

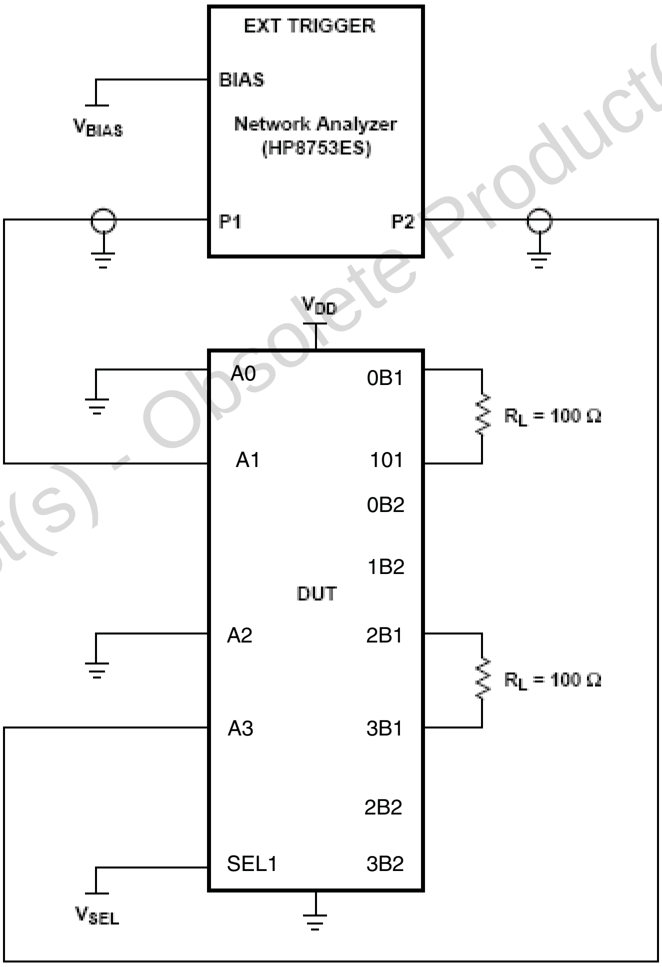
R_{BW} = 3 kHz

V_{BIAS} = 0.35 V

ST = 2 s

P1 = 0 dBm

Figure 9. Test circuit for crosstalk measurement (x_{talk})



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Crosstalk is measured at the output of the non-adjacent ON channel. For example, when V_{SEL1} = 0, and A1 is the input, the output is measured at A3. All unused analog input ports are connected to GND and output ports are left open.

HP8753ES setup:

Average = 4

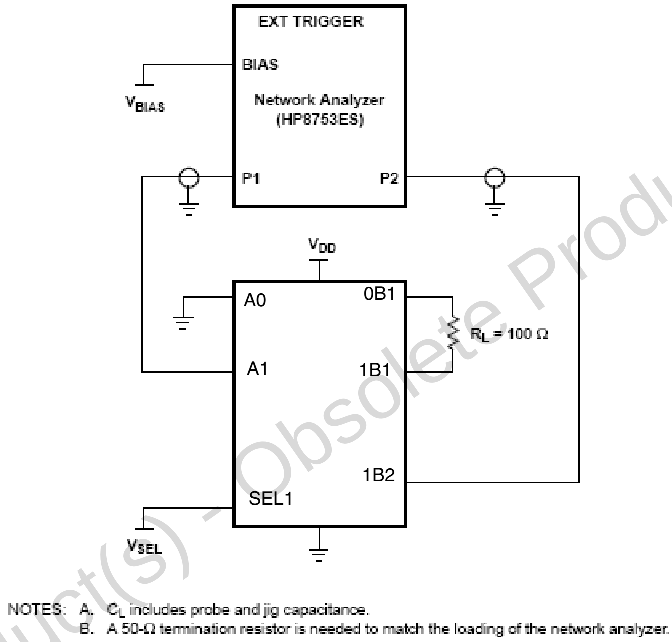
R_{BW} = 3 kHz

V_{BIAS} = 0.35 V

ST = 2 s

P1 = 0 dBm

Figure 10. Test circuit for off isolation measurement (O_{IRR})



Off isolation is measured at the output of the OFF channel. For example, when V_{SEL1} = 0, and A1 is the input, the output is measured at 1B2. All unused analog input ports are connected to GND and output ports are left open.

HP8753ES setup:

Average = 4

R_{BW} = 3 kHz

V_{BIAS} = 0.35 V

ST = 2 s

P1 = 0 dBm

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4 Package mechanical data

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Figure 11. Package outline for QFN32L (3 x 6 x 0.8 mm) - pitch 0.4 mm

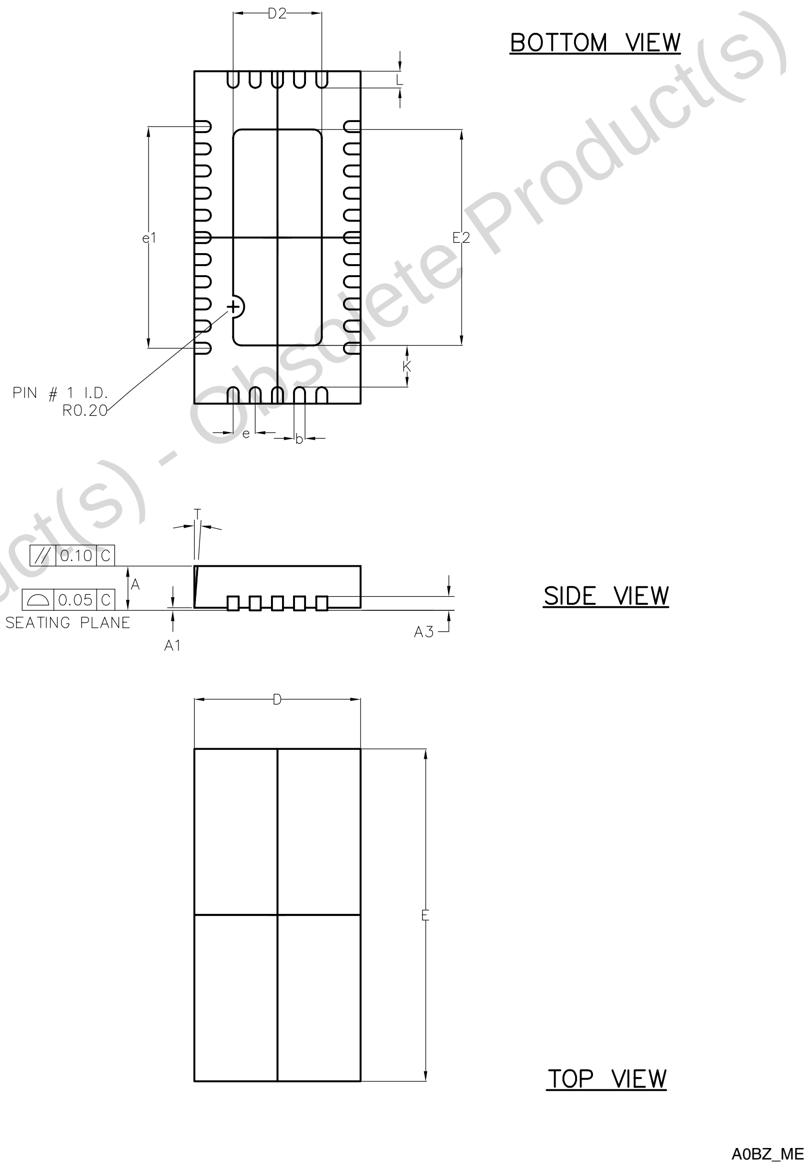

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Table 13. Mechanical data for QFN32L (3 x 6 x 0.8 mm) - pitch 0.4 mm

Symbol	Millimeters		
	Min	Typ	Max
A	0.70	0.80	0.90
A1	0.00	0.05	0.08
A3		0.25	
T	0.00		12.00
b	0.15	0.20	0.25
e		0.40	
e1		4.00	
K		0.75	
D		3.00	
E		6.00	
L	0.25	0.30	0.35
D2	1.50	1.60	1.79
E2	3.80	3.90	4.00

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Figure 12. Footprint recommendation

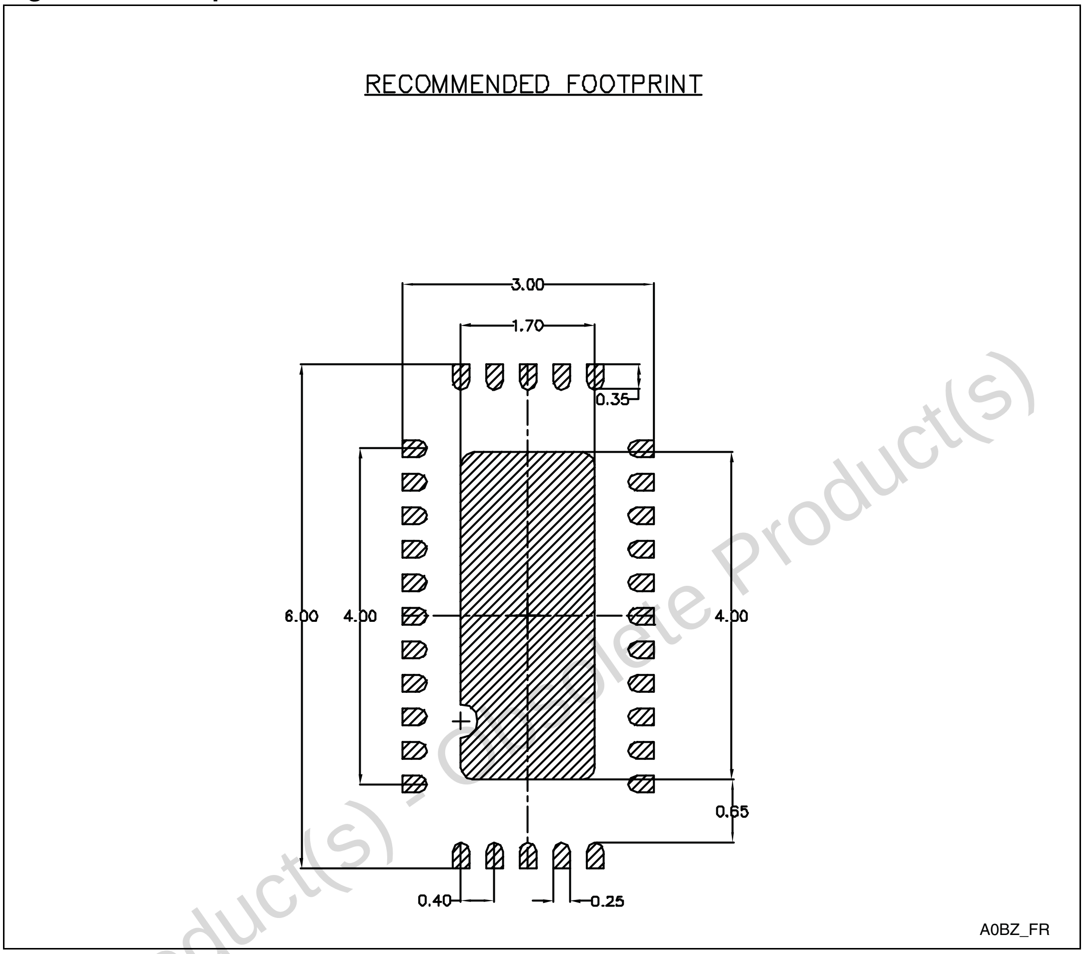

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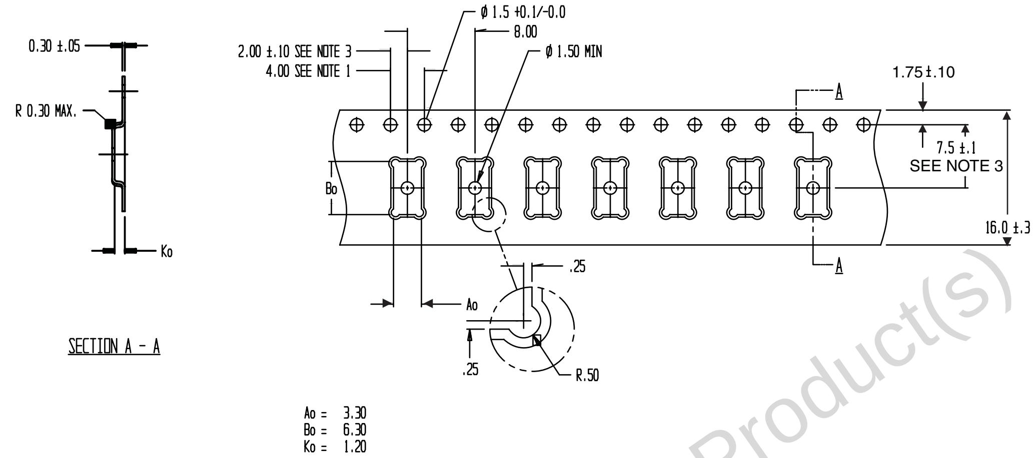
Figure 13. Carrier tape and reel information



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5 Revision history

Table 14. Document revision history

Date	Revision	Changes
23-Apr-2010	1	Initial release.
16-Jun-2010	2	Modified: *Figure 12*.
09-Mar-2011	3	Updated: *Table 8*, *Table 11* and *Table 12*.

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