

STN3NF06

N-channel 60V - 0.07Ω -4A - SOT-223 STripFET™ II Power MOSFET

General features

Туре	V _{DSS} (@Tjmax)	R _{DS(on)}	I _D
STN3NF06	60V	<0.1Ω	4A

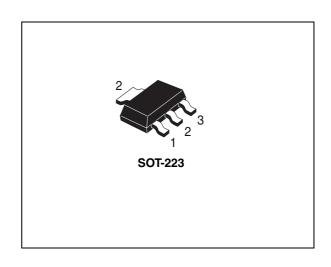
- Exceptional dv/dt capability
- 100% avalanche tested
- Avalanche rugged technology

Description

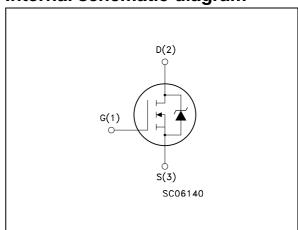
This Power MOSFET is the latest development of STMicroelectronics unique "Single Feature SizeTM" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

Applications

■ Switching application



Internal schematic diagram



Order codes

Part number	Marking	Package	Packaging	
STN3NF06	N3NF06	SOT-223	Tape & reel	

Contents STN3NF06

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STN3NF06 Electrical ratings

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source voltage (V _{GS} = 0)	60	V
V _{GS}	Gate-source voltage	± 20	V
I _D	Drain current (continuous) at T _C = 25°C	4	Α
I _D	Drain current (continuous) at T _C =100°C	2.9	Α
I _{DM} ⁽¹⁾	Drain current (pulsed)	16	Α
P _{TOT}	Total dissipation at T _C = 25°C	3.3	W
	Derating factor	0.026	W/°C
dv/dt (2)	Peak diode recovery voltage slope	10	V/ns
E _{AS} (3)	Single pulse avalanche energy	200	mJ
T _J T _{stg}	Operating junction temperature Storage temperature	-55 to 150	°C

^{1.} Pulse width limited by safe operating area

Table 2. Thermal data

Rthj-pcb	Thermal resistance junction-PCB ⁽¹⁾ max	38	°C/W
Rthj-pcb	Thermal resistance junction-PCB ⁽²⁾ max	100	°C/W
T _I ⁽³⁾	Maximum lead temperature for soldering purpose typ	260	°C

^{1.} When Mounted on FR-4 board with 1 inch² pad, 2 oz. of Cu. and t < 10 sec.

^{2.} $I_{SD} \leq 4 \text{ A, di/dt} \leq 150 \text{A/}\mu\text{s, } V_{DD} \leq V_{(BR)DSS}, T_J \leq T_{JMAX}$

^{3.} Starting $T_j = 25$ °C, $I_D = 4A$, $V_{DD} = 30V$

^{2.} When Mounted on minimum recommended footprint

^{3.} for 10 sec. 1.6 mm from case

Electrical characteristics STN3NF06

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	neter Test conditions		Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	$I_D = 250 \mu A, V_{GS} = 0$	60			V
I _{DSS}	Zero gate voltage drain current (V _{GS} = 0)	V_{DS} = Max rating, V_{DS} = Max rating @ 125°C			1 10	μ Α μ Α
I _{GSS}	Gate body leakage current (V _{DS} = 0)	V _{GS} = ±20V			± 100	nA
V _{GS(th)}	Gate threshold voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	2	3	4	V
R _{DS(on)}	Static drain-source on resistance	V _{GS} = 10V, I _D = 1.5A		0.07	0.10	Ω

Table 4. Dynamic

Symbol	Parameter	Parameter Test conditions Min.		Тур.	Max.	Unit
9 _{fs} (1)	Forward transconductance	V _{DS} = 15V, I _D =1.5A		3		S
C _{iss} C _{oss} C _{rss}	Input capacitance Output capacitance Reverse transfer capacitance	acitance $V_{DS} = 25V$, f=1 MHz, $V_{GS} = 0$		315 70 30		pF pF pF
Q _g Q _{gs} Q _{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} =48V, I_{D} = 3A V_{GS} =10V (see Figure 14)		10 3.5 3.5	13	nC nC nC

^{1.} Pulsed: pulse duration=300µs, duty cycle 1.5%

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t _{d(on)} t _r	Turn-on delay time rise time	V_{DD} =30 V, I_{D} =1.5A, R_{G} =4.7 Ω , V_{GS} =10V (see Figure 13)		7 18		ns ns
t _{d(off)}	Turn-off delay time fall time	V_{DD} =30 V, I_{D} =1.5A, R_{G} =4.7 Ω , V_{GS} =10V (see Figure 13)		17 6		ns ns

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min.	Тур.	Max	Unit
I _{SD}	Source-drain current				4	Α
I _{SDM} ⁽¹⁾	Source-drain current (pulsed)				16	Α
V _{SD} ⁽²⁾	Forward on voltage	I _{SD} =4A, V _{GS} =0			1.3	٧
t _{rr} Q _{rr} I _{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} =4 A, di/dt = 100A/ μ s, V_{DD} =25 V, Tj=150°C (see Figure 15)		50 88 3.5		ns nC A

^{1.} Pulse width limited by safe operating area.

^{2.} Pulsed: pulse duration=300µs, duty cycle 1.5%

Electrical characteristics STN3NF06

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

Figure 2. Thermal impedance

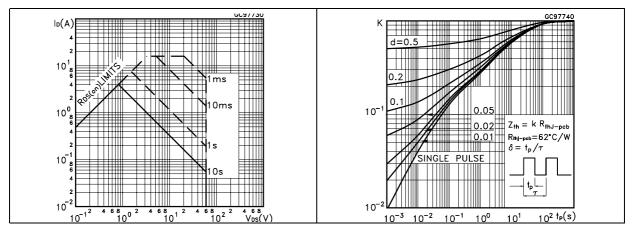


Figure 3. Output characteristics

Figure 4. Transfer characteristics

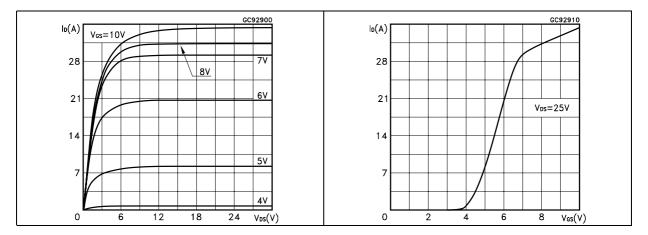
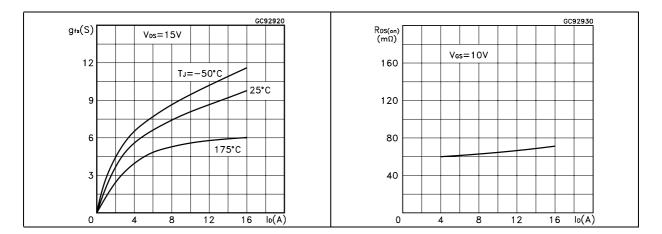


Figure 5. Transconductance

Figure 6. Static drain-source on resistance



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GC92950 Vgs(V) C(pF) f=1MHz Vgs=0V V_{DS}=48V In=3A 12 400 9 300

Gate charge vs. gate-source voltage Figure 8. **Capacitance variations** Figure 7.

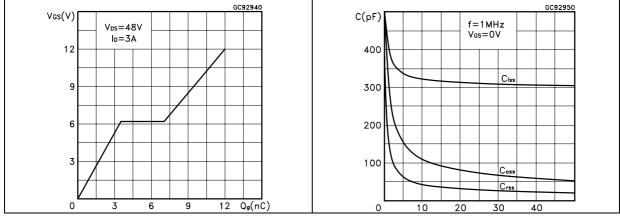


Figure 9. Normalized gate threshold voltage Figure 10. Normalized on resistance vs. vs. temperature temperature

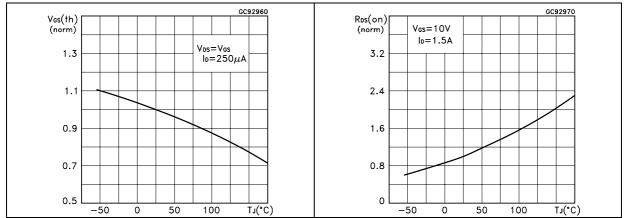
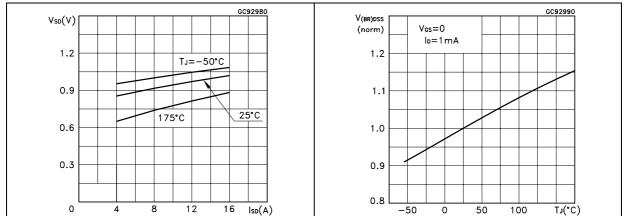


Figure 11. Source-drain diode forward characteristics

Figure 12. Normalized breakdown voltage vs. temperature



Test circuit STN3NF06

3 Test circuit

Figure 13. Switching times test circuit for resistive load

Figure 14. Gate charge test circuit

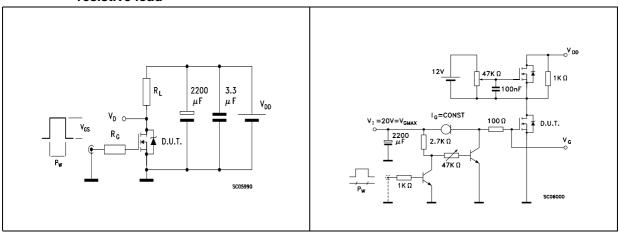


Figure 15. Test circuit for inductive load switching and diode recovery times

Figure 16. Unclamped Inductive load test circuit

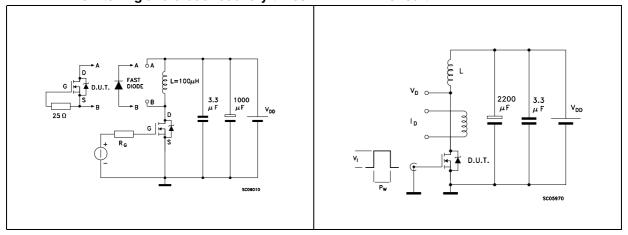
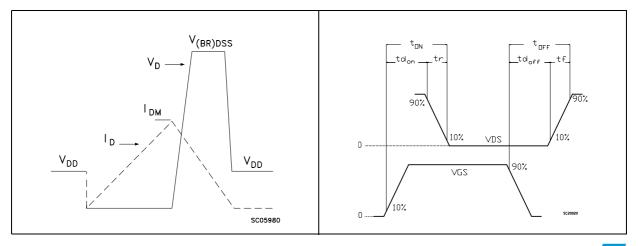


Figure 17. Unclamped inductive waveform

Figure 18. Switching time waveform



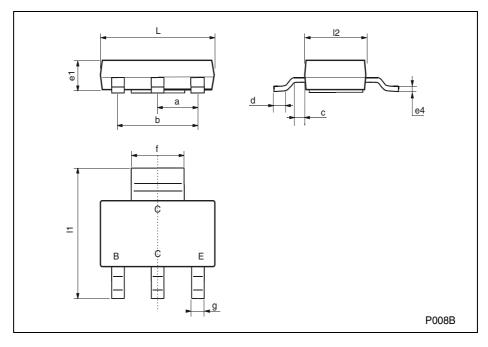
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4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

SOT-223 MECHANICAL DATA

DIM.		mm			mils	
Diw.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
а	2.27	2.3	2.33	89.4	90.6	91.7
b	4.57	4.6	4.63	179.9	181.1	182.3
С	0.2	0.4	0.6	7.9	15.7	23.6
d	0.63	0.65	0.67	24.8	25.6	26.4
e1	1.5	1.6	1.7	59.1	63	66.9
e4			0.32			12.6
f	2.9	3	3.1	114.2	118.1	122.1
g	0.67	0.7	0.73	26.4	27.6	28.7
l1	6.7	7	7.3	263.8	275.6	287.4
12	3.5	3.5	3.7	137.8	137.8	145.7
L	6.3	6.5	6.7	248	255.9	263.8



STN3NF06 Revision history

5 Revision history

Table 7. Revision history

Date	Revision	Changes
21-Jun-2004	4	Complete datasheet
04-Oct-2006	5	The document has been reformatted
01-Feb-2007	6	Typo mistake on <i>Table 1</i> .

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