STN4NF20L

N-channel 200 V, 1.1 Ω, 1 A SOT-223 low gate charge STripFET™ II Power MOSFET

Features

Order code	V_{DSS}	$R_{DS(on)}$ max.	I_D
STN4NF20L	200 V	< 1.5 Ω	1 A

■ 100% avalanche tested

■ Low gate charge

■ Exceptional dv/dt capability

Application

Switching applications

Description

This N-channel 200 V realized with STMicroelectronics unique STripFET™ process has specifically been designed to minimize input capacitance and gate charge. It is therefore suitable as primary switch in advanced high efficiency isolated DC-DC converters.
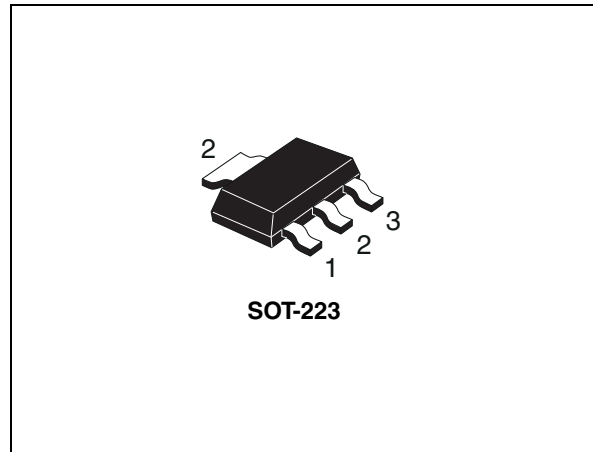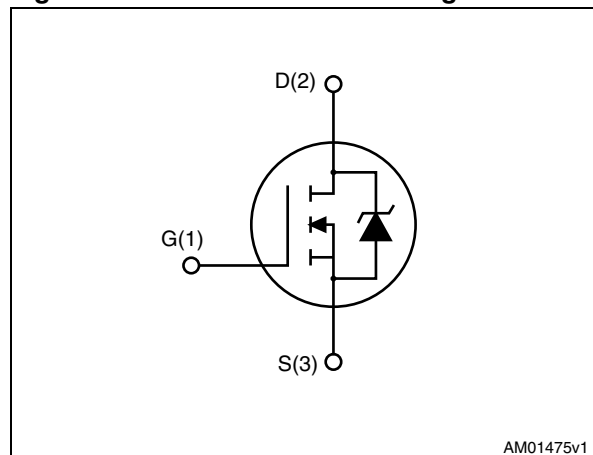

SOT-223

Figure 1.   Internal schematic diagram

AM01475v1

Table 1.   Device summary

Order code	Marking	Package	Packaging
STN4NF20L	4NF20L	SOT-223	Tape and reel

Contents

1 Electrical ratings

Table 2.   Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current continuous T_C = 25 °C	1	A
I_D	Drain current continuous T_C = 100 °C	0.63	A
I_{DM} [1]	Drain current pulsed	4	A
P_{TOT} [2]	Total dissipation at T_C = 25 °C	3.3	W
dv/dt [3]	Peak diode recovery voltage slope	20	V/ns
T_j T_{stg}	Operating junction temperature Storage temperature	- 55 to 150	°C

1. Pulse width limited by safe operating area.

2. This value is rated according to Rthj-amb ≤ 10 sec.

3. Isd ≤ 1 A, di/dt ≤ 200 A/μs, V_{DD} ≤ 80% $V_{(BR)DSS}$.

Table 3.   Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-amb}$ [1]	Thermal resistance junction to ambient	38	°C/W
$R_{thj-amb}$ [2]		62.5	°C/W

1. When mounted on 1 inch² FR-4 board, 2 oz. Cu, (t < 10 sec).

2. When mounted on 1 inch² FR-4 board, 2 oz. Cu, (t > 10 sec).

Table 4.   Thermal data

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetetive or not repetetive[1]	1	A
E_{AS}	Single pulse avalanche energy [2]	90	mJ

1. Pulse width limited by T_{JMAX}.

2. Starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V.

2 Electrical characteristics

(Tcase = 25 °C unless otherwise specified)

Table 5. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	200			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating V_{DS} = Max rating, T_C=125 °C			1 50	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V, V_{DS}=0			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{GS} = V_{DS}, I_D = 250 μA	1	2	3	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 0.5 A V_{GS} = 5 V, I_D = 0.5 A		1.1 1.13	1.5 1.55	Ω Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0	-	150 30 4	-	pF pF pF
R_g	Instrinsic gate resistance	f=1 MHz open drain	-	5.5	-	Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 160 V, I_D = 1 A, V_{GS} = 10 V (see *Figure 13*)	-	0.9 2.6 6.9	-	nC nC nC

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(v)}$ t_r t_f $t_{c(off)}$	Voltage delay time Voltage rise time Current fall time Crossing time	V_{DD} = 100 V, I_D = 0.5 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 12*)	-	3.6 2 10.4 15.4	-	ns ns ns ns

Table 8. **Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} [1]	Source-drain current Source-drain current (pulsed)		-		1 4	A A
V_{SD} [2]	Forward on voltage	I_{SD} = 1 A, V_{GS} = 0	-		1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 1 A, di/dt = 100 A/μs V_{DD} = 60 V (see *Figure 14*)	-	51 90 3.5		ns nC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 1 A, di/dt = 100 A/μs V_{DD} = 60 V, T_j = 150 °C (see *Figure 14*)	-	56 105 3.7		ns nC A

1. Pulse width limited by safe operating area

2. Pulsed: pulse duration = 300 μs, duty cycle 1.5%

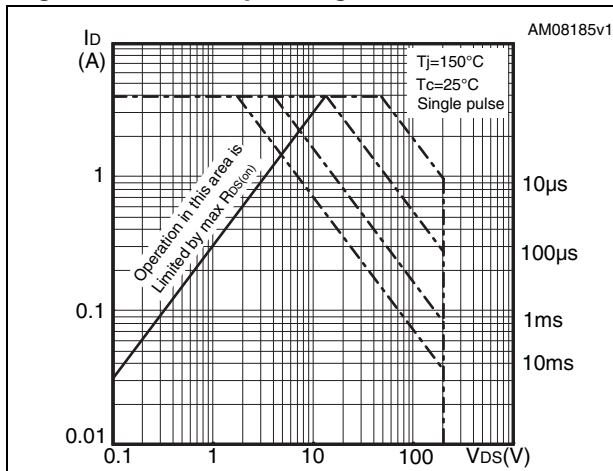# 2.1 Electrical characteristics (curves)

Figure 2.   Safe operating area

Figure 3.   Thermal impedance
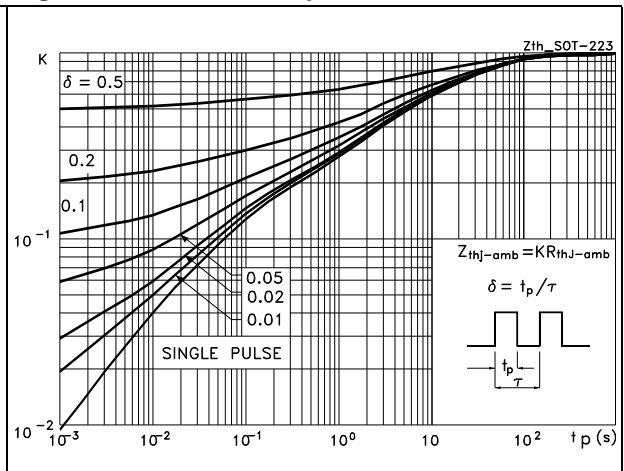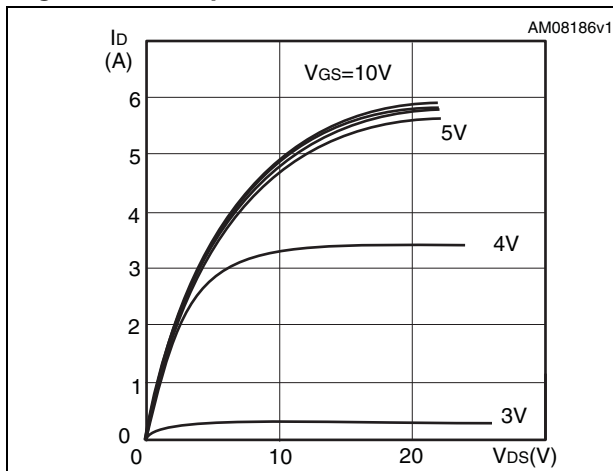

Figure 4.   Output characteristics

Figure 5.   Transfer characteristics

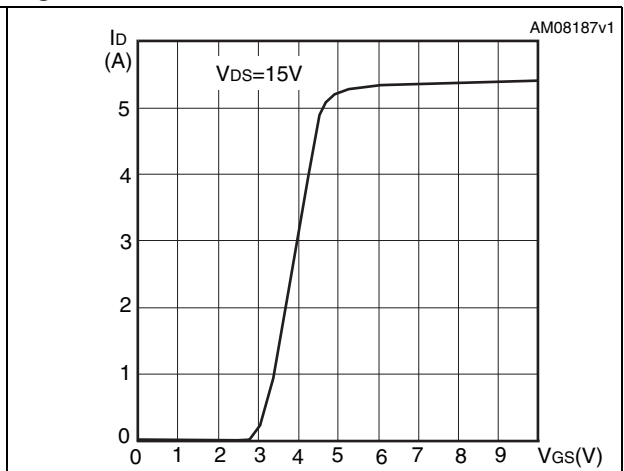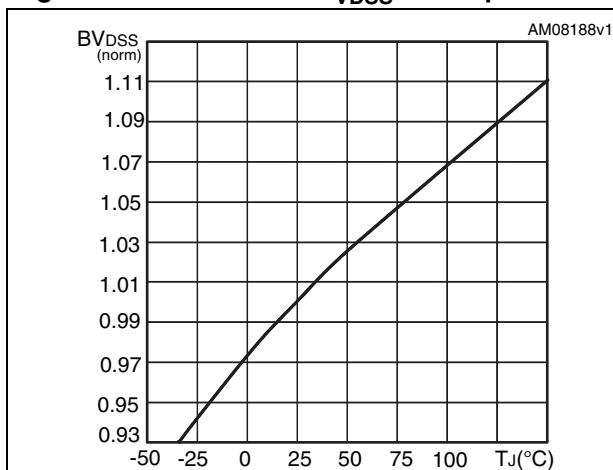**Figure 6.   Normalized B$_{VDSS}$ vs temperature**

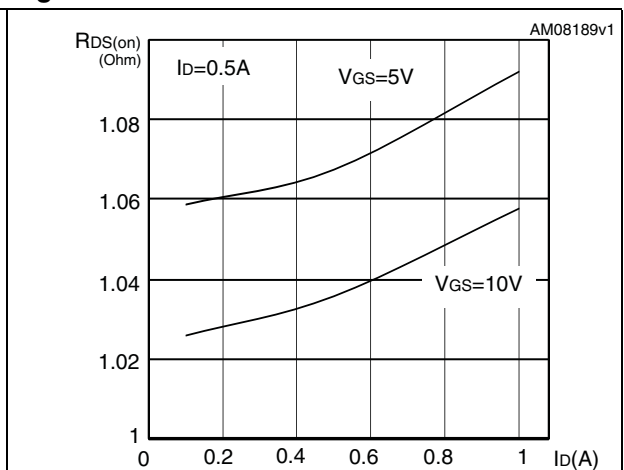**Figure 7.   Static drain-source on resistance**

Figure 8.   **Gate charge vs gate-source voltage**

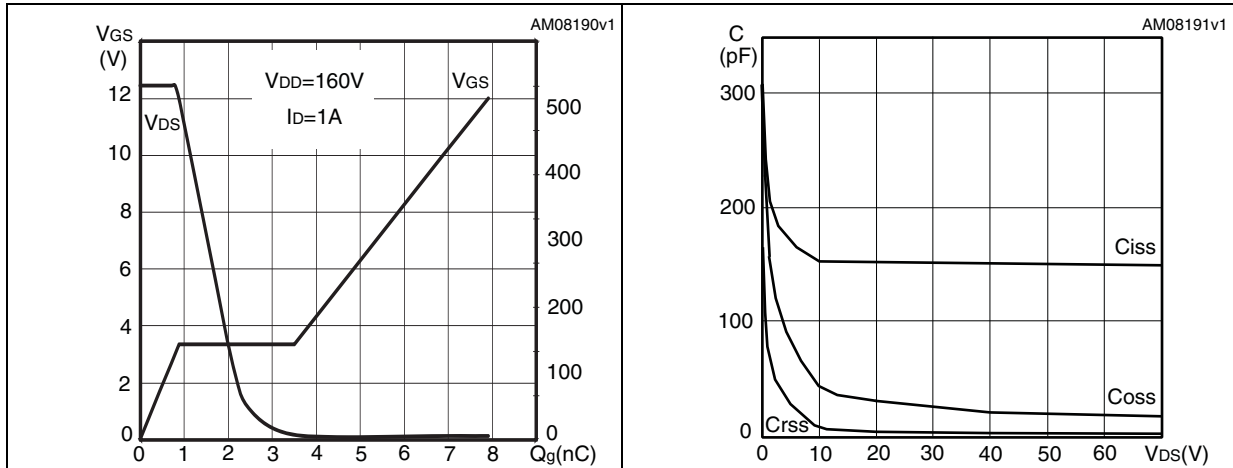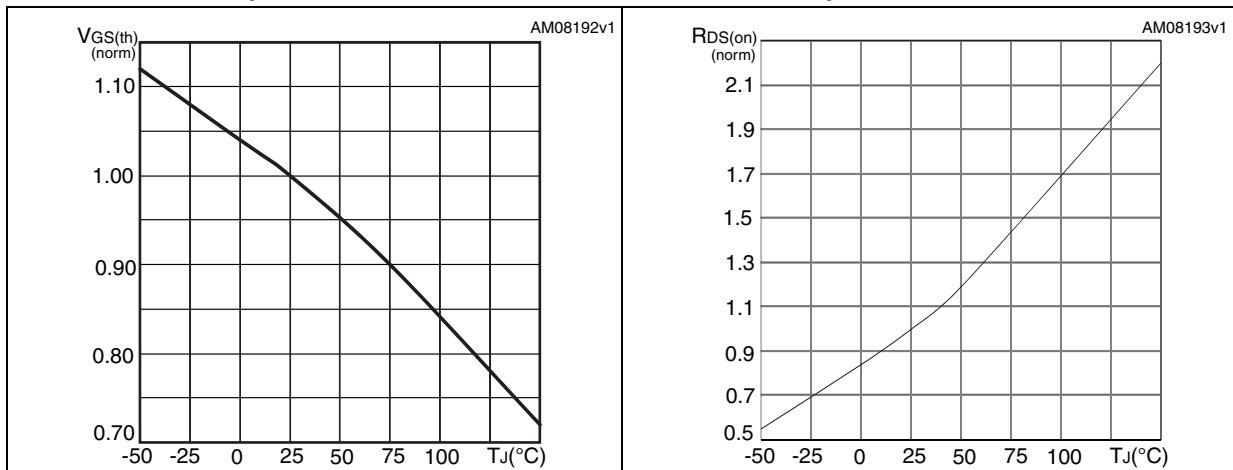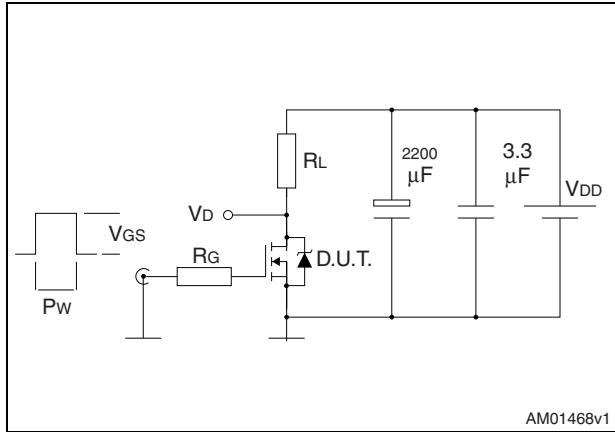**Figure 9.**   **Capacitance variations**

Figure 10.   **Normalized gate threshold voltage vs temperature**

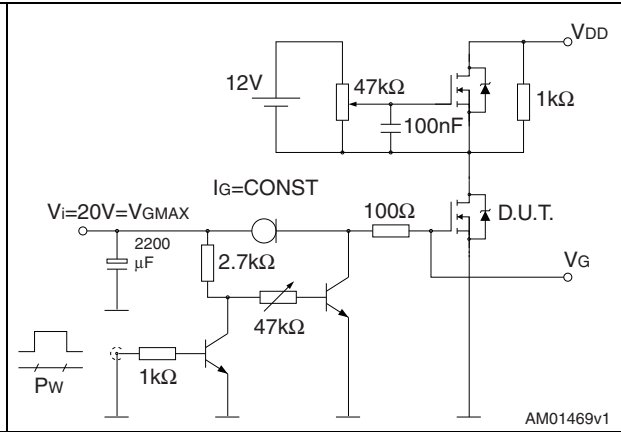**Figure 11.**   **Normalized on resistance vs temperature**

3 Test circuits

Figure 12. Switching times test circuit for resistive load
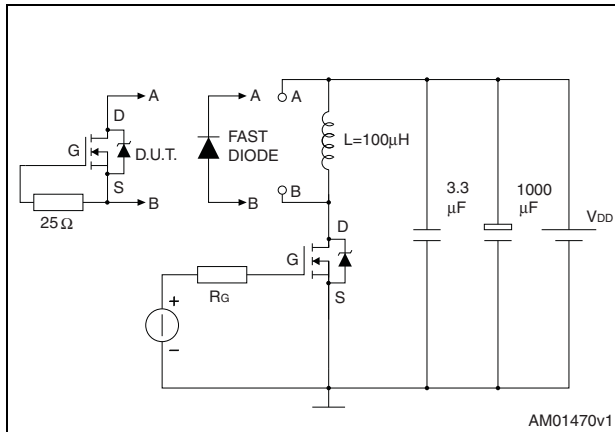

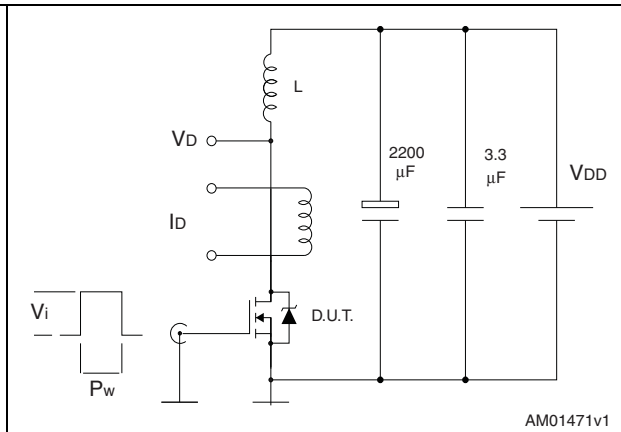AM01468v1

Figure 13. Gate charge test circuit

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Figure 14. Test circuit for inductive load switching and diode recovery times
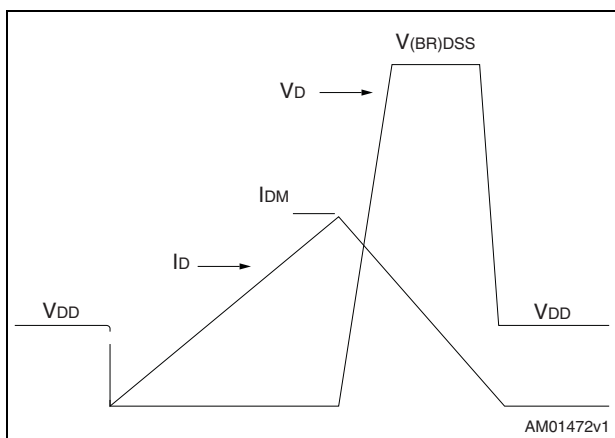

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Figure 15. Unclamped inductive load test circuit

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Figure 16. Unclamped inductive waveform
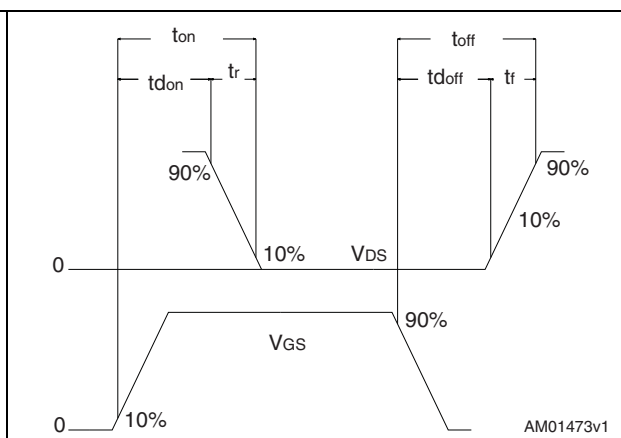

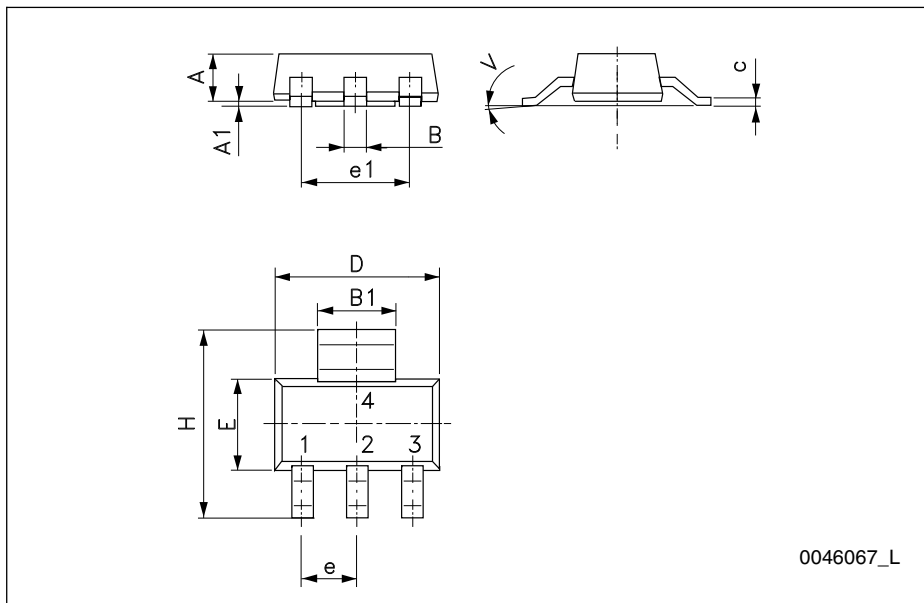AM01472v1

Figure 17. Switching time waveform

AM01473v1

4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

	mm.		
DIM.	**min.**	**typ**	**max.**
A			1.80
A1	0.02		0.1
B	0.60	0.70	0.85
B1	2.90	3.00	3.15
c	0.24	0.26	0.35
D	6.30	6.50	6.70
e		2.30	
e1		4.60	
E	3.30	3.50	3.70
H	6.70	7.00	7.30
V			10 º

SOT-223 mechanical data

0046067_L

5 Revision history

Table 9. **Document revision history**

Date	Revision	Changes
29-Apr-2010	1	First release.
11-Oct-2010	2	Document status promoted from preliminary data to datasheet.

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